

FEATURES

- **Ultra-Low Offset Voltage**
 $T_A = 25^\circ\text{C}$ $10\mu\text{V}$ Max
 $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ $20\mu\text{V}$ Max
- **Outstanding Offset Voltage Drift** $0.1\mu\text{V}/^\circ\text{C}$ Max
- **Excellent Open-Loop Gain and Gain Linearity** $12\text{V}/\mu\text{V}$ Typ
- **CMRR** 130dB Min
- **PSRR** 120dB Min
- **Low Supply Current** 2.0 mA Max
- **Fits Industry Standard Precision Op Amp Sockets (OP07/OP77)**

ORDERING INFORMATION †

CERDIP 8-PIN	PACKAGE			OPERATING TEMPERATURE RANGE
	PLASTIC 8-PIN	LCC 20-PIN	SO 8-PIN	
OP177AZ*	-	-	-	MIL
OP177BZ*	-	OP177BRC/883	-	MIL
OP177EZ	-	-	-	XIND
OP177FZ	OP177FP	-	-	XIND
OP177GZ	OP177GP	-	OP177GS	XIND

MIL = -55°C to $+125^\circ\text{C}$ XIND = -40°C to $+85^\circ\text{C}$

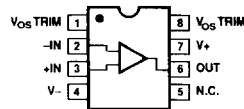
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The OP-177 features the highest precision performance of any op amp currently available. Offset voltage of the OP-177 is only $10\mu\text{V}$ MAX at room temperature and $20\mu\text{V}$ MAX over the full military temperature range of -55°C to $+125^\circ\text{C}$. The ultra-low V_{OS} of the OP-177, combines with its exceptional offset voltage

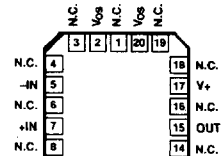
PIN CONNECTIONS



**EPOXY MINI-DIP
(P-Suffix)**

**8-PIN HERMETIC DIP
(Z-Suffix)**

**8-PIN SO
(S-Suffix)**



**OP-177BRC/883
LCC
(RC-Suffix)**

drift (TCV_{OS}) of $0.1\mu\text{V}/^\circ\text{C}$ MAX, to eliminate the need for external V_{OS} adjustment and increases system accuracy over temperature.

The OP-177's open-loop gain of $12\text{V}/\mu\text{V}$ is maintained over the full $\pm 10\text{V}$ output range. CMRR of 130dB MIN, PSRR of 120dB MIN, and maximum supply current of 2mA are just a few examples of the excellent performance of this operational amplifier. The OP-177's combination of outstanding specifications insure accurate performance in high closed-loop gain applications.

This low noise bipolar input op amp is also a cost effective alternative to chopper-stabilized amplifiers. The OP-177 provides chopper-type performance without the usual problems of high noise, low frequency chopper spikes, large physical size, limited common-mode input voltage range, and bulky external storage capacitors.

Continued

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

OP177

GENERAL DESCRIPTION *Continued*

The OP-177 is offered in both the -55°C to $+125^{\circ}\text{C}$ military, and the -40°C to $+85^{\circ}\text{C}$ extended industrial temperature ranges. This product is available in 8-pin ceramic and epoxy DIPs, as well as the space saving 8-pin Small-Outline (SO) and the Leadless Chip Carrier (LCC) packages.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 22\text{V}$
Differential Input Voltage	$\pm 30\text{V}$
Input Voltage (Note 1)	$\pm 22\text{V}$
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
Z and RC Packages	-65°C to $+150^{\circ}\text{C}$
P Package	-65°C to $+125^{\circ}\text{C}$

Operating Temperature Range

OP-177A, OP-177B	-55°C to $+125^{\circ}\text{C}$
OP-177E, OP-177F, OP-177G	-40°C to $+85^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 sec)	300°C
Junction Temperature (T_j)	-65°C to $+150^{\circ}\text{C}$

PACKAGE TYPE	θ_{JA} (NOTE 2)	θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	$^{\circ}\text{C}/\text{W}$
8-Pin Plastic DIP (P)	103	43	$^{\circ}\text{C}/\text{W}$
20-Contact LCC (RC)	98	38	$^{\circ}\text{C}/\text{W}$
8-Pin SO (S)	158	43	$^{\circ}\text{C}/\text{W}$

NOTES:

- For supply voltages less than $\pm 22\text{V}$, the absolute maximum input voltage is equal to the supply voltage.
- θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = +25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177A			OP-177B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		–	4	10	–	10	25	μV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)	–	0.2	–	–	0.2	–	$\mu\text{V}/\text{Mo}$
Input Offset Current	I_{OS}		–	0.3	1.0	–	0.3	1.5	nA
Input Bias Current	I_B		–0.2	–	1.5	–0.2	–	2.0	nA
Input Noise Voltage	e_n	$f_o = 1\text{Hz to }100\text{Hz}$ (Note 2)	–	118	150	–	118	150	nV_{RMS}
Input Noise Current	i_n	$f_o = 1\text{Hz to }100\text{Hz}$ (Note 2)	–	3	8	–	3	8	pA_{RMS}
Input Resistance Differential-Mode	R_{IN}	(Note 3)	26	45	–	26	45	–	M Ω
Input Resistance Common-Mode	R_{INCM}		–	200	–	–	200	–	G Ω
Input Voltage Range	IVR	(Note 4)	± 13	± 14	–	± 13	± 14	–	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{V}$	130	140	–	130	140	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{V to } \pm 18\text{V}$	120	125	–	115	125	–	dB
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$ (Note 5)	5000	12000	–	5000	12000	–	V/mV
Output Voltage Swing	V_O	$R_L \geq 10\text{k}\Omega$ $R_L \geq 2\text{k}\Omega$ $R_L \geq 1\text{k}\Omega$	± 13.5 ± 12.5 ± 12.0	± 14.0 ± 13.0 ± 12.5	–	± 13.5 ± 12.5 ± 12.0	± 14.0 ± 13.0 ± 12.5	–	V
Slew Rate	SR	$R_L \geq 2\text{k}\Omega$ (Note 2)	0.1	0.3	–	0.1	0.3	–	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 2)	0.4	0.6	–	0.4	0.6	–	MHz
Open-Loop Output Resistance	R_O		–	60	–	–	60	–	Ω
Power Consumption	Pd	$V_S = \pm 15\text{V}$, No Load $V_S = \pm 3\text{V}$, No Load	–	50 3.5	60 4.5	–	50 3.5	60 4.5	mW
Supply Current	I_{SY}	$V_S = \pm 15\text{V}$, No Load	–	1.6	2.0	–	1.6	2.0	mA
Offset Adjustment Range		$R_p = 20\text{k}\Omega$	–	± 3	–	–	± 3	–	mV

NOTES:

- Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than $2.0\mu\text{V}$.

- Sample tested.
- Guaranteed by design.
- Guaranteed by CMRR test condition.
- To insure high open-loop gain throughout the $\pm 10\text{V}$ output range, A_{VO} is tested at $-10\text{V} \leq V_O \leq 0\text{V}$, $0\text{V} \leq V_O \leq +10\text{V}$, and $-10\text{V} \leq V_O \leq +10\text{V}$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177A			OP-177B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		-	10	20	-	25	55	μV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	-	0.03	0.1	-	0.1	0.3	$\mu V/^\circ C$
Input Offset Current	I_{OS}		-	0.5	1.5	-	0.5	2.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	-	1.5	25	-	1.5	25	$\mu A/^\circ C$
Input Bias Current	I_B		-0.2	2.4	4	-0.2	2.4	4	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	-	8	25	-	8	25	$\mu A/^\circ C$
Input Voltage Range	IVR	(Note 3)	± 13	± 13.5	-	± 13	± 13.5	-	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	120	140	-	120	140	-	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	120	125	-	110	120	-	dB
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ (Note 4)	2000	6000	-	2000	6000	-	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13.0	-	± 12	± 13.0	-	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	-	60	75	-	60	75	mW
Supply Current	I_{SY}	$V_S = \pm 15V$, No Load	-	2.0	2.5	-	2.0	2.5	mA

NOTES:

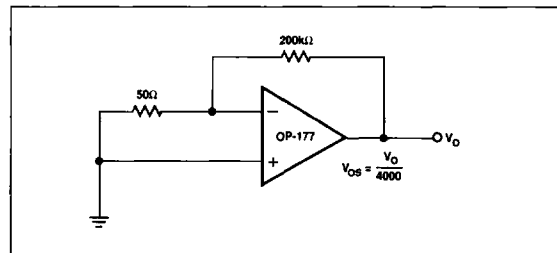
1. TCV_{OS} is 100% tested.
2. Guaranteed by end-point limits.

3. Guaranteed by CMRR test condition.

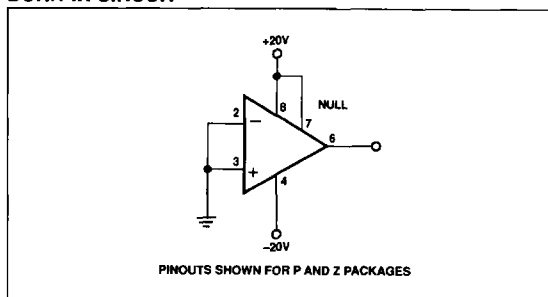
4. To insure high open-loop gain throughout the $\pm 10V$ output range, A_{VO} is tested at $-10V \leq V_O \leq 0V$, $0V \leq V_O \leq +10V$, and $-10V \leq V_O \leq +10V$.

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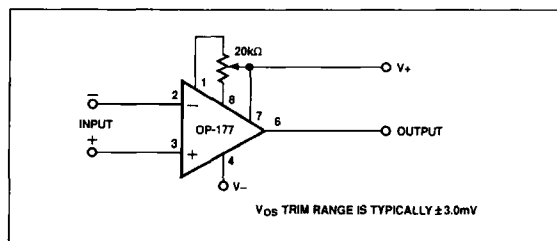
TYPICAL OFFSET VOLTAGE TEST CIRCUIT



BURN-IN CIRCUIT



OPTIONAL OFFSET NULLING CIRCUIT



OP177

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177E			OP-177F			OP-177G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		-	4	10	-	10	25	-	20	60	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 1)	-	0.2	-	-	0.3	-	-	0.4	-	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		-	0.3	1.0	-	0.3	1.5	-	0.3	2.8	nA
Input Bias Current	I_B		-0.2	1.0	1.5	-0.2	1.2	2.0	-0.2	1.2	2.8	nA
Input Noise Voltage	e_n	$f_o = 1\text{Hz to } 100\text{Hz}$ (Note 2)	-	118	150	-	118	150	-	118	150	nV_{RMS}
Input Noise Current	i_n	$f_o = 1\text{Hz to } 100\text{Hz}$ (Note 2)	-	3	8	-	3	8	-	3	8	pA_{RMS}
Input Resistance – Differential-Mode	R_{IN}	(Note 3)	26	45	-	26	45	-	18.5	45	-	$M\Omega$
Input Resistance – Common-Mode	R_{INCM}		-	200	-	-	200	-	-	200	-	$G\Omega$
Input Voltage Range	IVR	(Note 4)	± 13	± 14	-	± 13	± 14	-	± 13	± 14	-	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	130	140	-	130	140	-	115	140	-	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V \text{ to } \pm 18V$	120	125	-	115	125	-	110	120	-	dB
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ (Note 5)	5000	12000	-	5000	12000	-	2000	6000	-	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 13.5 ± 12.5 ± 12.0	± 14.0 ± 13.0 ± 12.5	-	± 13.5 ± 12.5 ± 12.0	± 14.0 ± 13.0 ± 12.5	-	± 13.5 ± 12.5 ± 12.0	± 14.0 ± 13.0 ± 12.5	-	V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	-	0.1	0.3	-	0.1	0.3	-	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 2)	0.4	0.6	-	0.4	0.6	-	0.4	0.6	-	MHz
Open-Loop Output Resistance	R_O		-	60	-	-	60	-	-	60	-	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load	-	50 3.5	60 4.5	-	50 3.5	60 4.5	-	50 3.5	60 4.5	mW
Supply Current	I_{SY}	$V_S = \pm 15V$, No Load	-	1.6	2.0	-	1.6	2.0	-	1.6	2.0	mA
Offset Adjustment Range		$R_P = 20k\Omega$	-	± 3	-	-	± 3	-	-	± 3	-	mV

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0 μV .
2. Sample tested.
3. Guaranteed by design.
4. Guaranteed by CMRR test condition.
5. To insure high Open-loop gain throughout the $\pm 10V$ output range, A_{VO} is tested at $-10V \leq V_O \leq 0V$, $0V \leq V_O \leq +10V$, and $-10V \leq V_O \leq +10V$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177E			OP-177F			OP-177G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		-	10	20	-	15	40	-	20	100	μV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	-	0.03	0.1	-	0.1	0.3	-	0.7	1.2	$\mu V/^\circ C$
Input Offset Current	I_{OS}		-	0.5	1.5	-	0.5	2.2	-	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	-	1.5	25	-	1.5	40	-	1.5	85	$pA/^\circ C$
Input Bias Current	I_B		-0.2	2.4	4.0	-0.2	2.4	4.0	-	2.4	± 6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	-	8	25	-	8	40	-	15	60	$pA/^\circ C$
Input Voltage Range	IVR	(Note 3)	± 13.0	± 13.5	-	± 13.0	± 13.5	-	± 13.0	± 13.5	-	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	120	140	-	120	140	-	110	140	-	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	120	125	-	110	120	-	106	115	-	dB
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	2000	6000	-	2000	6000	-	1000	4000	-	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 13.0	-	± 12.0	± 13.0	-	± 12.0	± 13.0	-	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	-	60	75	-	60	75	-	60	75	mW
Supply Current	I_{SY}	$V_S = \pm 15V$, No Load	-	2.0	2.5	-	2.0	2.5	-	2.0	2.5	mA

NOTES:

- OP177E and OP177F: TCV_{OS} is 100% tested.
- Guaranteed by end-point limits.

- Guaranteed by CMRR test condition.

- To insure high open-loop gain throughout the $\pm 10V$ output range, A_{VO} is tested at $-10V \leq V_O \leq 0V$, $0V \leq V_O \leq +10V$, and $-10V \leq V_O \leq +10V$.