HM658128 Series

T-46-23-25

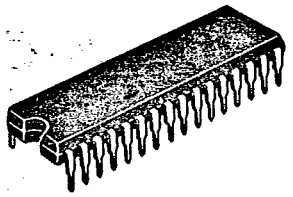
131072-word x 8-bit High Speed CMOS Pseudo Static RAM

The Hitachi HM658128 is a pseudo-static RAM organized as 131,072-word x 8-bit. HM658128 realizes low power consumption and high speed access time by employing 1.3μm CMOS process technology.

The HM658128 supports 3 refresh functions: Address Refresh, Auto Refresh and Self Refresh. Low power version dissipates only 0.5mW (typ.) in Self Refresh Mode and retains the data with battery backup for short time.

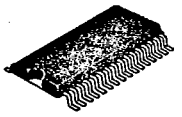
The HM658128 is pin-compatible with 256k-bit PSRAM and static RAM.

HM658128P Series



(DP-32)

HM658128FP Series



(FP-32D)

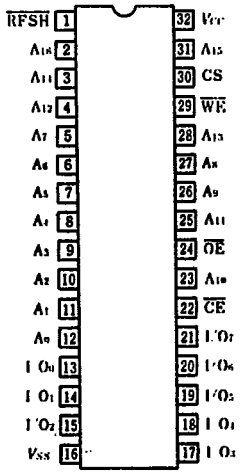
■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time
    - $\overline{CE}$ Access Time . . . 100/120/150ns
  - Cycle Time
    - Random Read/Write Cycle Time . . . 180/210/250ns
- Low Power . . . 200mW typ. (Active)
  - 0.5mW (standby) (L-version)
- All inputs and outputs TTL compatible
- Non Multiplexed Address
- 512 Refresh Cycles (8ms)
- Refresh Functions
  - Address Refresh
  - Automatic Refresh
  - Self Refresh

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM658128P-10	100ns	600 mil 32 pin Plastic DIP
HM658128P-12	120ns	
HM658128P-15	150ns	
HM658128LP-10	100ns	
HM658128LP-12	120ns	
HM658128LP-15	150ns	
HM658128FP-10	100ns	32 pin Plastic SOP
HM658128FP-12	120ns	
HM658128FP-15	150ns	
HM658128LFP-10	100ns	
HM658128LFP-12	120ns	
HM658128LFP-15	150ns	

■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

Symbol	Pin Name
A0 – A16	Address Inputs
I/O – I/O7	Data Input/Output
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
CS	Chip Select
V_{CC}	Power Supply
V_{SS}	Ground

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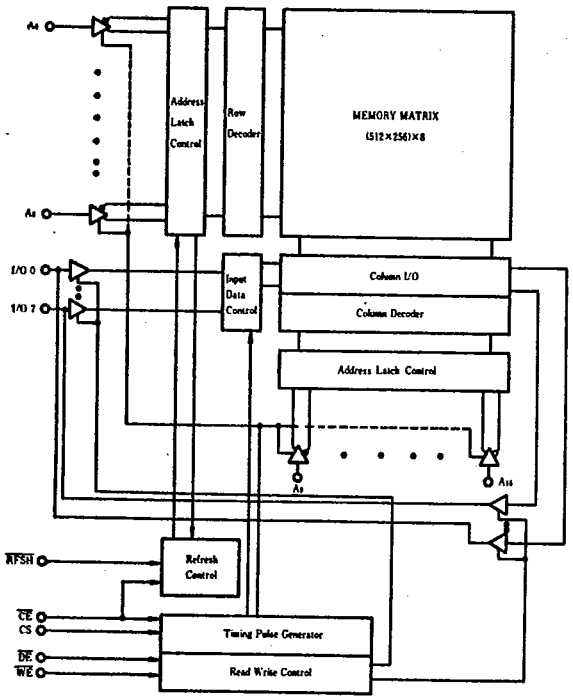
■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	CS at $\overline{CE}$ going Low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X	L	H	Low Z	Read
L	H	X	X	L	High Z	Write
L	H	X	H	H	High Z	–
L	L	X	X	X	High Z	CS Standby
H	X	L	X	X	High Z	Refresh
H	X	H	X	X	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−1.0	–	0.8	V

■ DC CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0 t_{cyc} = min.	–	40	75	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}	–	1	2	mA
Standby Power Supply Current	I_{SB2} *1	$\overline{CE}$ ≥ V_{CC} –0.2V $\overline{RFSH}$ ≥ V_{CC} –0.2V	–	100	200	μA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}	–	1	2	mA
	I_{CC3} *1	$\overline{CE}$ ≥ V_{CC} –0.2V $\overline{RFSH}$ ≤ 0.2V	–	100	200	μA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = V_{SS} to V_{CC}	–10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	–10	–	10	μA
Output Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
	V_{OH}	I_{OH} = –1mA	2.4	–	–	V

Note) *1. This characteristics is guranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	10	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

• AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level ..... V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load ..... 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM658128-10		HM658128-12		HM658128-15		Unit
		min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	180	–	210	–	250	–	ns
Random Read Modify Write Cycle Time	t_{RWC}	240	–	280	–	330	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	ns
Output Enable Access Time	t_{OEA}	–	30	–	40	–	50	ns
Chip Disable to Output in High Z	t_{CHZ}	–	30	–	35	–	40	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	35	–	40	–	ns
Output Disable to Output in HighZ	t_{OHZ}	–	25	–	30	–	35	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Enable Pulse Width	t_{CE}	100n	1μ	120n	1μ	150n	1μ	s
Chip Enable Precharge Time	t_P	70	–	80	–	90	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	ns
Address Hold Time	t_{AH}	30	–	35	–	40	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns
$\overline{RFSH}$ Hold Time	t_{RHC}	15	–	15	–	15	–	ns
Refresh Command Delay Time (Standby Mode)	t_{RCD}	–	5	–	5	–	5	ns

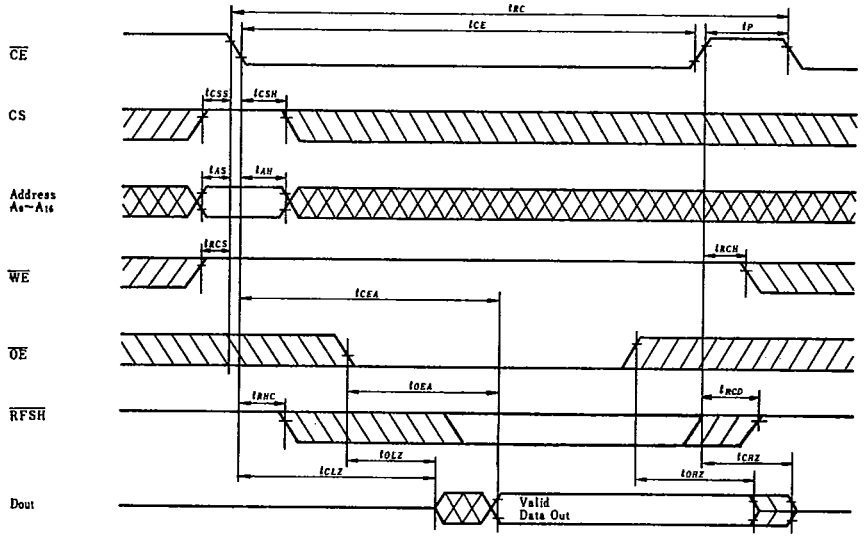
(to be continued)

Item	Symbol	HM658128-10		HM658128-12		HM658128-15		Unit
		min.	max.	min.	max.	min.	max.	
Chip Select Set-up Time	t_{CSS}	0	–	0	–	0	–	ns
Chip Select Hold Time	t_{CSH}	30	–	35	–	40	–	ns
Write Command Pulse Width	t_{WP}	30	–	35	–	40	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	ns
Data In to End of Write	t_{DW}	25	–	30	–	35	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	70	–	80	–	90	–	ns
Refresh Precharge Time	t_{FP}	40	–	40	–	40	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80n	8μ	80n	8μ	80n	8μ	s
Automatic Refresh Cycle Time	t_{FC}	180	–	210	–	250	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	8	–	8	–	8	–	μs
Refresh Reset Time for Self Refresh	t_{RFS}	180	–	210	–	250	–	ns
Refresh Reset Time for Automatic Refresh	t_{RFA}	0	–	0	–	0	–	ns
Refresh Period (512 cycles)	t_{REF}	–	8	–	8	–	8	ns

Notes:
(1) t_{CHZ}, t_{OHZ} and t_{WHZ} define the time at which the output achieves the open circuit conditions under the condition of t_T = 5ns and not 100% tested.
(2) t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T = 5ns and not 100% tested.
(3) A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$. Write end is defined at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.
(8) After Self Refresh, Auto Refresh should be started within 15μs.

■ TIMING WAVEFORMS

● Read Cycle



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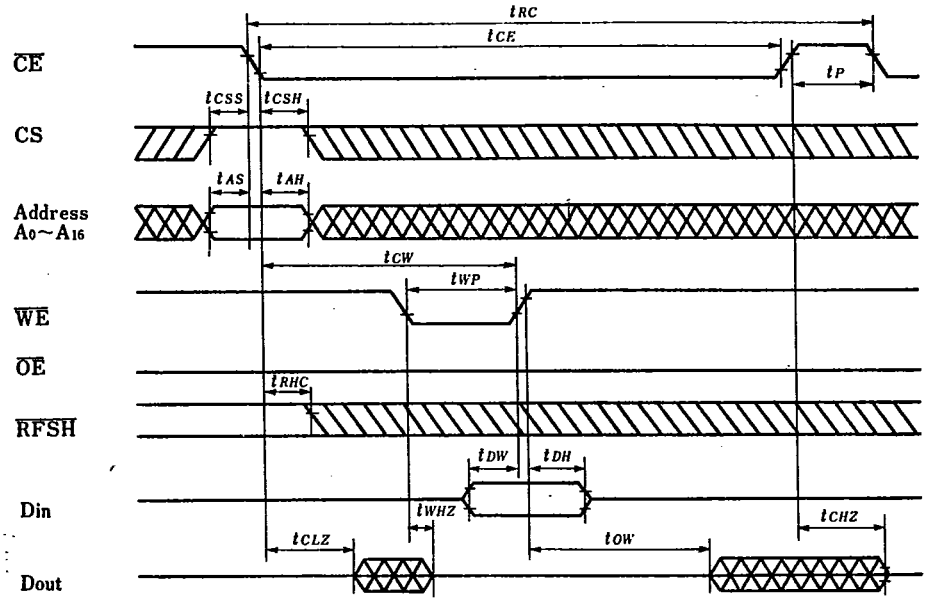
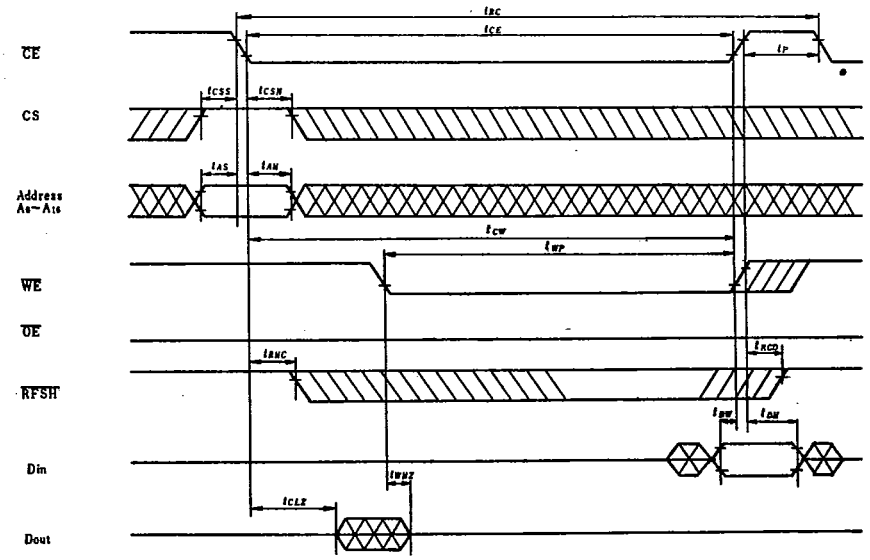
- **Write Cycle-1 ($\overline{OE}$ Clock)**



Write Cycle-2 ($\overline{OE}$ Low Fix)



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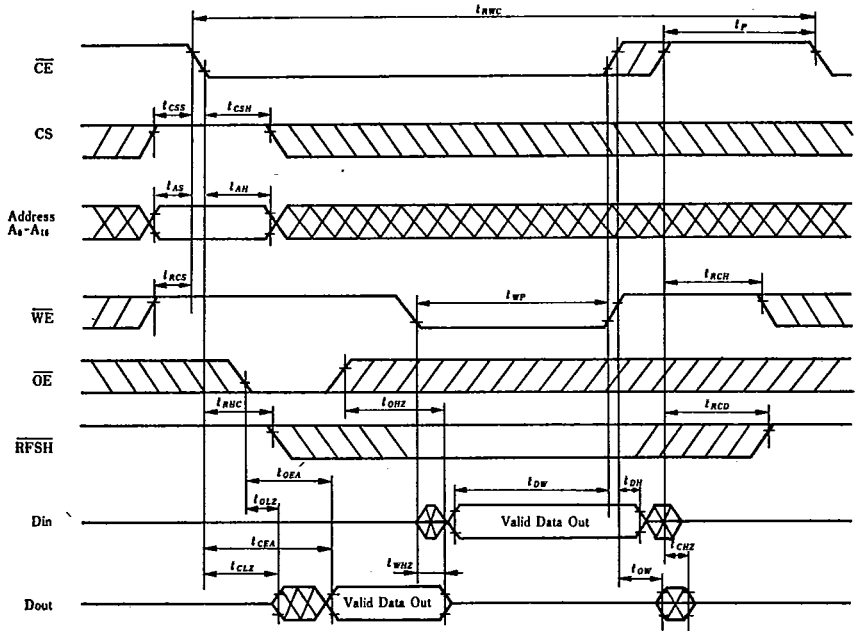
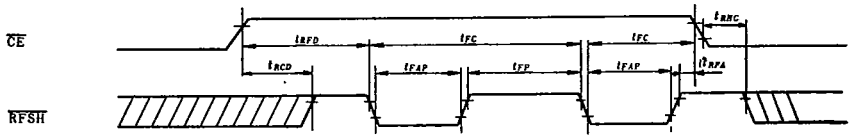
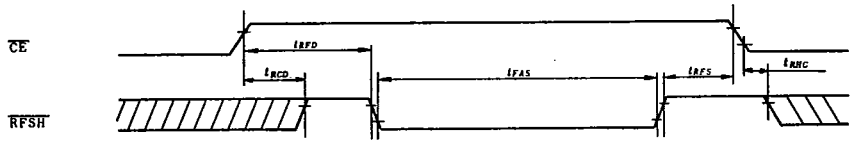
- **Read Modify Write Cycle**



- **Automatic Refresh Cycle**



- **Self Refresh Cycle**



- **CS Standby Mode**