GOULD
AMI Semiconductors

Static CMOS & NMOS Family of ROMs

Features

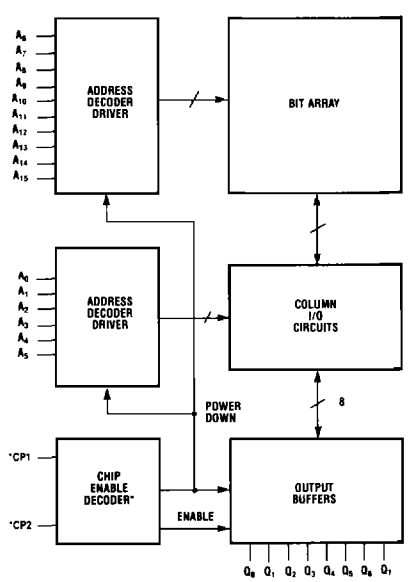
- 16K, 32K, 64K, 128K, 256K, 512K, 1M, 2M, 4M Selections
- Fast Access Time
- Mate With State-Of-The-Art 32 Bit Microprocessors
- Low Standby Power CMOS
- Fully Static Operation
- Single +5V ±10% Power Supply
- Directly TTL Compatible For Clean Interface
- Three-State TTL Compatible Outputs
- EPROM Pin Compatible
- Late Mask Programmable For Quick Turn Times
- Programmable Control Pins

General Description

The Gould AMI family of ROMs are static mask programmable and organized by 8 bits. The device is fully TTL compatible on all inputs and outputs and uses a single +5V power supply. There are no requirements for clocks or refreshing, because they are static in operation. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices. The control pin function and active level, as well as the memory contents, are user-defined.

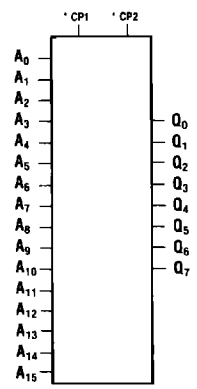
(512K Example)

Block Diagram



* THE USER DECIDES BETWEEN AN OE OR CE FUNCTION AND THE ACTIVE LEVEL FOR THE CP PINS

Logic Symbol



Pin Names

A_0-A_{15}	Address Inputs
Q_0-Q_7	Data Outputs
CP1/CP2	Output Enable/Chip Enable
V_{CC}; GND; NC	5V; Ground; No Contact

ROM Family

Table 1.

Device Name	S6316	S6333/S63332	S63364	S6364	S23128
Process	CMOS	CMOS	CMOS	CMOS	NMOS
Capacity	16K	32K	64K	64K	128K
Organization	2K x 8	4K x 8	8K x 8	8K x 8	16K x 8
Compatible EPROM	2516	2732/2532	68764	2764	27128
Number of Pins	24	24 (A)/24 (B)	24	28	28
Plastic Dip Package Available	YES	YES	YES	YES	YES
Ceramic Dip Package Available	YES	YES	YES	YES	YES
SOIC Plastic Package Available	NO	NO	NO	YES	YES
Temperature Range: C/I/M, 0 to 70ºC/ – 40 to 85ºC/ – 55 to 125ºC	C/I/M	C/I/M	C/I/M	YES C/I/M	NO C/I/M

Electrical Characteristics: V_{CC} = +5V ±10%

Symbol	Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{ol}	Output LOW Voltage (I_{ol} = 3.2mA)	V		0.4		0.4		0.4		0.4		0.4
V_{oh}	Ouput HIGH Voltage	V	2.4		2.4		2.4		2.4		2.4	
I_{oh}	Ouput HIGH Current			– 1.0 mA		– 1.0 mA		– 1.0 mA		– 1.0 mA		– 220 μA
V_{il}	Input LOW Voltage	V	– 0.3	0.8	– 0.3	0.8	– 0.3	0.8	– 0.3	0.8	– 0.5	0.8
V_{ih}	Input HIGH Voltage	V	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.0	V_{CC}
I_{L_I}	Input Leakage Current	μA	– 1	1	– 1	1	– 1	1	– 1	1	– 10	10
I_{L_O}	Output Leakage Current	μA	– 10	10	– 10	10	– 10	10	– 10	10	– 10	10
I_{CC_1}	Power Supply Current—TTL Active	mA	Note 3	40	Note 3	40	Note 3	40	Note 3	40	Note 1	80
I_{CC_2}	Power Supply Current—CMOS Active	mA	Note 4	35	Note 4	35	Note 4	35	Note 4	35		
I_{SD_1}	Power Supply Current TTL	mA	Note 5	2	Note 5	2	Note 5	2	Note 5	2	Note 2	20
I_{SD_2}	Power Supply Current CMOS	μA	Note 6	100	Note 6	100	Note 6	100	Note 6	100		
t_{AA}	Address Access Time—Commercial Temp	ns		100/120		100/120		100/120		100/120		250
	Industrial Temp.			150		150		150		150		280
	Mil Temp			175		175		175		175		300
t_{ACE}	Chip Enable Access Time	ns		100/120		100/120		100/120		100/120		250
	Industrial Temp.			150		150		150		150		280
	Mil Temp.			175		175		175		175		300
t_{OE}	Ouput Enable Access Time	ns		70		70		70		70		80
	Industrial Temp.			75		75		75		75		115
	Mil Temp.			80		80		80		80		120
t_{CEO}	Disable Time From Chip Enable	ns	0	50	0	50	0	50	0	50	0	80
	Industrial Temp.		0	65	0	65	0	65	0	65	0	115
	Mil Temp.		0	70	0	70	0	70	0	70	0	120
t_{OEO}	Disable Time From Output Enable (Note 5)	ns	0	50	0	50	0	50	0	50	0	80
	Industrial Temp		0	65	0	65	0	65	0	65	0	115
	Mil Temp.		0	70	0	70	0	70	0	70	0	120
t_{OH}	Output Hold Time	ns	0		0		0		0		0	
	Industrial Temp.		0		0		0		0		0	
	Mil Temp.		0		0		0		0		0	
C_{in}	Input Capacitance (Note 7)	pf		7		7		7		7		7
C_{out}	Output Capacitance (Note 7)	pf		10		10		10		10		10

Notes:
1 NMOS Power Test $V_{cc} = V_{CCmax}$ OE/CE = Active Address inputs @ V_{ih}
2 NMOS Standby Power Test: Same as Note 1 except CE = Deselected
3 TR = 150ns, duty = 100% V_{il} = 0.8v or 2.2v
4 TR = 150ns, duty = 100% V_{il} = Gnd or V_{CC}
5 Chip in Standby Mode $V_{il} = V_{il}$ or V_{ih}
6 Chip in Standby Mode V_{il} = Gnd or V_{CC}
7 Capacitance is measured at TA = 25º C, f = 1MHz V_{in} = 0v, V_{out} = 0v
8 In Notes 1 though 7 the Output Loads are Disconnected

‡ Package under development

Table 1. (continued)

				Preliminary	Preliminary
Device Name	S63256	S63512	S631000/S631001	S632000	S634000
Process	CMOS	CMOS	CMOS	CMOS	CMOS
Capacity	256K	512K	1 Meg	2 Meg	4 Meg
Organization	32K x 8	64K x 8	128K x 8	256K x 8	512K x 8
Compatible EPROM	27256	27512	27011/27010	27210	274001
Number of Pins	28	28	28/32	32	32
Plastic Dip Package Available	YES	YES	YES	YES	YES
Ceramic Dip Package Available	YES	YES (32 pin)	YES	YES	YES
SOIC Plastic Package Available	YES	YES (350 mil)	YES (350 mil)	NO	NO
PLCC Package Available	YES	YES	YES	YES	YES
Temperature Range: C/I/M, 0 to 70ºC/ – 40 to 85ºC/ – 55 to 125ºC	C/I/M	C/I/M‡	C/I/M	C/I/M‡	C/I/M

Electrical Characteristics: V_{CC} = +5V ±10%

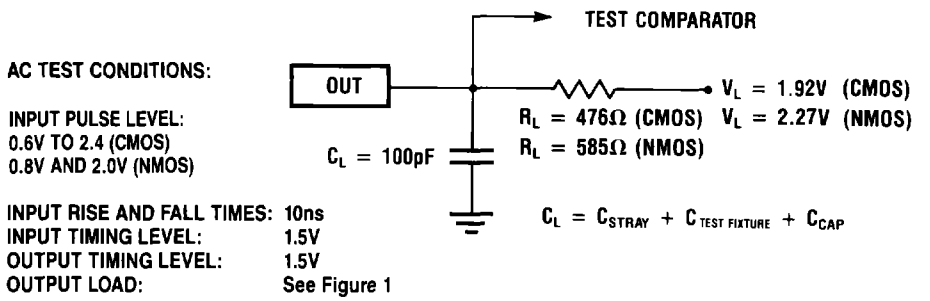
Symbol	Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{ol}	Output LOW Voltage (I_{ol} = 3.2mA)	V		0.4		0.4		0.4		0.4		0.4
V_{oh}	Ouput HIGH Voltage	V	2.4		2.4		2.4		2.4		2.4	
I_{oh}	Ouput HIGH Current			-1.0 mA		-1.0 mA		-1.0 mA		-1.0 mA		-1.0 mA
V_{il}	Input LOW Voltage	V	-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.5	0.8
V_{ih}	Input HIGH Voltage	V	2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	2.2	V_{CC} +0.3
IL_i	Input Leakage Current	µA	-1	1	-1	1	-1	1	-1	1	-1	1
IL_o	Output Leakage Current	µA	-10	10	-10	10	-10	10	-10	10	-10	10
I_{cc_1}	Power Supply Current—TTL Active	mA	Note 3	40	Note 3	40	Note 3	40	Note 3	40	Note 3	40
I_{cc_2}	Power Supply Current—CMOS Active	mA	Note 4	35	Note 4	35	Note 4	35	Note 4	35	Note 4	35
I_{sb_1}	Power Supply Current TTL	mA	Note 5	2	Note 5	2	Note 5	2	Note 5		Note 5	
I_{sb_2}	Power Supply Current CMOS	µA	Note 6	100	Note 6	150	Note 6	150	Note 6	150	Note 6	150
t_{AA}	Address Access Time—Commercial Temp	ns		120/150		150		100/120/150		150/200		150/200
	Industrial Temp.			175		175		120/150		200		200
	Mil Temp.			200		200		150		250		250
t_{ACE}	Chip Enable Access Time	ns		120/150		150		100/120/150		150/200		150/200
	Industrial Temp.			175		175		120/150		200		200
	Mil Temp.			200		200		150		250		250
t_{OE}	Ouput Enable Access Time	ns		70		80		80		70/80		70/80
	Industrial Temp.			75		85		90		85		85
	Mil Temp			80		90		100		90		90
t_{CEO}	Disable Time From Chip Enable	ns	0	50	0	60	0	70	0	60	0	60
	Industrial Temp		0	65	0	75	0	80	0	75	0	75
	Mil Temp		0	70	0	80	0	90	0	80	0	80
t_{OEO}	Disable Time From Output Enable (Note 5)	ns	0	50	0	60	0	70	0	60	0	60
	Industrial Temp.		0	65	0	75	0	80	0	75	0	75
	Mil Temp		0	70	0	80	0	90	0	80	0	80
t_{OH}	Output Hold Time	ns	0		0		0		0		0	
	Industrial Temp		0		0		0		0		0	
	Mil Temp.		0		0		0		0		0	
C_{in}	Input Capacitance (Note 7)	pf		7		7		5		5		5
C_{out}	Output Capacitance (Note 7)	pf		10		10		5		8		8

Notes:
1 NMOS Power Test $V_{cc} = V_{ccmax}$, OE/CE = Active, Address inputs @ V_{il}
2 NMOS Standby Power Test Same as Note 1 except CE = Deselected
3 TR = 150ns duty = 100% V_i = 0.8v or 2.2v
4 TR = 150ns duty = 100% V_i = Gnd or V_{cc}
5 Chip in Standby Mode, $V_i = V_{il}$ or V_{ih}
6 Chip in Standby Mode. V_i = Gnd or V_{cc}
7 Capacitance is measured at TA = 25º C, f = 1MHz, V_{in} = 0v V_{out} = 0v
8 In Notes 1 though 7 the Output Loads are Disconnected

‡ Package under development

ROM Family

Figure 1



Application of Gould ROMs
All of the ROMs offered by Gould are fully static, asynchronous, non-multiplexed devices. No matter what microprocessor you're using in your system, careful planning will give you the greatest flexibility in using our ever-expanding family of ROMs.

No Clocks Are Required
A clock is *not* required by our ROMs to latch addresses, precharge internal circuitry, or perform any other function. All control lines (CE, or OE) may remain in a valid read state for an indefinite period of time, during which the address inputs may be changed as desired to access various stored data.

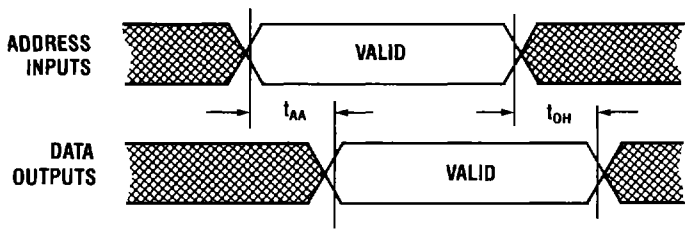
The Address Inputs Must Be Valid for the Entire Cycle
The addresses must be held constant to a Gould ROM until the output data has been placed onto the system data bus and read by the microprocessor or a peripheral device. If the microprocessor is one of several common types using a multiplexed address/data bus, the system design must incorporate latches to extract address information from this bus and supply the latched addresses to our ROM.

Flexibility on Control Pin Programming
You can use the programmable control functions to your best advantage. Let's take the S6364 as an example. If four S6364s are used in a system, pin 22 on each device could be a common OE signal for a master tristate control; pin 20 on each device could be a master powerdown control; and pins 26 and 27 could serve as 1-of-4 addressing to select which of four ROMs is active.

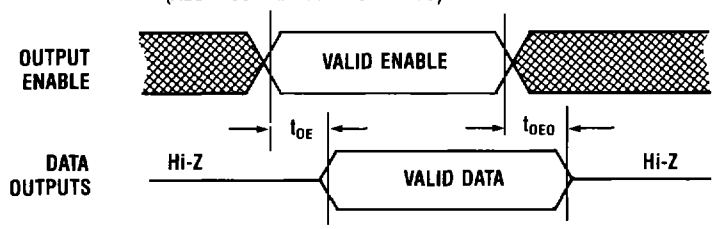
Another possibility would be to use all four control lines on the S6364 as higher order addresses. While the data sheet may show different labels on these pins to conform with common industry practice, all control lines on the S6364 can in reality be programmed with equal flexibility. Taking advantage of this, sixteen S6364 devices can be addressed from four control lines. These control lines can be all powerdown, all non-powerdown, or any combination. With this approach, a later system evolution to higher density ROMs means that the correct signals are already in place for both addressing and bus control.

AC Timing Diagram

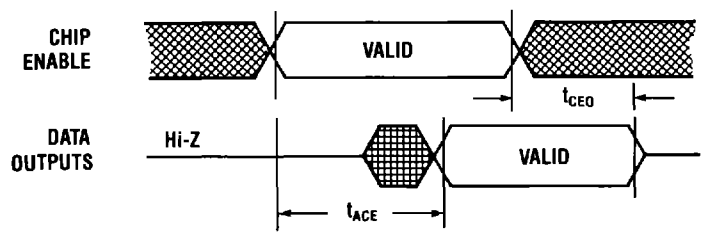
ADDRESS TO OUTPUT DELAY (OUTPUT ENABLED/AND CHIP ENABLE)



OUTPUT ENABLE TO OUTPUT DELAY
(ADDRESS VALID/CHIP ENABLED)



CHIP ENABLE TO OUTPUT DELAY (ADDRESS VALID/OUTPUT ENABLED)



ROM Family

Figure 1. Example of minimum configuration for a Gould ROM and a microprocessor using a non-multiplexed address bus.

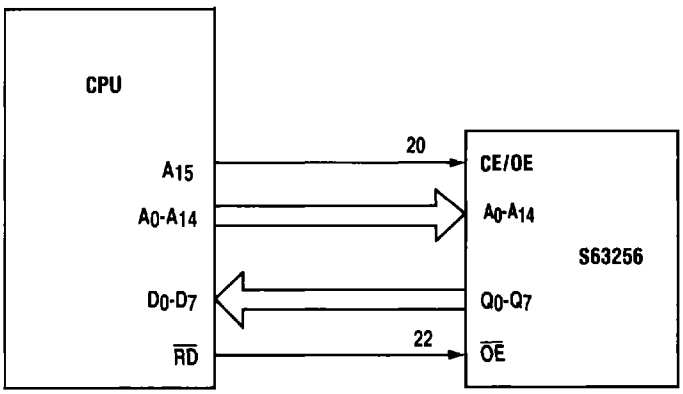
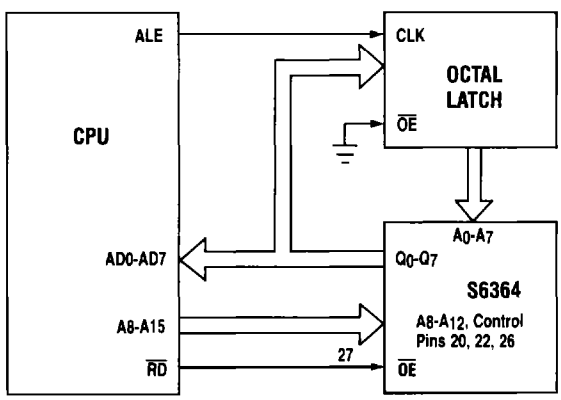


Figure 2. Example of a minimum configuration for a system using a multiplexed address/data bus.



Powerdown or Not: It's Up to You

Finally, you have the option on most of our ROMs to choose whether or not to incorporate powerdown or standby capability. The key is in the control pin programming that you specify when the order is placed. Any pin specified as a Chip Enable, either high or low, can place the device into a powerdown mode as well as place all outputs in a high Z condition. In powerdown or standby, the device draws much less current than in the active mode.

If, instead a pin is programmed as Output Enable, that pin controls only the output mode (active or high Z); device current is relatively constant. All Gould ROMs which provide powerdown capability allow you to choose your own combination of CE and OE. For example, the S23128 can be programmed with three CE functions, or one CE and two OE, etc.

When you are making a decision between CE and OE programming, note that standby current is not the only difference in the two options. Because of the differences in internal circuitry being controlled, a CE pin has relatively long access time, perhaps 150ns, compared to an OE pin, perhaps 80ns. Therefore, system timing requirements must be evaluated when weighing the relative merits of programming for powerdown.

Another item to consider is printed circuit (PC) board layout. A powerdown device has a noticeable change in power supply current when it is switched into the active mode. Careful PC board layout and power supply decoupling will prevent the introduction of noise into your system. This noise is due to the interaction of the change in current and the inherent inductance of PC board wiring traces.

Note that a device whose ouptputs are switched to the active state by an OE pin will not exhibit this change in power supply current, however, power supply decoupling is still necessary.

Table 2. Control Pin Options

AMI ROMs offer you the choice of control line functions as well as the active level. The possible functions and active level for each pin are shown below (a "bar" above the function name means active low).

CE Function = Power Down
OE Funtions = Non Power Down, high Z output control only
DC = Don't Care (Control pins programmed as DC have no effect on either the powerdown mode or high Z control but are still connected to input protection devices.)

2K x 8 (16K) 24 Pin S6316 CMOS
Pins 21-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
18-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

4K x 8 (32K) 24 Pin S6333 CMOS
Pins 20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
18-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

4K x 8 (32K) 24 Pin S63A332 CMOS
Pins 20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
21-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

8K x 8 (64K) 24 Pin S63364 (CMOS)
Pin 20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

8K x 8 (64K) 28 Pin S6364 CMOS
Pins 27-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
26-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

16K x 8 (128K) 28 Pins S23128 NMOS
Pins 27-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

32K x 8 (256K) 28 Pin S63256 CMOS
Pins 22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

64K x 8 (512K) 28 Pin S63512 CMOS
Pins 22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

128K x 8 (1 MEG) 28 Pin S631000 CMOS
Pin 20-OE, $\overline{OE}$, $\overline{CE}$

128K x 8 (1 MEG) 32 Pin S631001 CMOS
Pins 24-$\overline{OE}$
22-$\overline{CE}$

256K x 8 (2 MEG) 32 Pin S632000 CMOS
Pins 31-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
24-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

512K x 8 (4 MEG) 32 Pin S634000 CMOS
Pins 24-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

Truth Table: (For simplicity, all control functions in the Truth Table are defined as active high).

OE/CE	OE/CE	Outputs	Power
$\overline{CE}$	X	HI-Z	STANDBY
X	$\overline{CE}$	HI-Z	STANDBY
$\overline{OE}$	OE/CE	HI-Z	ACTIVE
OE/CE	$\overline{OE}$	HI-Z	ACTIVE
OE/CE	OE/CE	DATA OUT	ACTIVE

How to Get Your ROMs Fast

ROM Ordering Simplified
The following information should be included in the purchase order when ROM devices are being ordered:

—Part number
—Quantity of prototypes for each pattern (if any)
—Total quantity of each pattern
—Pricing and delivery (quotes can be obtained from any Gould AMI sales office)
—Package type (plastic or ceramic)
—Special marking (if required)
—Access speed
—Required temperature range

ROM Code Data

The preferred method of receiving ROM CODE DATA is by electronic data transmission or in EPROM. For EPROM ROM CODE DATA submission, two EPROMs should be submitted. One is programmed to the desired code and the other is blank. Gould AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees the the EPROM has been properly entered into the Gould AMI computer system. The Gould AMI programmed EPROM is returned to the customer for verification of the ROM data. Unless otherwise requested, Gould AMI will not proceed until the customer has returned the ROM CODE VERIFICATION form.

For electronic data transmission, contact your Gould AMI sales office for details.

Customer Requirements
Upon your approval of the returned EPROM and receipt of your purchase order by Gould, masks are generated for production. Prototypes can be furnished to you upon request. Depending upon the volume required, production shipments are made within six to eight weeks after code approval and receipt of the purchase order. Under the Gould corporate policy, if at any time you wish to cancel your code, you are liable for all work in process (WIP). For additional information on cancellation charges, please contact your local Gould sales office.

Other Programming Requirements
Depending upon the ROM required, you must define the correct pinout options. Programmable pins are either chip enable (CE) high or low, don't care (DC), or output enable (OE) high or low. *If a device pin is designated with a CE function, that pin can put the device into a powerdown condition. If OE function is used for a pin, that pin cannot control powerdown for the device. If a device has all control pins designated with OE functions, it is a non-powerdown device.*

If a drawing of your pin configuration is available, it should be provided at the time of EPROM conversion along with any special package marking requirements.

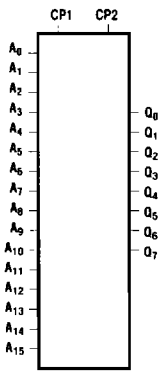
Your Access Time Requirements
As a further guarantee that the correct Gould device type has been specified, the following switching characteristics need to be defined by you when the order is placed.

TAA (Address Access Time)
TACE (Chip Enable Access Time)
TAOE (Output Enable Access Time)

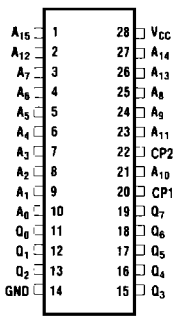
Static CMOS & NMOS Family of ROMs

CP = OE, $\overline{OE}$, CE, $\overline{CE}$, DC

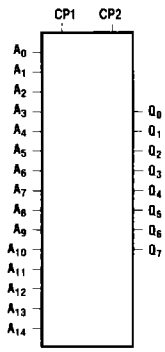
Logic Symbol 512K



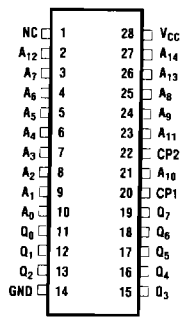
Pin Configuration 512K



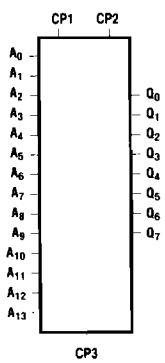
Logic Symbol 256K



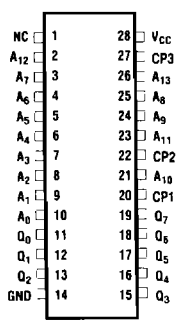
Pin Configuration 256K



Logic Symbol 128K

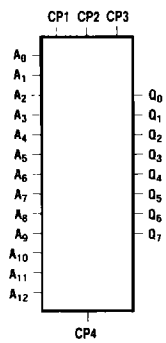


Pin Configuration 128K



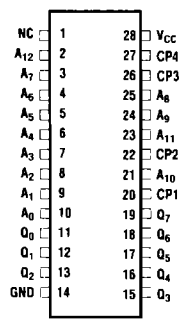
Logic Symbol 64K

28 Pin



Pin Configuration 64K

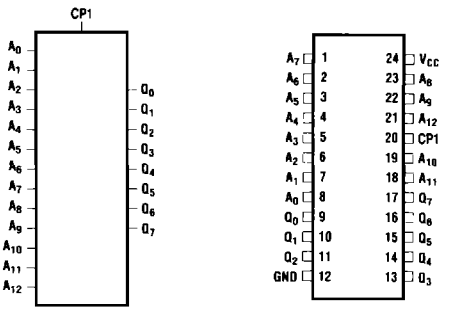
28 Pin



ROM Family

Logic Symbol 64K — Pin Configuration 64K

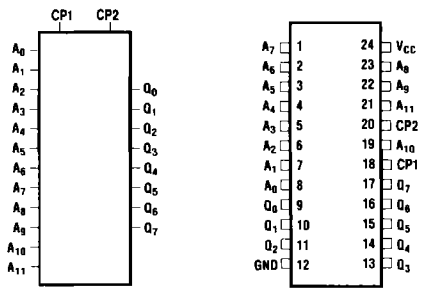
24 Pin



(A)

Logic Symbol 32K — Pin Configuration 32K

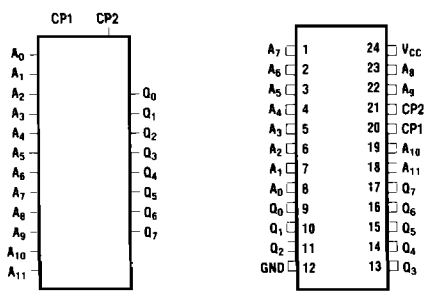
S6333



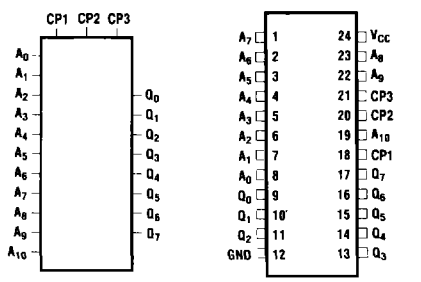
(B)

Logic Symbol 32K — Pin Configuration 32K

S63332



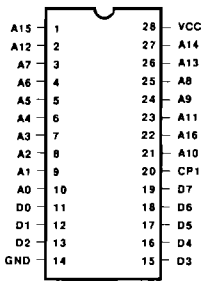
Logic Symbol 16K — Pin Configuration 16K



Static CMOS & NMOS Family of ROMs

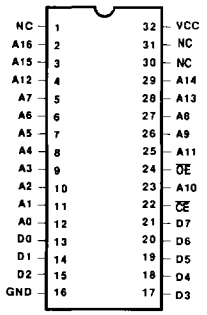
28 Pin P-Dip

S631000



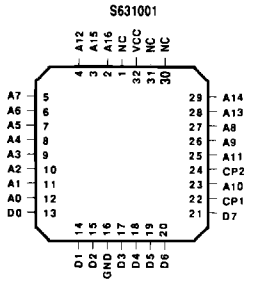
32 Pin P-Dip

S631001



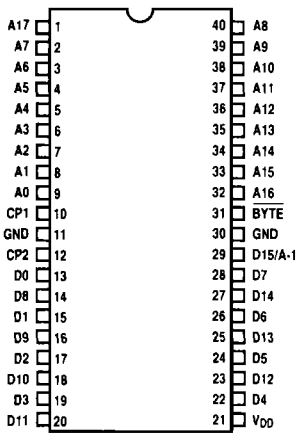
32 Pin PLCC

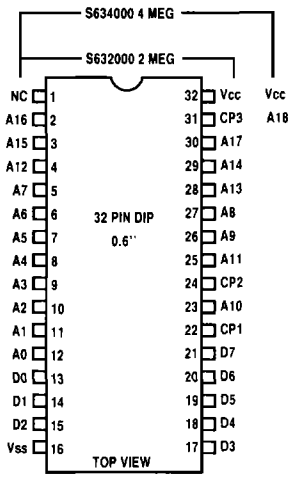
S631001



4 MEG (x16) 40 Pin P Dip

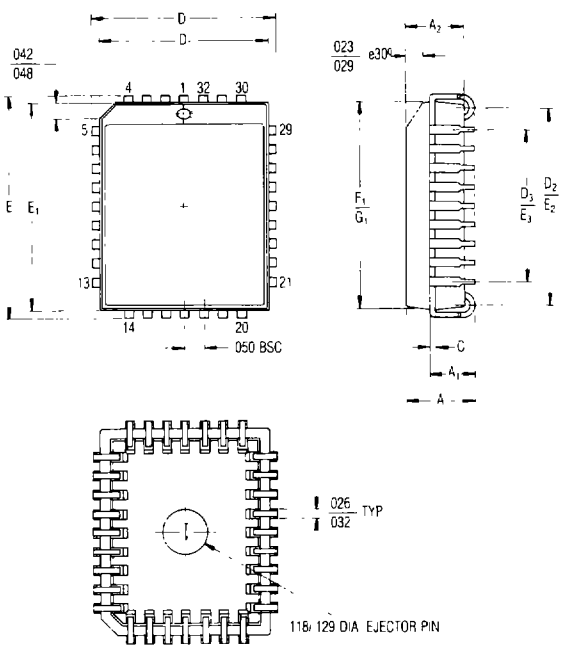
PIN CONNECTION (TOP VIEW)





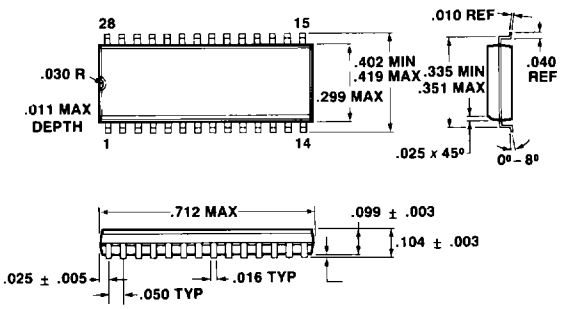
ROM Family

PLCC Outline

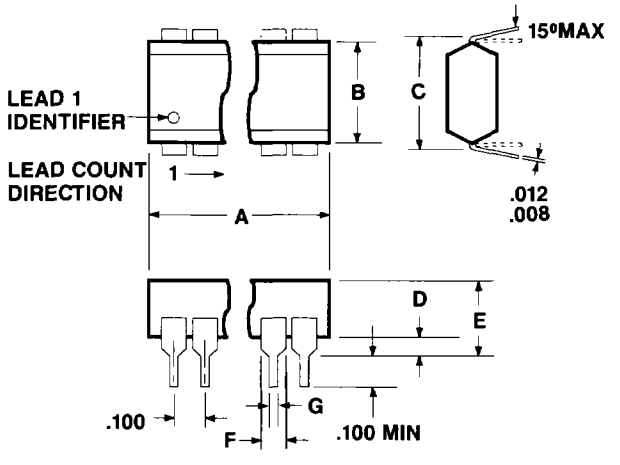


	DIMENSIONS (INCHES)			NOTE
	MIN.	NOM.	MAX.	
A	123	130	140	
A_1	078	085	095	
A_2	106	109	112	
D	485	490	495	
D_1	449	451	453	3
D_2	390	420	430	2
D_3		300 REF		
E	585	590	595	
E_1	549	.551	553	3
E_2	490	520	530	2
E_3		400 REF		
F_1	441	443	445	9
G_1	541	543	545	9
N		32		5
N_D		7		
N_E		9		
C	0097	0100	0103	

28-Lead SOIC Outline

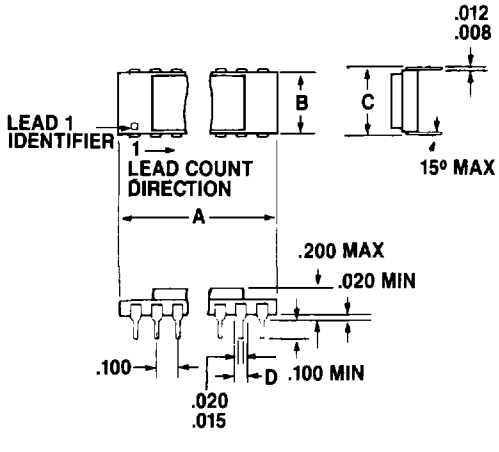


PDIP Outline



SYM	DIMENSIONS			
	LEAD COUNT			
	24	28	32	40
A	1.270 MAX	1.470 MAX	1.655 MAX	2.065 MAX
B	.560 .520	.560 .520	.560 .520	.560 .520
C	.610 .580	.610 .580	.610 .580	.610 .580
D	.020 MIN	.020 MIN	.020 MIN	.020 MIN
E	.200 MAX	.200 MAX	.200 MAX	.200 MAX
F	.070 .050	.070 .050	.040 .060	.060 .040
G	.020 .015	.020 .015	.020 .015	.020 .015

Ceramic Side Braze Outline



SYM	Dimensions	
	Lead Count	
	24	28
A	1.310 MAX	1.450 MAX
B	.598 .575	.598 .575
C	.620 .590	.620 .590
D	.065 .040	.065 .040

ROM Family