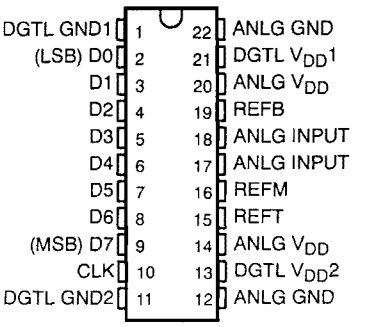
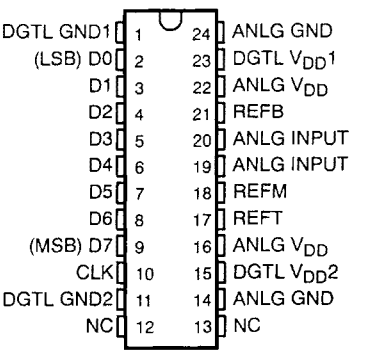
D3739, FEBRUARY 1991–REVISED NOVEMBER 1991

- **LinEPIC™ 1-μm CMOS Process**
- **8-Bit Resolution**
- **Differential Linearity Error . . . ±0.4% Max**
- **Maximum Conversion Rate . . . 25 MHz Typ**
  . . . 20 MHz Min
- **Analog Input Voltage Range . . . 3 V to V_{DD}**
- **TTL Digital I/O Level**
- **Low Power Consumption . . . 190 mW Typ**
- **5-V Single-Supply Operation**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TLC5503-2 is a low-power ultra-high-speed video-band 8-bit analog-to-digital converter manufactured using the LinEPIC™ CMOS process. It uses full-parallel comparison (flash method) for high-speed conversion of a wide-band analog signal (such as a video signal) to a digital signal at a sampling rate of dc to 25 MHz. Its high-speed capability makes the TLC5503-2 suitable for digital video applications such as digital TV, video processing with a computer, or radar signal processing.

Separate analog and digital supply pins are provided to reduce coupling between the high-speed digital switching sections and the lower-frequency analog signal comparators. This pin partitioning minimizes crosstalk and spurious signals. The two analog inputs (pins 17 and 18 on the N package; pins 19 and 20 on the DW package) should be connected together externally. The REFM input (pin 16 on the N package; pin 18 on the DW package) can be used to adjust for small tolerances in the resistor voltage divider by applying an external midpoint voltage.

The TLC5503-2 is characterized for operation from 0°C to 70°C.

During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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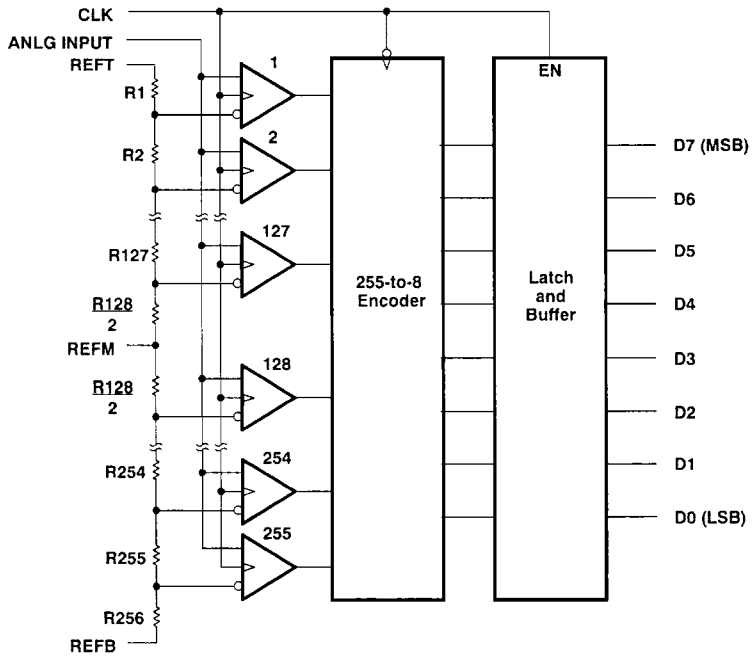
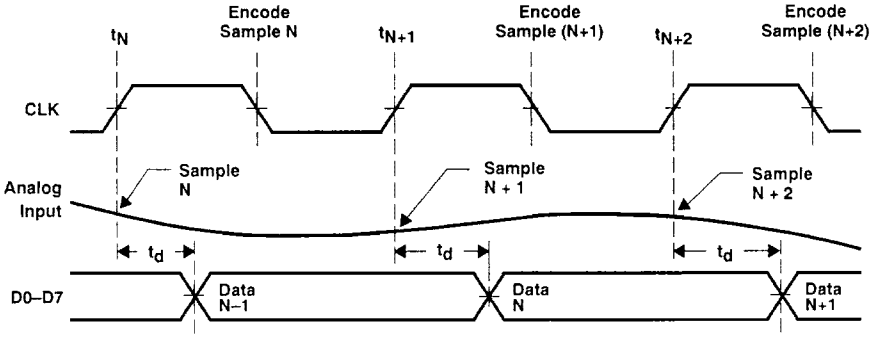
functional block diagram

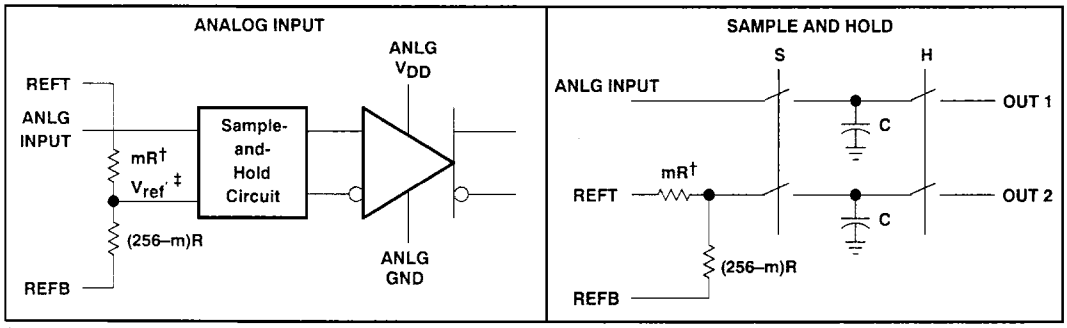


operating sequence



Following the operating sequence above, the rising edge of the clock samples the analog input (sample N) at time t_N and latches sample N−1 at the output (with a delay t_d). Sample N is encoded to eight digital lines on the next falling edge of the clock and then the following high clock level latches these eight bits to the outputs (with a delay t_d) and acquires sample N + 1. Conversion is completed in one clock cycle and continues the sequence for the next cycle.

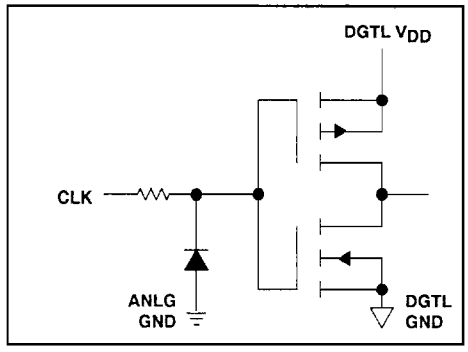
equivalents of analog input circuit



† m = comparator position along the resistor string.

‡ $V_{ref}' = [V_{refT} - V_{refB}] \left[1 - \frac{M}{256}\right] + V_{refB}$

equivalent of digital input circuit



FUNCTION TABLE

STEP	analog input VOLTAGE†	DIGITAL OUTPUT CODE
0	2.960 V	L L L L L L L L
1	2.968 V	L L L L L L L H
. . .	. . .	. . .
127	3.976 V	L H H H H H H H
128	3.984 V	H L L L L L L L
129	3.992 V	H L L L L L L H
. . .	. . .	. . .
254	4.992 V	H H H H H H H L
255	5.000 V	H H H H H H H H

† These values are based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 2.964 V and the transition to full scale (V_{FT}) is 4.996 V . 1 LSB = 8 mV.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, ANLG V_{DD} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range, DGTL V_{DD} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at CLK, V_I ..... −0.3 V to DGTL V_{DD} + 0.3 V
Input voltage range at analog input, V_I ..... −0.5 V to ANLG V_{DD} + 0.5 V
Analog reference voltage range, V_{ref} ..... −0.5 V to ANLG V_{DD} + 0.5 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltages at analog inputs and ANLG V_{DD} are with respect to the ANLG GND terminals. Voltages at the digital outputs and DGTL V_{DD} are with respect to the DGTL GND terminals.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, ANLG V_{DD}	4.75	5	5.25	V
Supply voltage, DGTL V_{DD}	4.75	5	5.25	V
High-level input voltage, V_{IH}, CLK	2			V
Low-level input voltage, V_{IL}, CLK			0.8	V
Input voltage at analog input, V_I	3		5	V
Analog reference voltage (top side), V_{refT}		ANLG V_{DD}		V
Analog reference voltage (midpoint), V_{refM}		$\frac{V_{refT} - V_{refB}}{2}$		V
Analog reference voltage (bottom side), V_{refB}	2.5	3		V
Differential reference voltage, $V_{refT} - V_{refB}$		2		V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			4	mA
Clock pulse duration, high-level or low-level, t_{wH} or t_{wL}	25			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating supply voltage range, T_A = 25°C

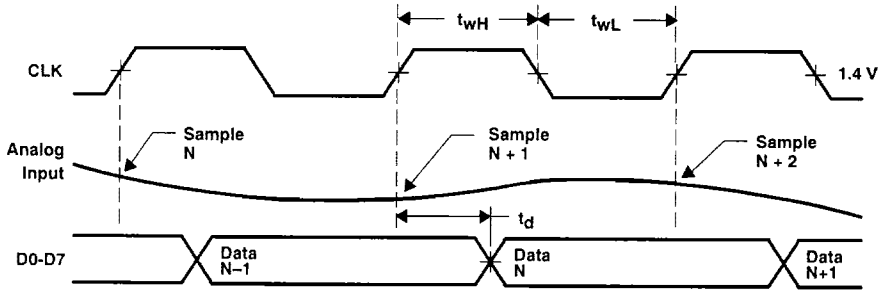
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 µA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_I	Analog input current	V_I = 3 to 5 V, f_{clock} = 15 MHz		±0.3		mA
I_{IH}	Digitial high-level input current	V_I = 5 V			1	µA
I_{IL}	Digital low-level input current	V_I = 0			−1	µA
I_{refB}	Reference current	V_{refB} = 3 V		−12	−20	mA
I_{refT}	Reference current	V_{refT} = 5 V		12	20	mA
C_i	Analog input capacitance			50		pF
I_{DD}	Supply current	f_{clock} = 15 MHz		37	60	mA

operating characteristics over operating supply voltage range, T_A = 25°C

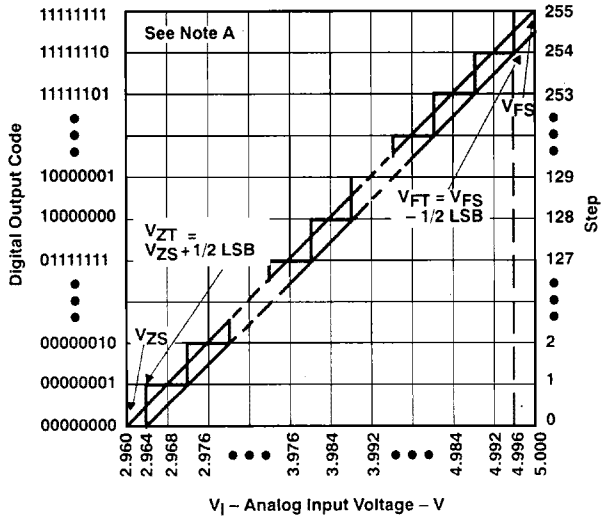
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum conversion rate		20	25		MHz‡
E_D	Linearity error, differential	V_I = 3 V to 5 V, f_{clock} = 15 MHz			±0.4	%FSR
E_L	Linearity error, best straight line	V_I = 3 V to 5 V, f_{clock} = 15 MHz			±0.4	%FSR
G_{diff}	Differential gain	NTSC 40-IRE modulated ramp, f_{clock} = 14.4 MHz		0.9%		
ϕ_{diff}	Differential phase			0.6°		
SNR†	Signal to noise ratio	f_{clock} = 16.4 MHz, f_{IN} = 1.248 MHz (90% P-P), BW = 8.2 MHz		48		dB
THD	Total harmonic distortion			−50		dB
t_d	Digital output dalay time	C_L = 15 pF		10	30	ns

† SNR does not include THD.
‡ No missing codes.

timing diagram



TYPICAL CHARACTERISTICS



NOTE A: This curve is based on the assumption that V_{refB} and V_{refT} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 2.964 V and the transition to full scale (V_{FT}) is 4.996 V. 1 LSB = 8 mV.

Figure 1. Ideal Conversion Characteristics

SUPPLY CURRENT
vs
OPERATING FREE-AIR TEMPERATURE

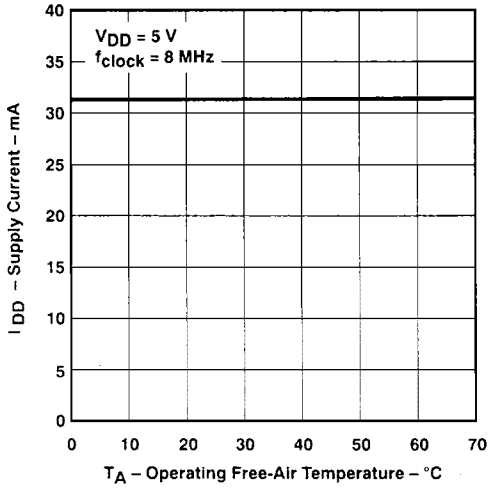


Figure 2

REFERENCE CURRENT
vs
OPERATING FREE-AIR TEMPERATURE

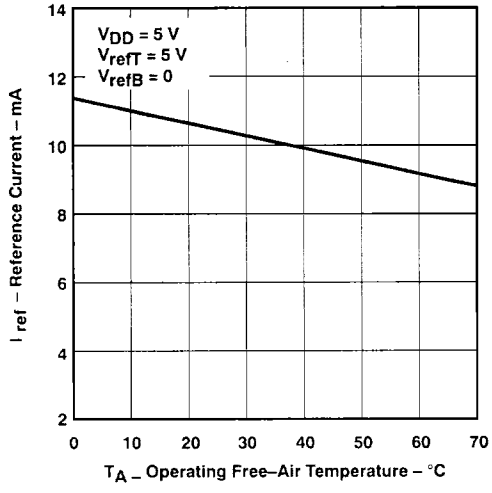


Figure 3

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
OPERATING FREE-AIR TEMPERATURE

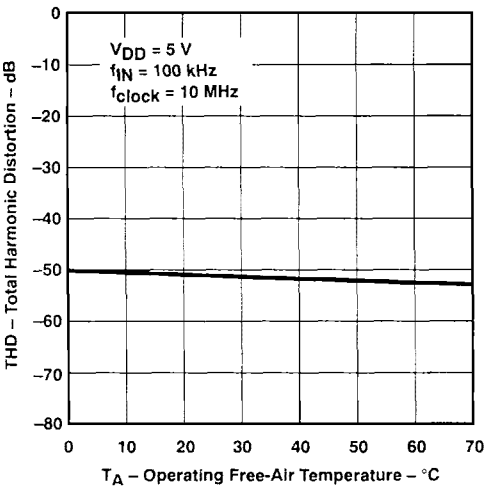


Figure 4

TOTAL HARMONIC DISTORTION
vs
OPERATING FREE-AIR TEMPERATURE

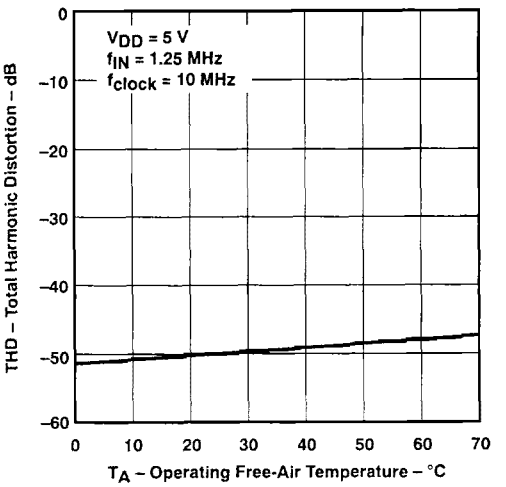


Figure 5

DIFFERENTIAL LINEARITY ERROR
vs
SUPPLY VOLTAGE

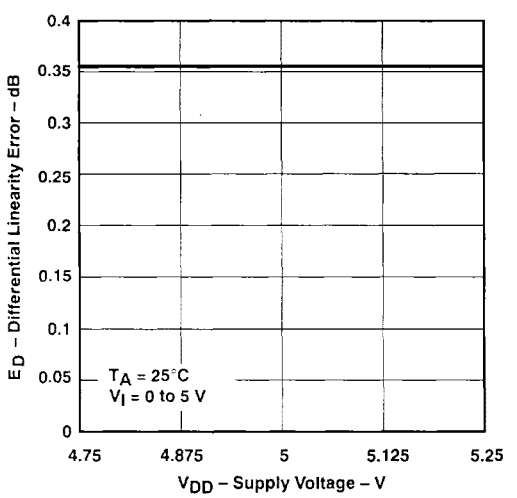


Figure 6

DIFFERENTIAL LINEARITY ERROR
vs
OPERATING FREE-AIR TEMPERATURE

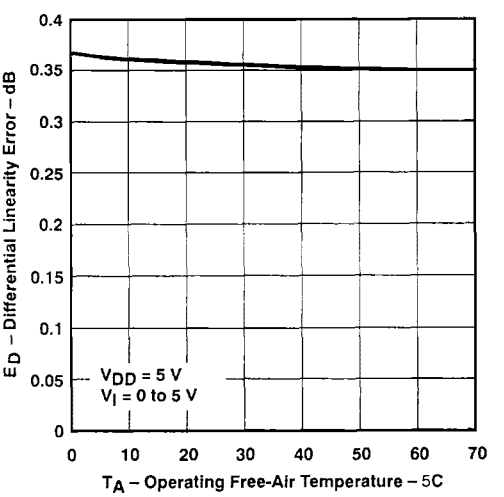


Figure 7

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
SUPPLY VOLTAGE

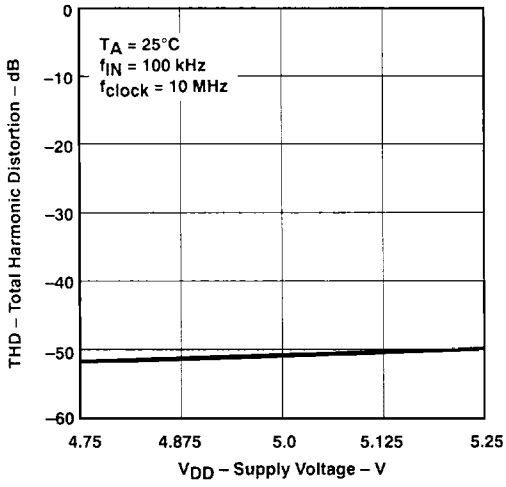


Figure 8

TOTAL HARMONIC DISTORTION
vs
SUPPLY VOLTAGE

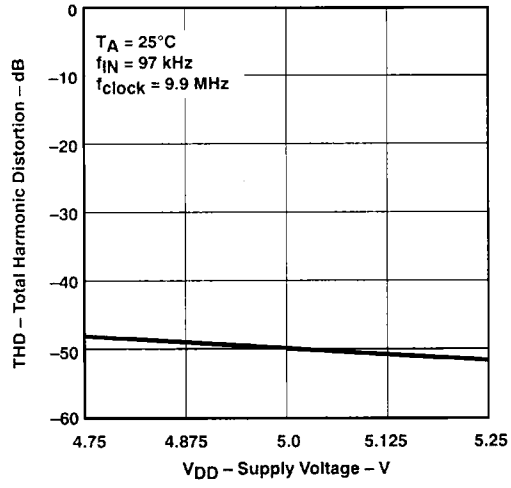


Figure 9

PARAMETER MEASUREMENT INFORMATION

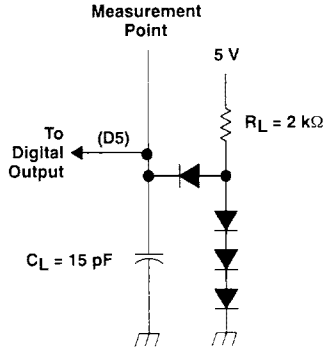


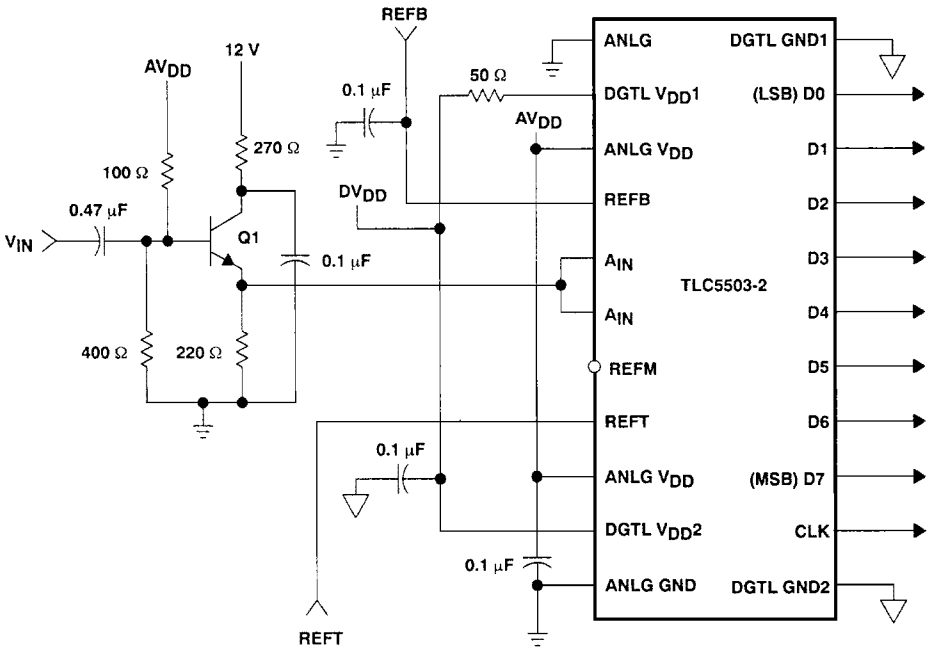
Figure 10. Load Circuit

APPLICATION INFORMATION

The following design recommendations will benefit the TLC5503-2 user:

1. External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
2. RF breadboarding or PCB techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
3. Since the ANLG GND, DGTL GND1, and DGTL GND2 are not connected internally, these pins need to be connected externally. With breadboards, these ground lines should be connected through separate leads with proper supply bypassing. A good method to use is separate twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts.
4. Since the ANLG V_{DD}, DGTL $V_{DD}1$, and DGTL $V_{DD}2$, are not connected internally, these pins also need to be connected externally. To connection ANLG V_{DD} to DGTL $V_{DD}1$ or DGTL $V_{DD}2$, a 50-Ω resistor should be placed in series with the DGTL $V_{DD}1$ pin and then a 0.1-μF capacitor to ground before being connected to the ANLG V_{DD}, and DGTL $DV_{DD}2$ supply.
5. ANLG V_{DD} to ANLG GND, DGTL $V_{DD}1$ to DGTL GND1, and DGTL $V_{DD}2$ to DGTL GND2 should be decoupled with 1-μF and 0.01-μF capacitors, respectively, as close as possible to the appropriate device pins. A ceramic chip capacitor is recommended for the 0.01-μF capacitor. Care should be exercised to assure a solid noise-free ground connection for the analog and digital grounds.
6. The no connection (NC) pins on the small-outline package should be connected to ground.
7. ANLG V_{DD}, ANLG GND, and the ANLG INPUT pins should be shielded from the higher-frequency pins, CLK and D0-D7. If possible, ANLG GND traces should be placed on both sides of the ANLG INPUT traces on the PCB.
8. In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

APPLICATION INFORMATION



NOTES: A. All resistors are 1/4 W carbon.
B. Q1 is 2N3414 or equivalent.
C. All capacitors are ceramic with as short leads as possible.