## DATA SHEET

# μ**PD784927, 784928, 784927Υ, 784928Υ**

## **16-BIT SINGLE-CHIP MICROCONTROLLER**

#### DESCRIPTION

EC

The  $\mu$ PD784927 and 784928 are members of the NEC 78K/IV Series of microcontrollers equipped with a high-speed, high-performance 16-bit CPU for VCR software servo control.

The  $\mu$ PD784927Y and 784928Y are based on the  $\mu$ PD784928 with the addition of an I<sup>2</sup>C bus interface compatible with multi-master.

They contain many peripheral hardware units ideal for VCR control, such as a multi-function timer unit (super timer unit) for software servo control and VCR analog circuits.

Flash memory models, the  $\mu$ PD78F4928 and  $\mu$ PD78F4928Y, are under development.

The functions of the  $\mu$ PD784927 is described in detail in the following User's Manual. Be sure to read this manual before designing your system.

$\mu$ PD784928, 784928Y Subseries User's Manual - Hardware	: U12648E
78K/IV Series User's Manual - Instruction	: U10905E

#### FEATURES

- High instruction execution speed realized by 16-bit CPU core
  - Minimum instruction execution time: 250 ns (with 8 MHz internal clock)
- High internal memory capacity

Item Part Number	μPD784927, 784927Υ	μPD784928, 784928Υ
Internal ROM capacity	96K bytes	128K bytes
Internal RAM capacity	2048 bytes	3584 bytes

• VCR analog circuits conforming to VHS Standard

- CTL amplifier
- DFG amplifierDPG amplifier
- Reel FG comparator (2 channels)
- CSYNC comparator
- CFG amplifier
   DPFG separation circuit (ternary separation circuit)
- Timer unit (super timer unit) for servo control
- Serial interface : 3 channels

RECCTL driver (rewritable)

- 3-wire serial I/O : 2 channels
- I<sup>2</sup>C bus interface: 1 channel
- A/D converter: 12 channels (conversion time: 10 μs)
- Low-frequency oscillation mode: main system clock frequency = internal clock frequency
- Low-power consumption mode: CPU can operate with a subsystem clock.
- Supply voltage range: VDD = +2.7 to 5.5 V
- Hardware watch function: watch operation at low voltage (VDD = 2.7 V (MIN.)) and low current consumption

Unless otherwise specified, the  $\mu$ PD784927 is treated as the representative model throughout this document.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version. Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

#### **APPLICATION FIELDS**

Stationary VCR, video camera, In-TV VCR

#### **\*** ORDERING INFORMATION

#### (1) $\mu$ PD784928 subseries

Part Number	Package
μPD784927GC-×××-8EU <sup>Note</sup>	100-pin plastic LQFP (fine pitch) (14 $\times$ 14 mm)
μPD784927GF-×××-3BA	100-pin plastic QFP (14 $ imes$ 20 mm)
$\mu$ PD784928GC- $\times$ ×-8EU <sup>Note</sup>	100-pin plastic LQFP (fine pitch) (14 $\times$ 14 mm)
μPD784928GF-×××-3BA	100-pin plastic QFP (14 $ imes$ 20 mm)
μPD784927GF-×××-3BA-A	100-pin plastic QFP (14 $ imes$ 20 mm)
μPD784928GF-×××-3BA-A	100-pin plastic QFP (14 $ imes$ 20 mm)

#### (2) $\mu$ PD784928Y subseries

Part Number	Package
μPD784927YGC-×××-8EU <sup>Note</sup>	100-pin plastic LQFP (fine pitch) (14 $ imes$ 14 mm)
μPD784927YGF-×××-3BA	100-pin plastic QFP (14 $\times$ 20 mm)
μPD784928YGC-×××-8EU <sup>Note</sup>	100-pin plastic LQFP (fine pitch) (14 $ imes$ 14 mm)
μPD784928YGF-×××-3BA	100-pin plastic QFP (14 $ imes$ 20 mm)
μPD784927YGF-×××-3BA-A	100-pin plastic QFP (14 $ imes$ 20 mm)
μPD784928YGF-×××-3BA-A	100-pin plastic QFP (14 $ imes$ 20 mm)

Note Under development

**Remarks 1.** ××× indicates ROM code suffix.

2. Products that have the part numbers suffixed by "-A" are lead-free products.

#### PRODUCT DEVELOPMENT OF VCR-SERVO MICROCONTROLLERS

The product development of VCR-servo microcontrollers is shown below. Enclosed in a frame are subseries names.

The Y subseries is a collection of products supporting the I<sup>2</sup>C bus.



## FUNCTION LIST (1/2)

Item	Part Number	μPD784927, 784927Υ		ļ	μPD784928, 784928Υ		
Internal RC	OM capacity	96K bytes		128K bytes			
Internal RA	M capacity	2048 bytes		3584 bytes	3584 bytes		
Operating of	clock	16 MHz (internal of Low frequency os Low power consult	16 MHz (internal clock: 8 MHz) Low frequency oscillation mode : 8 MHz (internal clock: 8 MHz)				
Minimum ir tion time	struction execu- 250 ns (with 8 MHz internal clock)						
I/O port		74 { input : 20 I/O : 54	(including 8 ports for L	ED direct drive)			
Real-time of	output port	11 (including one	each for pseudo VsyNG	c, head amplifier sw	itch, and chrominance rotation)		
	Timer/counter	Timer/counter TM0 (16 bits) TM1 (16 bits) FRC (22 bits) TM3 (16 bits) UDC (5 bits) EC (8 bits) FDV (8 bits)	Compare register 3 3  2 1 4 1	Capture register 1 6 1 — —	Remark For HSW signal generation For CEG signal division		
Super timer unit	Capture register	Input signal CFG DFG HSW Vsync CTL TREEL SREEL	Number of bits 22 22 16 22 16 22 16 22 22	Measurable cycle 125 ns to 524 ms 125 ns to 524 ms 1 $\mu$ s to 65.5 ms 125 ns to 524 ms 1 $\mu$ s to 65.5 ms 125 ns to 524 ms 125 ns to 524 ms 125 ns to 524 ms	$\begin{array}{c c} & & \\ \hline \\ \hline$		
	VCR special circuit	<ul> <li>V<sub>SYNC</sub> separation</li> <li>VISS detection</li> <li>Field identification</li> <li>Head amplifier</li> </ul>	on circuit, Hsync separ n, wide aspect detectic tion circuit switch/chrominance r	ation circuit on circuits rotation output circui	it		
	General-purpose timer	Timer           TM2 (16 bits)           TM4 (16 bits)           TM5 (16 bits)	Compare register 1 1 (capture/compare 1	r Capture regis 	ster		
	PWM output	<ul><li>16-bit resolutio</li><li>8-bit resolution</li></ul>	on : 3 channels (carrie : 3 channels (carrie	er frequency: 62.5 kl er frequency: 62.5 kl	Hz) Hz)		
Serial inter	face	<ul> <li>3-wire serial I/O: 2 channels (BUSY/STRB control: 1 channel)</li> <li>I<sup>2</sup>C bus interface: 1 channel (μPD784928Y subseries only)</li> </ul>					
A/D conver	ter	A/D converter 8-bit resolution $\times$ 12 channels, conversion time: 10 $\mu$ s					

### FUNCTION LIST (2/2)

Part Number		μPD784927, 784927Υ	μPD784928, 784928Υ	
Item				
Analog circuit       • CTL amplifier         • RECCTL driver (rewritable)         • DFG amplifier, DPG amplifier, CFG amplifier         • DPFG separation circuit (ternary separation circuit)         • Reel FG comparator (2 channels)         • CSYNC comparator			r circuit)	
Interrupt sources		4 levels (programmable), vectored interrupt, macro service, context switching		
	External	9 (including NMI)		
Internal		22 (including software interrupt) 23 (including software interrupt)		
Standby function		HALT mode/STOP mode/low power consumption mode/low power consumption HALT mode		
		STOP mode can be released by input of valid edge of NMI pin, watch interrupt (INTW), or INTP1/INTP2/KEY0-KEY4 pins		
Watch function		0.5-second measurement, low-voltage operati	on (V <sub>DD</sub> = 2.7 V)	
Buzzer output function		1.95 kHz, 3.91 kHz, 7.81 kHz, 15.6 kHz (Internal clock: 8 MHz) 2.048 kHz, 4.096 kHz, 32.768 kHz (Subsystem clock: 32.768 kHz)		
Supply voltage V <sub>DD</sub> = +2.7 to 5.5 V				
Package		<ul> <li>100-pin plastic LQFP (fine pitch)(14 × 14 mm)<sup>Note</sup></li> <li>100-pin plastic QFP (14 × 20 mm)</li> </ul>		

Note Under development

\*

#### **PIN CONFIGURATION (Top View)**

• 100-pin plastic LQFP (fine pitch)( $14 \times 14$  mm)



Notes 1. Under development

**2.** Pins SCL and SDA are provided for the  $\mu$ PD784928Y subseries only.

Caution Directly connect the IC (Internally Connected) pins to Vss in the normal operation mode.

• 100-pin plastic QFP (14  $\times$  20 mm)



**Note** Pins SCL and SDA are provided for the  $\mu$ PD784928Y subseries only.

Caution Directly connect the IC (Internally Connected) pins to Vss.

ANI0-ANI11	: Analog Input	P20-P23	: Port2
AVDD1, AVDD2	: Analog Power Supply	P30-P37	: Port3
AVSS1, AVSS2	: Analog Ground	P40-P47	: Port4
AVREF	: Analog Reference Voltage	P50-P57	: Port5
BUSY	: Serial Busy	P60-P67	: Port6
BUZ	: Buzzer Output	P70-P77	: Port7
CFGAMPO	: Capstan FG Amplifier Output	P80, P82-P87	: Port8
CFGCPIN	: Capstan FG Capacitor Input	P90-P96	: Port9
CFGIN	: Analog Unit Input	P100-P103	: Port10
CFGMON	: Capstan FG Monitor	P110-P113	: Port11
CLO	: Clock Output	PTO00-PTO02,	
CSYNCIN	: Analog Unit Input	PTO10, PTO11	: Programmable Timer Output
CTLDLY	: Control Delay Input	PWM0-PWM5	: Pulse Width Modulation Output
CTLIN	: CTL Amplifier Input Capacitor	RECCTL+, RECCTL-	: RECCTL Output/PBCLT Input
CTLMON	: CTL Amplifier Monitor	REEL0IN, REEL1IN	: Analog Unit Input
CTLOUT1, CTLOUT2	: CTL Amplifier Output	RESET	: Reset
DFGIN	: Analog Unit Input	ROTC	: Chrominance Rotate Output
DFGMON	: DFG Monitor	SCK1, SCK2	: Serial Clock
DPGIN	: Analog Unit Input	SCL <sup>Note</sup>	: Serial Clock
DPGMON	: DPG Monitor	SDA <sup>Note</sup>	: Serial Data
ENV	: Envelope Input	SI1, SI2	: Serial Input
HASW	: Head Amplifier Switch Output	SO1, SO2	: Serial Output
HWIN	: Hardware Timer External Input	STRB	: Serial Strobe
IC	: Internally Connected	Vdd	: Power Supply
INTP0-INTP3	: Interrupt From Peripherals	VREFC	: Reference Amplifier Capacitor
KEY0-KEY4	: Key Return	Vss	: Ground
NMI	: Nonmaskable Interrupt	X1, X2	: Crystal (Main System Clock)
P00-P07	: Port0	XT1, XT2	: Crystal (Subsystem Clock)

**Note** Pins SCL and SDA are provided for the  $\mu$ PD784928Y subseries only.

#### **INTERNAL BLOCK DIAGRAM**



**Note** Only the  $\mu$ PD784928 subseries supports I<sup>2</sup>C bus interface.

Remark Internal ROM and RAM capacities differ depending on the product.

#### SYSTEM CONFIGURATION EXAMPLE

• Video camera



**Note** Pins SCL and SDA are provided for the  $\mu$ PD784928Y subseries only.

#### Stationary VCR



**Note** Pins SCL and SDA are provided for the  $\mu$ PD784928Y subseries only.

NEC

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#### **\*** 1. DIFFERENCE BETWEEN $\mu$ PD784928 SUBSERIES AND 784928Y SUBSERIES

The  $\mu$ PD78F4928 and 78F4928Y are based on the  $\mu$ PD784927 and 784927Y and are provided with a 128K-byte flash memory instead of a mask ROM.

Table 1-1 shows the differences between the products in the  $\mu$ PD784928 subseries and 784928Y subseries.

Part Number	μPD784927,	μPD784928,	μPD78F4928,
Item	μPD784927Y	$\mu$ PD784928Y	$\mu$ PD78F4928Y
Internal ROM	Mask ROM		Flash memory
	96K bytes	128K bytes	
Internal RAM	2048 bytes	3584 bytes	
Internal memory capacity select register (IMS)	Not provided		Provided
IC pin	Provided		Not provided
VPP pin	Not provided Provided		Provided
Electrical characteristics	Refer to the Data Sheet of each product.		

Table 1-1. Differences between  $\mu$ PD784928 Subseries and 784928Y Subseries

## 2. PIN FUNCTION

#### 2.1 Port Pins

Pin Name	I/O	Shared with:	Function	
P00-P07	I/O	Real-time output port	<ul> <li>8-bit I/O port (port 0).</li> <li>Can be set in input or output mode in 1-bit units.</li> <li>Can be connected with software pull-up resistors.</li> </ul>	
P20	Input	NMI	4-bit I/O port (port 2).	
P21-P23		INTP0-INTP2	Can be connected with a	software pull-up resistors (P22 and P23 only).
P30-P32	I/O	PTO00-PTO02	8-bit I/O port (port 3).	
P33		SI2/BUSY	Can be set in input or	output mode in 1-bit units.
P34		SO2	Can be connected wit	h software pull-up resistors.
P35		SCK2		
P36, P37		PWM1, PWM0		
P40-P47	I/O	_	<ul> <li>8-bit I/O port (port 4).</li> <li>Can be set in input or output mode in 1-bit units.</li> <li>Can be connected with software pull-up resistors.</li> <li>Can directly drive LED.</li> </ul>	
P50-P57	I/O	_	<ul> <li>8-bit I/O port (port 5).</li> <li>Can be set in input or output mode in 1-bit units.</li> <li>Can be connected with software pull-up resistors.</li> </ul>	
P60	I/O	STRB/CLO	8-bit I/O port (port 6).	
P61		SCK1/BUZ	Can be set in input or output mode in 1-bit units.	
P62		SO1	Can be connected with software pull-up resistors.	
P63		SI1		
P64		DFGMON/BUZ		
P65		DPGMON/HWIN		
P66		CFGMON/PWM4		
P67		CTLMON/PWM5		
P70-P77	Input	ANI0-ANI7	8-bit input port (port 7)	
P80	I/O	Real-time	Pseudo Vsync output	7-bit I/O port (port 8).
P82		output port	HASW output	Can be set in input or output mode
P83			ROTC output	in 1-bit units.
P84		PWM2/SDA <sup>Note</sup>		Can be connected with software
P85		PWM3/SCL <sup>Note</sup>		pull-up resistors.
P86		PTO10		
P87		PTO11		
P90	I/O	ENV	7-bit I/O port (port 9).	
P91-P95		KEY0-KEY4	Can be set in input or output mode in 1-bit units.	
P96			Can be connected wit	h software pull-up resistors.
P100	Input	DPGIN	4-bit input port (port 10).	
P101		REEL1IN		
P102		REEL0IN/INTP3		
P103		CSYNCIN		
P110-P113	Input	ANI8-ANI11	4-bit input port (port 11).	

**Note** Pins SCL and SDA are provided for the  $\mu$ PD784928Y subseries only.

#### 2.2 Pins Other Than Port Pins (1/2)

Pin Name	I/O	Shared with:	Function
REELOIN	Input	P102/INTP3	Reel FG input
REEL1IN		P101	
DFGIN		_	Drum FG, PFG input (ternary)
DPGIN		P100	Drum PG input
CFGIN		_	Capstan FG input
CSYNCIN		P103	Composite SYNC input
CFGCPIN		_	CFG comparator input
CFGAMPO	Output	_	CFG amplifier output
PTO00	Output	P30	Programmable timer output of super timer unit
PTO01		P31	
PTO02		P32	
PTO10		P86	
PTO11		P87	
PWM0	Output	P37	PWM output of super timer unit
PWM1		P36	
PWM2		P84/SDA <sup>Note</sup>	
PWM3		P85/SCL <sup>Note</sup>	
PWM4		P66/CFGMON	
PWM5		P67/CTLMON	
HASW	Output	P82	Head amplifier switch signal output
ROTC	Output	P83	Chrominance rotation signal output
ENV	Input	P90	Envelope signal input
SI1	Input	P63	Serial data input (serial interface channel 1)
SO1	Output	P62	Serial data output (serial interface channel 1)
SCK1	I/O	P61/BUZ	Serial clock I/O (serial interface channel 1)
SI2	Input	P33/BUSY	Serial data input (serial interface channel 2)
SO2	Output	P34	Serial data output (serial interface channel 2)
SCK2	I/O	P35	Serial clock I/O (serial interface channel 2)
BUSY	Input	P33/SI2	Serial busy signal input (serial interface channel 2)
STRB	Output	P60/CLO	Serial strobe signal output (serial interface channel 2)
SDA	I/O	P84/PWM2	I <sup>2</sup> C bus data I/O
SCL	I/O	P85/PWM3	I <sup>2</sup> C bus clock I/O
ANIO-ANI7	Analog input	P70-P77	Analog signal input of A/D converter
ANI8-ANI11		P110-P113	
CTLIN	_	_	CTL amplifier input capacitor connection
CTLOUT1	Output	_	CTL amplifier output
CTLOUT2	I/O	_	Logic signal input/CTL amplifier output
RECCTL+, RECCTL-	I/O	_	RECCTL signal output/PBCTL signal input
CTLDLY	_	_	External time constant connection (for RECCTL rewriting)

**Note** Pins SCL and SDA are provided for the  $\mu$ PD784928Y subseries only.

## 2.2 Pins Other Than Port Pins (2/2)

Pin Name	I/O	Shared with:	Function
VREFC	_	_	VREF amplifier AC connection
DFGMON	Output	P64/BUZ	Drum FG signal output
DPGMON		P65/HWIN	Drum PG signal output
CFGMON		P66/PWM4	CFG signal output
CTLMON		P67/PWM5	CTL signal output
NMI	Input	P20	Non-maskable interrupt request input
INTP0-INTP2	Input	P21-P23	External interrupt request input
INTP3	Input	P102/REEL0IN	
KEY0-KEY4	Input	P91-P95	Key input signal input
CLO	Output	P60/STRB	Clock output
BUZ	Output	P61/SCK1	Buzzer output
		P64/DFGMON	
HWIN	Input	P65/DPGMON	External input of hardware watch counter
RESET	Input	_	Reset input
X1	Input	_	Crystal connection for main system clock oscillation
X2	_		
XT1	Input	_	Crystal connection for subsystem clock oscillation.
XT2	_		Crystal connection for watch clock oscillation
AVDD1	_	_	Positive power supply to analog amplifier circuit
AVDD2	_	_	Positive power supply to A/D converter and analog circuits input buffer
AVss1	_	_	GND of analog amplifier circuit
AVss2	_	_	GND of A/D converter and analog circuits input buffer
AVREF	_	_	Reference voltage input to A/D converter
Vdd	_	_	Positive power supply to digital circuits
Vss	_	_	GND of digital circuits
IC	_	_	Internally connected. Directly connect this pin to Vss.

#### 2.3 I/O Circuits of Pins and Processing of Unused Pins

Table 2-1 shows the types of the I/O circuits of the respective pins and processing of the unused pins. Figure 2-1 shows the circuits of the respective types.

Pin	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00-P07	5-A	I/O	Input: Connect to VDD.
			Output: Leave unconnected.
P20/NMI	2	Input	Connect to VDD.
P21/INTP0			Connect to VDD or Vss.
P22/INTP1, P23/INTP2	2-A	]	Connect to VDD.
P30/PTO00-P32/PTO02	5-A	I/O	Input: Connect to VDD.
P33/SI2/BUSY	8-A	]	Output: Leave unconnected.
P34/SO2	5-A	]	
P35/SCK2	8-A	]	
P36/PWM1, P37/PWM0	5-A	]	
P40-P47			
P50-P57			
P60/STRB/CLO			
P61/SCK1/BUZ	8-A	]	
P62/SO1	5-A	]	
P63/SI1	8-A	]	
P64/DFGMON/BUZ	5-A	]	
P65/HWIN/DPGMON	8-A		
P66/PWM4/CFGMON	5-A		
P67/PWM5/CTLMON			
P70/ANI0-P77/ANI7	9	Input	Connect to Vss.
P80	5-A	I/O	Input: Connect to VDD.
P82/HASW			Output: Leave unconnected.
P83/ROTC			
P84/PWM2/SDA <sup>Note</sup>	10-A		
P85/PWM3/SCL <sup>Note</sup>			
P86/PTO10	5-A		
P87/PTO11			
P90/ENV			
P91/KEY0-P95/KEY4	8-A	]	
P96	5-A		

#### Table 2-1. I/O Circuits of Respective Pins and Processing of Unused Pins (1/2)

**Note** Pins SCL and SDA are provided for the  $\mu$ PD784928Y subseries only.

## Table 2-1. I/O Circuits of Respective Pins and Processing of Unused Pins (2/2)

Pin	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P100/DPGIN	—	Input	When ENDRUM = 0 or ENDRUM = 1 and
			SELPGSEPA = 0: Connect to Vss.
P101/REEL1IN			When ENREEL = 0: Connect to Vss.
P102/REEL0IN/INTP3			
P103/CSYNCIN			When ENCSYN = 0: Connect to Vss.
P110/ANI8-P113/ANI11	9	Input	Connect to Vss.
RECCTL+, RECCTL-	_	I/O	When ENCTL = 0 and ENREC = 0: Connect to Vss.
DFGIN	_	Input	When ENDRUM = 0: Connect to Vss.
CFGIN, CFGCPIN			When ENCAP = 0: Connect to Vss.
CTLOUT1	_	Output	Leave unconnected.
CTLOUT2	_	I/O	When ENCTL = 0 and ENCOMP = 0: Connect to Vss.
			When ENCTL = 1: Leave unconnected.
CFGAMPO	_	Output	Leave unconnected.
CTLIN	_	_	When ENCTL = 0: Leave unconnected.
VREFC			When ENCTL = 0 and ENCAP = 0 and ENCOMP = 0: Leave unconnected.
CTLDLY			Leave unconnected.
AVDD1, AVDD2	_	_	Connect to VDD.
AVREF, AVSS1, AVSS2			Connect to Vss.
RESET	2	_	—
XT1			Connect to Vss.
XT2			Leave unconnected.
IC			Directly connect to Vss.

Remark	ENCTL	: bit 1 of amplifier control register (AMPC)
	ENREC	: bit 7 of amplifier mode register 0 (AMPM0)
	ENDRUM	: bit 2 of amplifier control register (AMPC)
	SELPGSEPA	: bit 2 of amplifier mode register 0 (AMPM0)
	ENCAP	: bit 3 of amplifier control register (AMPC)
	ENCSYN	: bit 5 of amplifier control register (AMPC)
	ENREEL	: bit 6 of amplifier control register (AMPC)
	ENCOMP	: bit 4 of amplifier control register (AMPC)



Figure 2-1. I/O Circuits of Respective Pins

#### 3. INTERNAL BLOCK FUNCTION

#### 3.1 CPU Registers

#### 3.1.1 General-purpose registers

The  $\mu$ PD784927 has eight banks of general-purpose registers. One bank consists of sixteen 8-bit general-purpose registers. Two of these 8-bit registers can be used in pairs as a 16-bit register. Four of the 16-bit general-purpose registers can be used to specify a 24-bit address in combination with an 8-bit address expansion register.

These eight banks of general-purpose registers can be selected by software or context switching function.

The general-purpose registers, except for the address expansion registers V, U, T, and W, are mapped to the internal RAM.



Figure 3-1. Configuration of General-Purpose Register

Caution Although R4, R5, R6, R7, RP2, and RP3 can be used as X, A, C, B, AX, and BC registers, respectively, by setting the RSS bit of PSW to 1, do not use this function. The function of the RSS bit is planned to be deleted from the future models in the 78K/IV Series.

#### 3.1.2 Other CPU registers

#### (1) Program counter

The program counter of the  $\mu$ PD784927 is 20 bits wide. The value of the program counter is automatically updated as the program is executed.



#### (2) Program status word

This is a register that holds the various statuses of the CPU. Its contents are automatically updated as the program is executed.

		15	14	13	12	11	10	9	8
	PSWH	UF	RBS2	RBS1	RBS0	—			—
PSW∢		7	6	5	4	3	2	1	0
	PSWL	S	Z	Note RSS	AC	IE	P/V	0	CY

**Note** The RSS flag is provided to maintain compatibility with the microcomputers in the 78K/III Series. Always clear this flag to 0 except when the software of the 78K/III Series is used.

#### (3) Stack pointer

This is a 24-bit pointer that holds the first address of the stack. Be sure to write 0 to the high-order 4 bits.

#### 3.2 Memory Space

A memory space of 1M bytes can be accessed. The mapping of the internal data area (special function registers and internal RAM) can be selected by using the LOCATION instruction. The LOCATION instruction must be always executed after reset has been cleared, and cannot be used more than once.

#### ★ (1) When LOCATION 0H instruction is executed

Part Number	Internal Data Area	Internal ROM Area
μPD784927, 784927Υ	0F700H-0FFFFH	00000H-0F6FFH 10000H-17FFFH
μPD784928, 784928Υ	0F100H-0FFFFH	00000H-0F0FFH 10000H-1FFFFH

**Remark** The area of the internal ROM overlapping the internal data area cannot be used when the LOCATION 0 instruction is executed.

Part Number	Unusable Area
μPD784927, 784927Υ	0F700H-0FFFFH (2304 bytes)
μPD784928, 784928Υ	0F100H-0FFFFH (3840 bytes)

#### ★ (2) When LOCATION 0FH instruction is executed

Part Number	Internal Data Area	Internal ROM Area
μPD784927, 784927Υ	FF700H-FFFFFH	00000H-17FFFH
μPD784928, 784928Υ	FF100H-FFFFFH	00000H-1FFFFH



#### Figure 3-2. Memory Map of $\mu$ PD784927, 784927Y

When LOCATION 0H instruction is executed

#### When LOCATION 0FH instruction is executed

Notes 1. Accessed in external memory expansion mode

2. The 2304 bytes in this area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.

3. When LOCATION 0H instruction is executed: 96000 bytes, when LOCATION 0FH instruction is executed: 98304 bytes

4. Base area or entry area for reset or interrupt. Excluding the internal RAM for reset.

784927Y,

784928Y

Z



**Notes 1.** Accessed in external memory expansion mode

- 2. The 3840 bytes in this area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.
- 3. When LOCATION 0H instruction is executed: 127232 bytes, when LOCATION 0FH instruction is executed: 131072 bytes
- 4. Base area or entry area for reset or interrupt. Excluding the internal RAM for reset.

M

#### 3.3 Special Function Registers (SFRs)

Special function registers are assigned special functions and mapped to a 256-byte space of addresses FF00H through FFFFH. These registers include mode registers and control registers that control the internal peripheral hardware units.

## Caution Do not access an address to which no SFR is assigned. If such an address is accessed by mistake, the $\mu$ PD784927 may be deadlocked. This deadlock can be cleared only by reset input.

Table 3-1 lists the special function registers (SFRs). The meanings of the symbols in this table are as follows:

- Symbol ...... Abbreviation of an SFR. This abbreviation is reserved for NEC's assembler (RA78K4). With a C compiler (CC78K4), the abbreviation can be used as sfr variable by the #pragma sfr instruction.
- R/W ...... Indicates whether the SFR in question can be read or written.
  - R/W : Read/write
  - R : Read only
  - W : Write only
- Bit length ...... Indicates the bit length (word length) of the SFR.
- Bit units for manipulation ...... Indicates bit units in which the SFR in question can be manipulated. An SFR that can be manipulated in 16-bit units can be used as the operand sfrp of an instruction. Specify an even address to manipulate this SFR.
   An SFR that can be manipulated in 1-bit units can be used for a bit manipulation instruction.
- After clearing reset ...... Indicates the status of each register immediately after clearing reset.
- Caution The addresses shown in Table 3-1 are used when the LOCATION 0H instruction is executed. Add "F0000H" to the address values shown in the table when the LOCATION 0FH instruction is executed.

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit	Bit Units	s for Man	ipulation	After Clearing
				Length	1 bit	8 bits	16 bits	Reset
FF00H	Port 0	P0	R/W	8	0	0	_	Undefined
FF02H	Port 2	P2	R	8	0	0	_	
FF03H	Port 3	P3	R/W	8	0	0	_	
FF04H	Port 4	P4	-	8	0	0	_	
FF05H	Port 5	P5		8	0	0	_	
FF06H	Port 6	P6		8	0	0	_	
FF07H	Port 7	P7	R	8	0	0	_	
FF08H	Port 8	P8	R/W	8	0	0	_	
FF09H	Port 9	P9		8	0	0	_	
FF0AH	Port 10	P10	R	8	0	0	—	
FF0BH	Port 11	P11		8	0	0	—	
FF0EH	Port 0 buffer register L	POL	R/W	8	0	0	-	
FF0FH	Port 0 buffer register H	P0H		8	0	0	-	
FF10H	Timer 0 compare register 0	CR00		16	_	_	0	Cleared to 0
FF11H	Event counter compare register 0	ECC0	W	8	_	0	-	
FF12H	Timer 0 compare register 1	CR01	R/W	16	_	_	0	
FF13H	Event counter compare register 1	ECC1	W	8	_	0	-	
FF14H	Timer 0 compare register 2	CR02	R/W	16	_	_	0	
FF15H	Event counter compare register 2	ECC2	W	8	_	0	-	
FF16H	Timer 1 compare register 0	CR10	R/W	16	_	_	0	
FF17H	Event counter compare register 3	ECC3	W	8	_	0	—	
FF18H	Timer 1 compare register 1	CR11	R/W	16	_	_	0	
FF1AH	Timer 1 compare register 2	CR12	R	16	—	_	0	
FF1CH	Timer 1 compare register 3	CR13	R/W	16	—	_	0	
FF1EH	Timer 2 compare register 0	CR20		16	—	_	0	
FF20H	Port 0 mode register	PM0		8	0	0	—	FFH
FF23H	Port 3 mode register	PM3		8	0	0	—	
FF24H	Port 4 mode register	PM4		8	0	0	—	
FF25H	Port 5 mode register	PM5		8	0	0	—	
FF26H	Port 6 mode register	PM6		8	0	0	—	
FF28H	Port 8 mode register	PM8		8	0	0	—	FDH
FF29H	Port 9 mode register	PM9		8	0	0	—	7FH
FF2EH	Real-time output port 0 control register	RTPC		8	0	0		00H
FF30H	Timer counter 0	TM0	R	16	_		0	Cleared to 0
FF31H	Event counter	EC	R/W	8		0	—	
FF32H	Timer counter 1	TM1	R	16			0	
FF34H	Free running counter (bits 0-15)	FRCL		16			0	0000H
FF35H	Free running counter (bits 16-21)	FRCH		8		0		00H
FF36H	Timer counter 2	TM2		16	-	_	0	Cleared to 0

#### Table 3-1. Special Function Registers (1/5)

**Remark** Cleared to 0: Counter is initialized to 0 within 16 clocks after the reset signal has been cleared (the contents before initialization are undefined).

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit	Bit Units	for Man	ipulation	After Clearing
				Length	1 bit	8 bits	16 bits	Reset
FF38H	Timer control register 0	TMC0	R/W	8	0	0	_	00H
FF39H	Timer control register 1	TMC1		8	0	0	_	
FF3AH	Timer control register 2	TMC2		8	0	0	_	
FF3BH	Timer control register 3	TMC3		8	0	0	_	00×0000
FF3CH	Timer counter 3	ТМЗ	R	16	_		0	Cleared to 0
FF3DH	Timer control register 4	TMC4	R/W	8	0	0	_	××000000
FF3EH	Timer counter 4	TM4	R	16	_	_	0	Cleared to 0
FF43H	Port 3 mode control register	PMC3	R/W	8	0	0	_	00H
FF48H	Port 8 mode control register	PMC8		8	0	0	_	
FF4BH	Control mode select register	CMS		8	0	0	_	
FF4DH	Trigger source select register 0	TRGS0		8	0	0	_	
FF4EH	Pull-up resistor option register L	PUOL		8	0	0	_	
FF4FH	Pull-up resistor option register H	PUOH		8	0	0	_	
FF50H	Input control register	ICR		8	0	0	_	10H
FF51H	Up/down counter count register	UDC		8	—	0	_	Undefined
FF52H	Event divider counter	EDV	R	8	—	0	_	Cleared to 0
FF53H	Capture mode register	CPTM	R/W	8	0	0	_	00H
FF54H	Timer counter 5	TM5	R	16	—	—	0	Cleared to 0
FF56H	Timer 3 capture register 0	CPT30		16	—	_	0	
FF58H	Timer 0 output mode register	TOM0	W	8	—	0	_	××000000
FF59H	Timer 0 output control register	TOC0		8	—	0	_	00H
FF5AH	Timer 1 output mode register	TOM1 <sup>Note 1</sup>	R/W	8	—	0	_	80H
FF5BH	Timer 1 output control register	TOC1	W	8	—	0	_	00H
FF5CH	Timer 3 compare register 0	CR30	R/W	16	—	—	0	Cleared to 0
FF5EH	Timer 3 compare register 1	CR31		16	—	—	0	
FF60H	Port 8 buffer register L	P8L		8	0	0	—	000×0×0×
FF63H	Up/down counter compare register	UDCC	W	8	—	0	—	Undefined
FF65H	Trigger source select register 1	TRGS1	R/W	8	0	0	—	00H
FF66H	Port 6 mode control register	PMC6		8	0	0	_	
FF68H	A/D converter mode register	ADM		16			0	0000H
		ADML <sup>Note 2</sup>		8	0	0	_	
FF6AH	A/D conversion result register	ADCR	R	8	—	0	—	Undefined
FF6CH	Hardware watch counter 0	HW0	R/W	16	—	_	0	Not affected
FF6EH	Hardware watch counter 1	HW1	R	16	—		0	by reset
FF6FH	Watch mode register	WM	R/W	8	0	0		00××0×00
FF70H	PWM control register 0	PWMC0		8	0	0	-	05H

#### Table 3-1. Special Function Registers (2/5)

**Notes 1.** When the TOM1 is read, the write sequence of the REC driver is read (bits 0 and 1).

2. ADML is the low-order 8 bits of ADM and can be manipulated in 1- or 8-bit units.

**Remark** Cleared to 0: Counter is initialized to 0 within 16 clocks after the reset signal has been cleared (the contents before initialization are undefined).

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit	Bit Units	for Man	ipulation	After Clearing
				Length	1 bit	8 bits	16 bits	Reset
FF71H	PWM control register 1	PWMC1	R/W	8	0	0	—	15H
FF72H	PWM0 modulo register	PWM0	1	16	_	_	0	0000H
FF73H	PWM2 modulo register	PWM2	1	8	_	0	_	00H
FF74H	PWM1 modulo register	PWM1	1	16	_	_	0	0000H
FF75H	PWM3 modulo register	PWM3	1	8	_	0	_	00H
FF76H	PWM5 modulo register	PWM5	1	16	_	_	0	0000H
FF77H	PWM4 modulo register	PWM4	1	8	_	0	_	00H
FF78H	Event divider control register	EDVC	W	8	_	0	—	Cleared to 0
FF79H	Clock output mode register	CLOM	R/W	8	0	0	_	00H
FF7AH	Timer 4 capture/compare register 0	CR40	1	16	_	_	0	Cleared to 0
FF7BH	Clock control register	СС	1	8	0	0	—	00H
FF7CH	Timer 4 capture register 1	CR41	R	16	_		0	Cleared to 0
FF7DH	Capture/compare control register	CRC	W	8	_	0	—	00H
FF7EH	Timer 5 compare register	CR50	R/W	16	_	_	0	Cleared to 0
FF80H	I <sup>2</sup> C control register	IICC	]	8	0	0	—	00H
FF82H	I <sup>2</sup> C clock select register	IICCL	]	8	0	0	—	
FF84H	Serial mode register 1	CSIM1	1	8	0	0	—	
FF85H	Serial shift register 1	SIO1	]	8	_	0	—	Undefined
FF86H	Slave address register	SVA	]	8	0	0	—	00H
FF88H	Serial mode register 2	CSIM2	]	8	0	0	—	
FF89H	Serial shift register 2	SIO2	]	8	—	0	—	Undefined
FF8AH	Serial control register 2	CSIC2		8	—	0	—	00H
FF8CH	I <sup>2</sup> C bus status register <sup>Note</sup>	lics	R	8	0	0	—	
FF8EH	I <sup>2</sup> C bus shift register <sup>Note</sup>	IIC	R/W	8	0	0	—	
FF90H	Amplifier mode register 2	AMPM2		8	0	0	—	
FF91H	Head amplifier switch output control register	HAPC		8	0	0	—	
FF94H	Amplifier control register	AMPC		8	0	0	—	
FF95H	Amplifier mode register 0	AMPM0		8	0	0	—	
FF96H	Amplifier mode register 1	AMPM1		8	0	0	—	
FF97H	Gain control register	CTLM		8	0	0	—	
FF98H	VISS detection circuit shift register 0	VSFT0		16	—	—	0	0000H
FF99H								
FF9AH	VISS detection circuit shift register 1	VSFT1		16	_	_	0	
FF9BH								
FFA0H	External interrupt mode register	INTM0		8	0	0	—	000000×0
FFA1H	External capture mode register 1	INTM1		8	0	0	—	00H
FFA2H	External capture mode register 2	INTM2		8	0	0	—	
FFA3H	VISS detection circuit control register	VDC		8	0	0	—	

Table 3-1. Special Function Registers (3/5)

**Note** These registers are provided for the  $\mu$ PD784928Y subseries only.

**Remark** Cleared to 0: Counter is initialized to 0 within 16 clocks after the reset signal has been cleared (the contents before initialization are undefined).

Address	Special Function Register (SFR) Name	Sym	bol	R/W	Bit	Bit Units	for Man	ipulation	After Clearing
					Length	1 bit	8 bits	16 bits	Reset
FFA4H	VISS detection circuit up/down counter register	VUE	C	R/W	8	—	0	—	00H
FFA5H	VUDC value setting register	VUD	ST		8	_	0	_	
FFA6H	Key interrupt control register	KE١	/C		8	0	0	—	70H
FFA7H	VISS pulse pattern setting register	VP	S		8	—	0	—	00H
FFA8H	In-service priority register	ISF	'nR	R	8	0	0	_	
FFAAH	Interrupt mode control register	IM	С	R/W	8	0	0	—	80H
FFACH	Interrupt mask flag register	MK0L	MKO		8	0	0	0	FFH
FFADH		МКОН	WITCO		8	0	0		
FFAEH		MK1L	MK1		8	0	0	0	
FFAFH		MK1H			8	0	0	]	
FFB0H	FRC capture register 0L	CPT	0L	R	16	_	_	0	Cleared to 0
FFB1H	FRC capture register 0H	CPT	ОH		8	_	0	_	
FFB2H	FRC capture register 1L	CPT	1L		16	_	_	0	
FFB3H	FRC capture register 1H	CPT	1H		8	_	0	_	
FFB4H	FRC capture register 2L	CPT	2L		16	_	_	0	
FFB5H	FRC capture register 2H	CPT	2H		8	_	0	_	
FFB6H	FRC capture register 3L	CPT	3L		16	_	_	0	
FFB7H	FRC capture register 3H	CPT	ЗН		8	_	0	_	
FFB8H	FRC capture register 4L	CPT	4L		16	_	_	0	
FFB9H	FRC capture register 4H	CPT	4H		8	_	0	_	
FFBAH	FRC capture register 5L	CPT	5L		16	_	_	0	
FFBBH	FRC capture register 5H	CPT	5H		8	_	0	_	
FFBDH	VSYNC separation circuit control register	VS	С	R/W	8	0	0	—	00H
FFBEH	VSYNC separation circuit up/down counter register	VSU	DC		8	_	0	-	
FFBFH	VSYNC separation circuit compare register	VSC	MP		8	_	0	-	FFH
FFC0H	Standby control register	STE	3C		8	—	0	—	0011×000
FFC4H	Execution speed select register	M	N	W	8	_	0	-	20H
FFCEH	CPU clock status register	PC	S	R	8	0	0	-	00H
FFCFH	Oscillation stabilization time specification register	OS	ГS	W	8	_	0	-	
FFE0H	Interrupt control register (INTP0)	PIC	0	R/W	8	0	0	-	43H
FFE1H	Interrupt control register (INTCPT3)	CPT	IC3		8	0	0	_	
FFE2H	Interrupt control register (INTCPT2)	CPT	IC2		8	0	0	-	
FFE3H	Interrupt control register (INTCR12)	CRIC	012		8	0	0	_	
FFE4H	Interrupt control register (INTCR00)	CRIC	000		8	0	0	-	
FFE5H	Interrupt control register (INTCLR1)	CLR	IC1		8	0	0	-	
FFE6H	Interrupt control register (INTCR10)	CRIC	C10		8	0	0	_	

#### Table 3-1. Special Function Registers (4/5)

**Remark** Cleared to 0: Counter is initialized to 0 within 16 clocks after the reset signal has been cleared (the contents before initialization are undefined).

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit	Bit Units	for Man	ipulation	After Clearing
				Length	1 bit	8 bits	16 bits	Reset
FFE7H	Interrupt control register (INTCR01)	CRIC01	R/W	8	0	0	—	43H
FFE8H	Interrupt control register (INTCR02)	CRIC02		8	0	0	-	
FFE9H	Interrupt control register (INTCR11)	CRIC11		8	0	0	—	
FFEAH	Interrupt control register (INTCPT1)	CPTIC1		8	0	0	—	
FFEBH	Interrupt control register (INTCR20)	CRIC20		8	0	0	—	
FFECH	Interrupt control register (INTIIC)Note 1	IICIC		8	0	0	—	
FFEDH	Interrupt control register (INTTB)	TBIC		8	0	0	—	
FFEEH	Interrupt control register (INTAD)	ADIC		8	0	0	—	
FFEFH	Interrupt control register (INTP2)Note 2	PIC2		8	0	0	—	
	Interrupt control register (INTCR40)Note 2	CRIC40						
<b>FFF0H</b>	Interrupt control register (INTUDC)	UDCIC		8	0	0	—	
FFF1H	Interrupt control register (INTCR30)	CRIC30		8	0	0	—	
FFF2H	Interrupt control register (INTCR50)	CRIC50		8	0	0	—	
FFF3H	Interrupt control register (INTCR13)	CRIC13		8	0	0	—	
FFF4H	Interrupt control register (INTCSI1)	CSIIC1		8	0	0	—	
FFF5H	Interrupt control register (INTW)	WIC		8	0	0	—	×1000011
FFF6H	Interrupt control register (INTVISS)	VISIC		8	0	0	—	43H
FFF7H	Interrupt control register (INTP1)	PIC1	]	8	0	0	_	
FFF8H	Interrupt control register (INTP3)	PIC3	]	8	0	0	_	
FFFAH	Interrupt control register (INTCSI2)	CSIIC2		8	0	0	_	

#### Table 3-1. Special Function Registers (5/5)

**Notes 1.**  $\mu$ PD784928Y subseries only.

- 2. PIC2 and CRIC40 are at the same address (register).
- **Remark** Cleared to 0: Counter is initialized to 0 within 16 clocks after the reset signal has been cleared (the contents before initialization are undefined).

#### 3.4 Ports

The  $\mu$ PD784927 is provided with the ports shown in Figure 3-3. Table 3-2 shows the function of each port.



Figure 3-4. Port Configuration

Table 3-2. Port Function

Name	Pin Name	Function	Specification of Pull-up Resistor
Port 0	P00-P07	Can be set in input or output mode in 1-bit units.	Pull-up resistors are connected to all pins in input mode.
Port 2	P20-P23	Input port	Pull-up resistors are connected to pins P22 and P23.
Port 3	P30-P37	Can be set in input or output mode in 1-bit units.	Pull-up resistors are connected to all pins in input mode.
Port 4	P40-P47	Can be set in input or output mode in 1-bit units. Can directly drive LED.	
Port 5	P50-P57	Can be set in input or output mode in	
Port 6	P60-P67	1-bit units.	
Port 7	P70-P77	Input port	Pull-up resistor is not provided.
Port 8	P80, P82-P87	Can be set in input or output mode in	Pull-up resistors are connected to all pins
Port 9	P90-P96	1-bit units.	in input mode.
Port 10	P100-P103	Input port	Pull-up resistor is not provided.
Port 11	P110-P113		

#### 3.5 Real-Time Output Port

A real-time output port consists of a port output latch and a buffer register (refer to Figure 3-5).

The function to transfer the data prepared in advance in the buffer register to the output latch when a trigger such as a timer interrupt occurs, and output the data to an external device is called a real-time output function. A port used in this way is called a real-time output port (RTP).

Table 3-3 shows the real-time output ports of the  $\mu$ PD784927.

Table 3-4 shows the trigger sources of RTPs.





Table 3-3. Bit Configuration of RTP

RTP	Shared with:	Number of Bits of Real-Time Output Data	Number of Bits That Can Be Specified as RTP	Remark
RTP0	Port 0	4 bits $\times$ 2 channels or 8 bits $\times$ 1 channel	4-bit units	_
RTP8	Port 8	1 bit × 1 channel and 2 bits × 1 channel	1-bit units	Pseudo V <sub>SYNC</sub> output: 1 channel (RTP80) Head amplifier switch: 1 channel (RTP82) Chrominance rotation signal output: 1 channel (RTP83)

Table 3-4.	Trigger	Sources	of	RTP
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RTP	Trigger Source	INTCR00	INTCR01	INTCR02	INTCR13	INTCR50	INTP0	Remark
RTP0	High-order 4 bits		0					
	Low-order 4 bits			0			0	
	All 8 bits			0			0	
RTP8	Bit 0		0	0	0	0		Note 1
	Bits 2 and 3	0						Note 2

**Notes 1.** Select one of the four trigger sources.

2. When the real-time output port mode is set by the port mode control register 8 (PMC8), the HASW and ROT-C signals that are set by the head amplifier switch output control register (HAPC) are directly output. The HASW and ROT-C signals are synchronized with HSW output (TM0-CR00 coincidence signal). However, the set signal is output immediately when the HAPC register is rewritten.

Figures 3-6 and 3-7 show the block diagrams of RTP0 and RTP8. Figure 3-8 shows the types of RTP output trigger sources.



Figure 3-6. Block Diagram of RTP0

Remark INTCR01: TM0-CR01 coincidence signal INTCR02: TM0-CR02 coincidence signal







Figure 3-8. Types of RTP Output Trigger Sources

RTP80 can output low-level, high-level, and high-impedance values real-time.

Because RTP80 can superimpose a horizontal sync signal, it can be used to create pseudo vertical sync signal. When RTP80 is set in the pseudo V<sub>SYNC</sub> output mode, it repeatedly outputs a specific pattern when an output trigger occurs.

Figure 3-9 shows the operation timing of RTP80.

#### Figure 3-9. Example of Operation Timing of RTP80

#### (a) When HSYNC signal is superimposed



#### (b) Pseudo VSYNC output mode



#### 3.6 Super Timer Unit

The  $\mu$ PD784927 is provided with a super timer unit that consists of the timers, and VCR special circuits such as a VISS detection circuit and a VsyNc separation circuit, etc., shown in Table 3-5.

Unit Name	Timer/Counter	Resolution	Maximum	Register	Remark
<b>T</b> imer 0	TMO	4	Count Time	0.000	
Timer 0		ιμs	65.5 ms	CRUU	Controls delay of video nead switching signal
	(16-bit timer)			CRU1	Controls delay of audio nead switching signal
				CR02	Controls pseudo VsyNc output timing
	EC	_	_	ECC0, ECC1,	Creates internal head switching signal
	(8-bit counter)			ECC2, ECC3	
Free	FRC	125 ns	524 ms	CPT0	Detects reference phase (to control drum phase)
running	(22-bit counter)			CPT1	Detects phase of drum motor (to control drum
counter					phase)
				CPT2	Detects speed of drum motor (to control drum
					speed)
				CPT3	Detects speed of capstan motor (to control speed
					of capstan motor)
				CPT4, CPT5	Detects remaining tape for reel FG
Timer 1	TM1	1 <i>µ</i> s	65.5 ms	CR10	Playback: Creates internal reference signal
	(16-bit timer)				Recording: Buffer oscillator in case VsyNc is
	. ,				missing
				CR11	Controls RECCTL output timing
				CB12	Detects phase of capstan motor (to control capstan
					nhase)
				CB13	Controls V <sub>SYNC</sub> mask as noise preventive measures
	ТМЗ	1 <i>u</i> s or	65.5 ms or	CR30, CR31	Controls duty detection timing of PBCTL signal
	(16-bit timer)	, 1.1 μs	71.5 ms	CPT30	Measures cycle of PBCTL signal
	FDV		_	FDVC	Divides CEG signal frequency
	(8-bit counter)			2010	
Timer 2		1 //s	65.5 ms	CB20	Can be used as interval timer (to control system)
	(16 bit timor)	ι μ5	00.0 113	01120	Can be used as interval linter (to control system)
Timor 4		2 110	121 mc	CP40	Detects duty of remote controller signal (to decade
TIMEI 4	(16  bit times)	2 μ5	131 1115	0140	
	(10-bit tiller)			0041	Macaurea avala of remote controllar signal (to de
				CR41	Measures cycle of remote controller signal (to de
					code remote controller signal)
Timer 5	IM5	2 µs	131 ms	CR50	Can be used as interval timer (to control system)
	(16-bit timer)				
Up/down	UDC	_	_	UDCC	Creates linear tape counter
counter	(5-bit counter)				
PWM	—	—	—	PWM0, PWM1,	16-bit resolution (carrier frequency: 62.5 kHz)
output unit				PWM5	
				PWM2, PWM3,	8-bit resolution (carrier frequency: 62.5 kHz)
				PWM4	

#### Table 3-5. Configuration of Super Timer Unit
# (1) Timer 0 unit

Timer 0 unit creates head switching signal and pseudo V<sub>SYNC</sub> output timing from the PG and FG signals of the drum motor.

This unit consists of an event counter (EC: 8 bits), compare registers (ECC0 through ECC3), a timer (TM0: 16 bits), and compare registers (CR00 through CR02).

A signal indicating coincidence between the value of timer 0 and the value of a compare register can be used as the output trigger of the real-time output port.

# (2) Free running counter unit

The free running counter unit detects the speed and phase of the drum motor, and the speed and reel speed of the capstan motor.

This unit consists of a free running counter (FRC), capture registers (CPT0 through CPT5), a VSYNC separation circuit, and a HSYNC separation circuit.

# (3) Timer 1 unit

Timer 1 unit is a reference timer unit synchronized with the frame cycle and creates the RECCTL signal, detects the phase of the capstan motor, and detects the duty factor of the PBCTL signal. This unit consists of the following three groups:

- Timer 1 (TM1), compare registers (CR10, CR11, and CR13), and capture register (CR12)
- Timer 3 (TM3), compare registers (CR30 and CR31), and capture register (CPT30)
- Event divider counter (EDV) and compare register (EDVC)

The TM1-CR13 coincidence signal can be used for automatic unmasking of V<sub>SYNC</sub> or as the output trigger of the real-time output port.

Figure 3-10. Block Diagram of Super Timer Unit (TM0, FRC, TM1)



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# (4) Timer 2 unit

Timer 2 unit is a general-purpose 16-bit timer unit.

This unit consists of a timer (TM2) and a compare register (CR20).

The timer is cleared when the TM2-CR20 coincidence signal occurs, and at the same time, an interrupt request is generated.

#### Figure 3-11. Block Diagram of Timer 2 Unit



## (5) Timer 4 unit

Timer 4 unit is a general-purpose 16-bit timer unit.

This unit consists of a timer (TM4), a capture/compare register (CR40), and a capture register (CR41). The value of the timer is captured to CR40/CR41 when the INTP2 signal is input. This timer can be used to decode a remote controller signal.

#### Figure 3-12. Block Diagram of Timer 4 Unit



## (6) Timer 5 unit

Timer 5 unit is a general-purpose 16-bit timer unit.

This unit consists of a timer (TM5) and a compare register (CR50).

The timer is cleared by the TM5-CR50 coincidence signal, and at the same time, an interrupt request is generated.

#### Figure 3-13. Block Diagram of Timer 5 Unit



# (7) Up/down counter unit

The up/down counter unit is a counter that realizes a linear time counter.

This unit consists of an up/down counter (UDC) and a compare register (UDCC).

The up/down counter counts up the rising edges of PBCTL and counts down the falling edges of PBCTL. When the value of the up/down counter coincides with the value of the compare register, or when the counter underflows, an interrupt request is generated.





## (8) PWM output unit

The PWM output unit has three 16-bit accuracy output lines (PWM0, PWM1, and PWM5) and 8-bit accuracy output lines (PWM2 through PWM4). The carrier frequency of all the output lines is 62.5 kHz (fcLK = 8 MHz). PWM0 and PWM1 can be used to control the drum motor and capstan motor.

## Figure 3-15. Block Diagram of 16-Bit PWM Output Unit





Figure 3-16. Block Diagram of 8-Bit PWM Output Unit

(9) VISS detection circuit





#### (10) VSYNC separation circuit





# 3.7 Serial Interface

The  $\mu$ PD784927 is provided with the serial interfaces shown in Table 3-6.

Data can be automatically transmitted or received through these serial interfaces, when the macro service is used.

 Table 3-6.
 Types of Serial Interfaces

Name	Function
Serial interface channel 1	<ul> <li>Clocked serial interface (3-wire)</li> <li>Bit length: 8 bits</li> <li>Clock rate: External clock/31.25 kHz/62.5 kHz/125 kHz/250 kHz/500 kHz/1 MHz (fcLK = 8 MHz)</li> <li>MSB first/LSB first selectable</li> </ul>
Serial interface channel 2	<ul> <li>Clocked serial interface (3-wire)</li> <li>Bit length: 8 bits</li> <li>Clock rate: External clock/31.25 kHz/62.5 kHz/125 kHz/250 kHz/500 kHz/1 MHz (fcLk = 8 MHz)</li> <li>MSB first/LSB first selectable</li> <li>BUSY/STRB control function</li> </ul>
Serial interface channel 3	I <sup>2</sup> C bus interface     For multimaster

(1) Serial interface channels 1, 2





Remark The circuits enclosed in the broken line are provided to serial interface channel 2 only.

# (2) Serial interface channel 3 (µPD784928Y subseries only)

This channel transfers 8-bit data with multiple devices using two lines: serial clock (SCL) and serial data bus (SDA).

It conforms to the I<sup>2</sup>C bus format, and can output a "start condition", "data", and "stop condition" onto the serial data bus during transmission. This data is automatically detected by hardware during reception. SCL and SDA are open-drain output pins and therefore, must be connected with a pull-up resistor.

Figure 3-20. Serial Interface Channel 3



# 3.8 A/D Converter

The  $\mu$ PD784927Y has an analog-to-digital (A/D) converter with 12 multiplexed analog inputs (ANI0 through ANI11). This A/D converter is of successive approximation type, and the conversion result is held by an 8-bit A/D conversion result register (ADCR) (conversion time: 10  $\mu$ s at fcLK = 8 MHz).

A/D conversion can be started in the following two modes:

- Hardware start: Conversion is started by a hardware triggerNote.
- Software start : Conversion is started by setting a bit of the A/D converter mode register (ADM).

After conversion has been started, the A/D converter operates in the following modes:

- Scan mode : Sequentially selects more than one analog input to obtain data to be converted from all the pins.
- Select mode: Use only one pin for analog input to obtain successive data to be converted.

When the conversion result is transferred to ADCR, interrupt request INTAD is generated. By processing this interrupt with the macro service, the conversion result can be successively transferred to memory.

A mode in which starting A/D conversion of the next pin is kept pending until the value of ADCR is read is also available. When this ode is used, reading the conversion result by mistake when timing is shifted because an interrupt is disabled can be prevented.

- **Note** A hardware trigger is the following coincidence signals, one of which is selected by the trigger source select register 1 (TRGS1):
  - TM0-CR01 coincidence signal
  - TM0-CR02 coincidence signal
  - TM1-CR13 coincidence signal
  - TM5-CR50 coincidence signal



Figure 3-21. Block Diagram of A/D Converter

## 3.9 VCR Analog Circuits

The  $\mu$ PD784927 is provided with the following VCR analog circuits:

- CTL amplifier
- RECCTL driver (rewritable)
- DPG amplifier
- DFG amplifier
- DPFG separation circuit (ternary separation circuit)
- CFG amplifier
- Reel FG comparator (2 channels)
- CSYNC comparator

# (1) CTL amplifier/RECCTL driver

The CTL amplifier is used to amplify the playback control (PBCTL) signal that is reproduced from the CTL signal recorded on a VCR tape.

The gain of the CTL amplifier is set by the gain control register (CTLM). Thirty-two types of gains can be set in increments of about 1.78 dB.

The  $\mu$ PD784927 is also provided with a gain control signal generation circuit that monitors the status of the amplifier output to perform optimum gain control by software. The gain control signal generation circuit generates a CTL detection flag that identifies the amplitude status of the CTL amplifier output. By using this CTL detection flag, the gain of the CTL amplifier can be optimized.

The RECCTL driver writes a control signal onto a VCR tape.

This driver operates in two modes: REC mode that is used for recording, and rewrite mode used to rewrite the VISS signal. The output status of the RECCTL± pin is changed by hardware, by using the timer output from the super timer unit as a trigger.



Figure 3-22. Block Diagram of CTL Amplifier and RECCTL Driver

# (2) DPG amplifier, DFG amplifier, and DFPG separation circuit

The DPG amplifier converts the drum PG (DPG) signal that indicates the phase information of the drum motor into a logic signal.

The DFG amplifier amplifies the drum FG (DFG) signal that indicates the speed information of the drum motor. The DPFG separation circuit (ternary separation circuit) separates a drum PFG (DPFG) signal having speed and phase information into a DFG and DPG signals.





# (3) CFG amplifier

The CFG amplifier amplifies the capstan FG (CFG) signal that indicates the speed information of the capstan motor. This amplifier consists of an operational amplifier and a comparator. The gain of the operational amplifier is set by using an external resistor.

When the gain of the operational amplifier is set to 50 dB, the output duty accuracy of the CFG signal can be improved to  $50.0 \pm 0.3\%$ .





## (4) Reel FG comparators

The reel FG comparator converts a reel FG signal that indicates the speed information of the reel motor into a logic signal. Two comparators, one for take-up and the other for supply, are provided.

Figure 3-25. Block Diagram of Reel FG Comparators



# (5) CSYNC comparator

The CSYNC comparator converts the COMPSYNC signal into a logic signal.





#### (6) Reference amplifier

The reference amplifier generates a reference voltage (VREF) to be supplied to the internal amplifiers and comparators of the  $\mu$ PD784927.



Figure 3-27. Block Diagram of Reference Amplifier



# (7) Analog circuit monitor function

This function is to output the following signals to port pins, and is mainly used for debugging.

- Comparator output of CTL amplifier  $\rightarrow$  CTLMON (multiplexed port: P67)
- Comparator output of CFG amplifier  $\rightarrow$  CFGMON (multiplexed port: P66)
- Comparator output of DPG amplifier  $\rightarrow$  DPGMON (multiplexed port: P65)
- Comparator output of DFG amplifier  $\rightarrow$  DFGMON (multiplexed port: P64)

#### 3.10 Watch Function

The  $\mu$ PD784927 has a watch function that counts the overflow signals of the watch timer by hardware. As the clock, the subsystem clock (32.768 kHz) is used.

Because this watch function is independent of the CPU, it can be used even while the CPU is in the standby mode (STOP mode) or is reset. In addition, this function can be used at a low voltage of  $V_{DD} = 2.7 \text{ V}$  (MIN.).

Therefore, by using only the watch function with the CPU set in the standby mode or reset, a watch operation can be performed at a low voltage and low current consumption.

In addition, the watch function can also be used while the CPU is in the normal operation mode, because a dedicated counter is provided.

The watch function can be used to count up to about 17 years of data.

The hardware watch counters (HW0 and HW1) are shared with external input counters. These counters execute counting at the falling edge of input to the P65 pin, and can be used to count the HsyNc signals.



#### Figure 3-28. Block Diagram of Watch Counter

#### 3.11 Clock Output Function

The  $\mu$ PD784927 can output a square wave (with a duty factor of 50%) to the P60/STRB/CLO pin as the operating clock for the peripheral devices or other microcomputers. To enable or disable the clock output, and to set the frequency of the clock, the clock output mode register (CLOM) is used.

When setting the frequency, the division ratio can be set to  $f_{CLK}/n$  (where n = 1, 2, 4, 8, 16, 32, 64, or 128) ( $f_{CLK} = f_{OSC}/2$ : fosc is the oscillation frequency of the resonator).

Figure 3-29 shows the block diagram of the clock output circuit.

The clock output (CLO) pin is shared with P60 and STRB.





Remark fclk: internal system clock

Caution Do not use the clock output function in the STOP mode. Clear ENCLO (CLOM.4) to 0 in the STOP mode.





# 3.12 Buzzer Output Function

The BUZ signal can be superimposed on P61 or P64.

The buzzer output frequency can be generated from the subsystem clock frequency or main system clock frequency.

Figure 3-31 shows the block diagram of the BUZ output circuit.

The BUZ signal can be also used for trimming the subsystem clock.





# 4. INTERNAL/EXTERNAL CONTROL FUNCTION

#### 4.1 Interrupt Function

The μPD784927 has as many as 32 interrupt sources, including internal and external sources. For 28 sources, a high-speed interrupt processing mode such as context switching or macro service can be specified by software. Table 4-1 lists the interrupt sources.

Interrupt			Interrupt Request Source	Interrupt	Macro	Context	Macro Service	Vector
Request	Priority	Nomo	Triagor	Control Register	Service	Switching	Control Word	Table
Туре		Name	l rigger	Name			Address	Address
Reset	_	RESET	RESET pin input	—	No	No		0000H
Non-	-	NMI	NMI pin input edge	_			_	0002H
maskable								
Maskable	0	INTP0	INTP0 pin input edge	PIC0	Yes	Yes	FE06H	0006H
	1	INTCPT3	EDVC output signal (CPT3 capture)	CPTIC3			FE08H	0008H
	2	INTCPT2	DFGIN pin input edge (CPT2 capture)	CPTIC2			FE0AH	000AH
	3	INTCR12	PBCTL input edge/EDVC output signal	CRIC12			FE0CH	000CH
			(CR12 capture)					
	4	INTCR00	TM0-CR00 coincidence signal	CRIC00			FE0EH	000EH
	5	INTCLR1	CSYNCIN pin input edge	CLRIC1			FE10H	0010H
	6	INTCR10	TM1-CR10 coincidence signal	CRIC10			FE12H	0012H
	7	INTCR01	TM0-CR01 coincidence signal	CRIC01			FE14H	0014H
	8	INTCR02	TM0-CR02 coincidence signal	CRIC02			FE16H	0016H
	9	INTCR11	TM1-CR11 coincidence signal	CRIC11			FE18H	0018H
	10	INTCPT1	Pin input edge/EC output signal	CPTIC1			FE1AH	001AH
			(CPT1 capture)					
	11	INTCR20	TM2-CR20 coincidence signal	CRIC20			FE1CH	001CH
	12	INTIIC	End of I <sup>2</sup> C bus transfer	IICIC <sup>Note</sup>			FE1EH	001EH
	13	INTTB	Time base from FRC	TBIC			FE20H	0020H
	14	INTAD	A/D converter conversion end	ADIC			FE22H	0022H
	15	INTP2	INTP2 pin input edge	PIC2			FE24H	0024H
		INTCR40	TM4-CR40 coincidence signal	CRIC40				
	16	INTUDC	UDC-UDCC coincidence/UDC underflow	UDCIC			FE26H	0026H
	17	INTCR30	TM3-CR30 coincidence signal	CRIC30			FE28H	0028H
	18	INTCR50	TM5-CR50 coincidence signal	CRIC50			FE2AH	002AH
	19	INTCR13	TM1-CR13 coincidence signal	CRIC13			FE2CH	002CH
	20	INTCSI1	End of serial transfer (channel 1)	CSIIC1			FE2EH	002EH
	21	INTW	Overflow of watch timer	WIC			FE30H	0030H
	22	INTVISS	VISS detection signal	VISIC			FE32H	0032H
	23	INTP1	INTP1 pin input edge	PIC1			FE34H	0034H
	24	INTP3	INTP3 pin input edge	PIC3			FE36H	0036H
	25	INTCSI2	End of serial transfer (channel 2)	CSIIC2			FE3AH	003AH
Operand	_	_	Illegal operand of MOV STBC, #byte or	_	No	No	_	003CH
error			LOCATION instruction					
Software	_		Execution of BRK instruction					003EH
	—		Execution of BRKCS instruction	_		Yes	_	_

#### Table 4-1. Interrupt Sources

**Note**  $\mu$ PD784928Y subseries only.

- Remark EVDC : Event divider compare register
  - EC : Event counter
  - FRC : Free running counter
  - MSCW: Macro service control register



#### Figure 4-1. Differences in Operation Depending on Interrupt Processing Mode

- **Notes 1.** When the register bank switching function is used and when initial values are set in advance to the registers
  - 2. Selecting a register bank and saving PC and PSW by context switching
  - 3. Restoring register bank, PC, and PSW by context switching
  - 4. Saves PC and PSW to stack and loads vector address to PC

## 4.1.1 Vectored interrupt

When an interrupt request is acknowledged, an interrupt processing program is executed according to the data stored in the vector table area (the first address of the interrupt processing program created by the user). In addition, four levels of priorities can be specified by software.

4.1.2 Context switching

When an interrupt request is generated or when the BRKCS instruction is executed, a specific register bank is selected by hardware, and execution branches to a vector address set in advance in the register bank. At the same time, the current contents of the program counter (PC) and program status word (PSW) are saved to the registers in the register bank. Because the contents of PC and PSW are not saved to the stack area, execution can be branched to an interrupt processing routine more quickly than the vectored interrupt.





## 4.1.3 Macro service

The macro service is a function to transfer data between the memory and a special function register (SFR) without intervention by the CPU. A macro service controller accesses the memory and SFR and directly transfers the data. Because the status of the CPU is not saved or restored, data can be transferred more quickly than context switching. The processing that can be executed with the macro service is described below.





## (1) Counter mode

In this mode, the value of the macro service counter (MSC) is decremented when an interrupt request occurs. This mode can be used to execute the division operation of an interrupt request or count the number of times an interrupt request has occurred.

When the value of the macro service counter has been decremented to 0, a vectored interrupt occurs.



## (2) Compound data transfer mode

When an interrupt request occurs, data are simultaneously transferred from an 8-bit SFR to memory, a 16-bit SFR to memory (word), memory (byte) to an 8-bit SFR, and memory (word) to a 16-bit SFR (3 points MAX. for each transfer).

This mode can also be used to exchange data, instead of transferring data.

This mode can be used for automatic transfer/reception by the serial interface or automatic updating of data/ timing by the serial output port.

When the value of the macro service counter reaches to 0, a vectored interrupt request occurs.



# (3) Macro service type A

When an interrupt request occurs, data is transferred from an 8-/16-bit SFR to memory (byte/word) or from memory (byte/word) to an 8-/16-bit SFR.

Data is transferred the number of times set in advance by the macro service counter.

This mode can be used to store the result of A/D conversion or for automatic transfer (or reception) by the serial interface.

Because transfer data is stored at an address FE00H to FEFFH, if only a small quantity of data is to be transferred, the data can be transferred at high speeds.

When the value of the macro service counter is decremented to 0, a vectored interrupt request occurs.



## (4) Data pattern identification mode (VISS detection mode)

This mode of macro service is for detection of the VISS signal and is used in combination with a pulse width detection circuit.

When an interrupt request occurs, the content of bit 7 of an SFR (usually, TMC3) specified by SFR pointer 1 is shifted into the buffer area. At the same time, the data in the buffer area is compared with the data in the compare area. If the two data coincide, a vectored interrupt request is generated. When the value of the macro service counter is decremented to 0, a vectored interrupt request occurs.

It can be specified by option that the value of an SFR (usually, CPT30) specified by SFR pointer 2 be multiplied by a coefficient and the result of this multiplication be stored to an SFR (usually, CR30) specified by SFR pointer 3 (this operation is to automatically update an identification threshold value when the tape speed fluctuates).



#### 4.1.4 Application example of macro service

#### (1) Automatic transfer/reception of serial interface

Automatic transfer/reception of 3-byte data by serial interface channel 1 Setting of macro service register: compound data transfer mode (exchange mode)



# (2) Reception operation of serial interface

Transfer of receive data by serial interface channel 1 (16 bytes) Setting of macro service mode register: macro service type A (1-byte data transfer from SFR to memory)



# (3) VISS detection operation

Setting of macro service mode register: data pattern identification mode (with multiplication, 8-byte comparison)



# 4.2 Standby Function

The standby function is to reduce the power consumption of the chip and is used in the following modes:

Mode	Function
HALT mode	Stops operating clock of CPU. Reduces average power consumption when used in combination with normal mode for intermittent operation
STOP mode	Stops oscillator. Stops all internal operations of chip to minimize power consumption to leakage current only
Low power consumption mode	Stops main system clock with subsystem clock used as system clock. CPU can operate with subsystem clock to reduce current consumption
Low power consumption HALT mode	Standby function in low power consumption mode. Stops operating clock of CPU. Reduces power consumption of overall system

These modes are programmable.

The macro service can be started in the HALT mode.





Notes 1. NMI input means starting NMI by NMI pin input, watch interrupt, or key interrupt input.

2. Unmasked interrupt request



Figure 4-5. Relations among NMI, Watch Interrupt, and Key Interrupt When STOP Mode Is Released

Z 

4.3

**Clock Generation Circuit** 

The clock generation circuit generates and controls the internal system clock (CLK) to be supplied to the CPU and

# "PD784927, 784928, 784927Y, 784928Y

# Figure 4-6. Block Diagram of Clock Generation Circuit



Notes 1. fxx: oscillation frequency, ( ): in low-frequency oscillation mode.

2. The peripheral hardware units that can operate with the subsystem clock have some restrictions. For details, refer to  $\mu$ PD784928, 784928Y Subseries User's Manual-Hardware (U12648E).

#### 4.4 Reset Function

When a low-level signal is input to the RESET pin, the system is reset, and each hardware unit is initialized (reset status). During the reset period, oscillation of the system clock is unconditionally stopped, so that the current consumption of the overall system can be reduced.

When the RESET pin goes high, the reset status is cleared. After the count time of the oscillation stabilization timer (32.8 ms at 16 MHz or 65.6 ms at 8 MHz) has elapsed, the contents of the reset vector table are set to the program counter (PC), and execution branches to the address set to the PC, and the program is executed starting from the branch destination address. Therefore, execution can be reset and started from any address.





The RESET pin is provided with an analog delay noise rejection circuit to prevent malfunctioning due to noise.

Figure 4-8. Accepting Reset Signal



# 5. INSTRUCTION SET

# (1) 8-bit instructions (( ): combination realized by using A as r)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC, CHKL, CHKLA

r' saddr' !!addr24 [saddrp] PSWL	
IST Operand \\ [[%saddrg]] PSWH	
A (MOV) (MOV) MOV (MOV) <sup>Note 6</sup> MOV (MOV) MOV (MOV) (MOV) (MOV)	
ADD <sup>Note 1</sup> (XCH) XCH (XCH) <sup>Note 6</sup> (XCH) (XCH) XCH (XCH) (XCH)	
(ADD)Note 1 (ADD)Note 1 (ADD)Note 1 (ADD)Note 1,6 (ADD)Note 1 ADDNote 1 ADDNote 1 (ADD)Note 1 (ADD)Note 1 (ADD)Note 1	
r MOV (MOV) MOV MOV MOV MOV MOV ROR <sup>Note 3</sup>	MULU
ADD <sup>Note 1</sup> (XCH) XCH XCH XCH XCH	DIVUW
(ADD)Note 1 ADDNote 1 ADDNote 1 ADDNote 1	INC
	DEC
saddr MOV (MOV) <sup>Note 6</sup> MOV MOV	INC
ADDNote 1 (ADD)Note 1 ADDNote 1 XCH	DEC
ADDNote 1	DBNZ
sfr MOV MOV MOV	PUSH
ADDNote 1 (ADD)Note 1 ADDNote 1	POP
	CHKL
	CHKLA
laddr16 MOV (MOV) MOV	
!!addr24 ADD <sup>Note 1</sup>	
mem MOV	
[saddrp] ADD <sup>Note 1</sup>	
[%saddrg]	
mem3	ROR4
	ROL4
r3 MOV MOV	
PSWL	
PSWH	
B, C	DBNZ
STBC, WDM MOV	
[TDE+] (MOV) MOVBK <sup>Note 5</sup>	
(ADD) <sup>Note 1</sup>	
MOVM <sup>Note 4</sup>	
[TDE-] (MOV) MOVBK <sup>Note 5</sup>	
(ADD)Note 1	
MOVM <sup>Note 4</sup>	

Notes 1. ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as ADD.

- 2. Either the second operand is not used, or the second operation is not an operand address.
- 3. ROL, RORC, ROLC, SHR, and SHL are the same as ROR.
- 4. XCHM, CMPME, CMPMNE, CMPMNC, and CMPMC are the same as MOVM.
- 5. XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC are the same as MOVBK.
- 6. If saddr2 instead of saddr is used in this combination, the code length of some instructions is short.

(2) 16-bit instructions ((): combination realized by using AX as rp) MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

2nd Operand	# word	AX	rp	saddrp	sfrp	laddr16	mem	[WHL+]	byte	n	None Note 2
			rp'	saddrp		!!addr24	[saddrp]				
1st Operand							[%saddrg]				
AX	(MOVM)	(MOVW)	(MOVW)	(MOVW)Note 3	MOVW	(MOVW)	MOVW	(MOVW)			
	ADDW <sup>Note 1</sup>	(XCHW)	(XCHW)	(XCHW) <sup>Note 3</sup>	(XCHW)	XCHW	XCHW	(XCHW)			
		(ADDW)Note 1	(ADDW)Note 1	(ADDW) <sup>Notes 1,3</sup>	(ADDW)Note 1						
rp	MOVW	(MOVW)	MOVW	MOVW	MOVW	MOVW				SHRW	MULWNote 4
	ADDW <sup>Note 1</sup>	(XCHW)	XCHW	XCHW	XCHW					SHLW	INCW
		(ADDW)Note 1	ADDW <sup>Note 1</sup>	ADDW <sup>Note 1</sup>	ADDW <sup>Note 1</sup>						DECW
saddrp	MOVW	(MOVW)Note 3	MOVW	MOVW							INCW
	ADDW <sup>Note 1</sup>	(ADDW)Note 1	ADDW <sup>Note 1</sup>	XCHW							DECW
				ADDW <sup>Note 1</sup>							
sfrp	MOVW	MOVW	MOVW								PUSH
	ADDW <sup>Note 1</sup>	(ADDW)Note 1	ADDW <sup>Note 1</sup>								POP
!addr16	MOVW	(MOVW)	MOVW						MOVTBLW		
!!addr24											
mem		MOVW									
[saddrp]											
[%saddrg]											
PSW											PUSH
											POP
SP	ADDWG										
	SUBWG										
post											PUSH
											POP
											PUSHU
											POPU
[TDE+]		(MOVW)						SACW			
byte											MACW
											MACSW

**Notes 1.** SUBW and CMPW are the same as ADDW.

- 2. Either the second operand is not used, or the second operation is not an operand address.
- 3. If saddr2 instead of saddr is used in this combination, the code length of some instructions is short.
- 4. MULUW and DIVUX are the same as MULW.

(3) 24-bit instructions ((): combination realized by using WHL as rg) MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

2nd Operand	# imm24	WHL	rg	saddrg	!!addr24	mem1	[%saddrg]	SP	None <sup>Note</sup>
			rg'						
1st Operand									
WHL	(MOVG)	(MOVG)	(MOVG)	(MOVG)	(MOVG)	MOVG	MOVG	MOVG	
	(ADDG)	(ADDG)	(ADDG)	ADDG					
	(SUBG)	(SUBG)	(SUBG)	SUBG					
rg	MOVG	(MOVG)	MOVG	MOVG	MOVG				INCG
	ADDG	(ADDG)	ADDG						DECG
	SUBG	(SUBG)	SUBG						PUSH
									POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG
									DECG

Note Either the second operand is not used, or the second operation is not an operand address.

## (4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

2nd Operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit iaddr16.bit	/saddr.bit /sfr.bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit	None <sup>Note</sup>
1st Operand		laddr24.bit	/!!addr24.bit	
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

**Note** Either the second operand is not used, or the second operation is not an operand address.

# (5) Call/return and branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Operand of	\$addr20	\$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None
instruction										ĺ		
address										Í		
Basic	BC <sup>Note</sup>	CALL	CALL	CALL	CALL	CALL	CALL	CALL	CALLF	CALLT	BRKCS	BRK
instruction	BR	BR	BR	BR	BR	BR	BR	BR		Í		RET
			RETCS							Í		RETI
			RETCSB							ĺ		RETB
Compound	BF											
instruction	вт									Í		
	BTCLR									Í		
	BFSET									Í		
	DBNZ									Í		

**Note** BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as BC.

# (6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT, EI, DI, SWRS

# 6. ELECTRICAL SPECIFICATIONS

# Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	Vdd	$ V_{DD} - AV_{DD1}  \le 0.5 V$	-0.5 to +7.0	V
	AV <sub>DD1</sub>	$ V_{DD} - AV_{DD2}  \le 0.5 V$	-0.5 to +7.0	V
	AV <sub>DD2</sub>	$  AV_{DD1} - AV_{DD2}   \le 0.5 V$	-0.5 to +7.0	V
	AV <sub>SS1</sub>		-0.5 to +0.5	V
	AVss2		-0.5 to +0.5	V
Input voltage	VI		-0.5 to VDD + 0.5	V
Analog input voltage	VIAN	$V_{DD} \ge AV_{DD2}$	-0.5 to AVDD2 + 0.5	V
(ANI0-ANI11)		VDD < AVDD2	-0.5 to VDD + 0.5	V
Output voltage	Vo		-0.5 to VDD + 0.5	V
Low-level output current	lol	Pin 1	15	mA
		Total of all pins	100	mA
High-level output current	Іон	Pin 1	-10	mA
		Total of all pins	-50	mA
Operating ambient temperature	TA		-10 to +70	°C
Storage temperature	Tstg		-65 to +150	°C

Caution If the rated value of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings therefore specify the values exceeding which the product may be physically damaged. Never exceed these values when using the product.

# **Operating Conditions**

Clock Frequency	Operating Ambient Temperature (TA)	Operating Conditions	Supply Voltage (VDD)
$4 \text{ MHz} \le \text{fxx} \le 16 \text{ MHz}$	-10 to +70°C	All functions	+4.5 to +5.5 V
		CPU function only	+4.0 to +5.5 V
32 kHz ≤ fx⊤ ≤ 35 kHz		Subclock operation	+2.7 to +5.5 V
		(CPU, watch, and port	
		functions only)	

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Crystal resonator		Oscillation frequency (fxx)	4	16	MHz

Oscillator Characteristics (main clock) (T<sub>A</sub> = -10 to  $+70^{\circ}$ C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

## Oscillator Characteristics (subclock) (T<sub>A</sub> = -10 to $+70^{\circ}$ C, V<sub>DD</sub> = AV<sub>DD</sub> = 2.7 to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Crystal resonator		Oscillation frequency (fxt)	32	35	kHz

- Caution When using the main system clock and subsystem clock oscillator, wire the portion enclosed by the broken line in the above figures as follows to avoid the adverse influence of wiring capacitance:
  - Keep the wiring length as short as possible.
  - Do not cross the wiring with the other signal lines. Do not route the wiring in the neighborhood of a signal line through which a high alternating current flows.
  - Always keep the ground point of the capacitor of the oscillator to the same potential as Vss. Do not ground the capacitor to a ground pattern to which a high current flows.
  - Do not extract signals from the oscillation circuit.

Exercise particular care in using the subsystem clock oscillator because the amplification factor of this circuit is kept low to reduce the current consumption.

**Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.
Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
Low-level input voltage	VIL1	Pins other th	an those listed in <b>Note 1</b> below	0		0.3 VDD	V
	VIL2	Pins listed in	Note 1 below	0		0.2 Vdd	V
	VIL3	X1, X2		0		0.4	V
High-level input voltage	VIH1	Pins other th	an those listed in <b>Note 1</b> below	0.7 Vdd		VDD	V
	VIH2	Pins listed in	n Note 1 below	0.8 Vdd		VDD	V
	VIH3	X1, X2		Vdd - 0.5		VDD	V
Low-level output voltage	V <sub>OL1</sub>	lo∟ = 8.0 mA	(pins in <b>Note 2</b> )			1.0	V
	V <sub>OL2</sub>	lo∟ = 5.0 mA	(pins in Note 4)			0.6	V
	Vol3	lo∟ = 2.0 mA	<u> </u>			0.45	V
	Vol4	IoL = 100 μA	l.			0.25	V
High-level output voltage	Vон1	Іон = -1.0 m	A	Vdd - 1.0			V
	Vон2	Іон = -100 <i>µ</i>	ιA	Vdd - 0.4			V
Input leakage current	Lu	$0 \le V_I \le V_{DD}$	$\leq V_{I} \leq V_{DD}$			±10	μA
Output leakage current	Ilo	$0 \le V_0 \le V_{DI}$	)			±10	μA
VDD supply current	DD1	Operation	fxx = 16 MHz		30	50	mA
		mode	fxx = 8 MHz (low-frequency os-				
			cillation mode)				
			Internally, 8 MHz main				
			clock operation				
			fxt = 32.768 kHz		50	80	μA
			Subclock operation (CPU,				
			watch, port)				
			$V_{DD} = 2.7 V$				
	DD2	HALT mode	fxx = 16 MHz		10	25	mA
			fxx = 8 MHz (low-frequency				
			oscillation mode)				
			Internally, 8 MHz main clock				
			operation				
			fxt = 32.768 MHz		25	50	μA
			Subclock operation (CPU,				
			watch, port)				
			VDD = 2.7 V				
Data hold voltage	Vdddr	STOP mode		2.5			V
Data hold current Note 3	Idddr	STOP mode	Subclock oscillates		18	50	μA
		$V_{DDDR} = 5.0 V$					
		STOP mode	Subclock oscillates		2.5	10	μA
		$V_{DDDR} = 2.7 V$					
		STOP mode	Subclock stops		0.2	7.0	μA
		$V_{DDDR} = 2.5 V$					
Pull-up resistor	R∟	V1 = 0 V		25	55	110	kΩ

## DC Characteristics (T<sub>A</sub> = -10 to $+70^{\circ}$ C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.5 to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

- Notes 1. RESET, IC, NMI, INTPO-INTP2, P61/SCK1/BUZ, P63/SI1, SCK2, SI2/BUSY, P65/HWIN, P91/KEY0 to P95/KEY4
  - 2. P40 to P47
  - **3.** In the STOP mode in which the subclock oscillation is stopped, disconnect the feedback resistor, and connect the XT1 pin to V<sub>DD</sub>.
  - **4.** P46, P47

## **AC Characteristics**

CPU and peripheral circuit operation clock (T<sub>A</sub> = -10 to +70°C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.5 to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol		Conditions		Unit
CPU operation clock cycle time	tськ	fxx = 16 MHz	$V_{DD} = AV_{DD} = 4.0$ to 5.5 V	125	ns
		CPU function only			
		fxx = 16 MHz			
		fxx = 8 MHz	low-frequency oscillation mode		
			(Bit 7 of CC = 1)		
Peripheral operation clock cycle time	tclk1	fxx = 16 MHz		125	ns
		fxx = 8MHz	low-frequency oscillation mode		
			(Bit 7 of CC = 1)		

#### Serial interface

(1) SIOn: n = 1 or 2 ( $T_A = -10$  to  $+70^{\circ}C$ ,  $V_{DD} = AV_{DD} = 4.5$  to 5.5 V,  $V_{SS} = AV_{SS} = 0$  V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Serial clock cycle time	<b>t</b> cysк	Input	External clock	1.0		μs
		Output	fclk1/8	1.0		μs
			fclk1/16	2.0		μs
			fclк1/32	4.0		μs
			fclk1/64	8.0		μs
			fclk1/128	16		μs
			fclk1/256	32		μs
Serial clock high- and low-level widths	twsкн	Input	External clock	420		ns
	twsĸ∟	Output	Internal clock	tсүsк/2 — 50		ns
SIn setup time (vs. SCKn ↑)	<b>t</b> sssk			100		ns
SIn hold time (vs. SCKn ↑ )	tнssк			400		ns
SOn output delay time (vs. $\overline{\text{SCKn}} \downarrow$ )	<b>t</b> dssk			0	300	ns

Remarks 1. fclk1: operating clock of peripheral circuit (8 MHz)

**2.** n = 1 or 2

## (2) SIO2 only ( $T_A = -10$ to $+70^{\circ}C$ , $V_{DD} = AV_{DD} = 4.5$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCK2(8) ↑→STRB ↑	<b>t</b> dstrb		twsкн	tсүsк	
Strobe high-level width	twstrb		tсүsк <b>– 30</b>	tсүзк + 30	ns
BUSY setup time	<b>t</b> sbusy		100		ns
(vs. BUSY detection timing)					
BUSY hold time	tнвusy		100		ns
(vs. BUSY detection timing)					
BUSY inactive → SCK2(1) ↓	<b>t</b> LBUSY			tcysk + twskн	

**Remarks 1.** The value in ( ) following  $\overline{SCK2}$  indicates the number of  $\overline{SCK2}$ .

- **2.** BUSY is detected after the time of  $(n + 2) \times \text{tcysk}$  (n = 0, 1, and so on) in respect to SCK2 (8)  $\uparrow$ .
- **3.** BUSY inactive  $\rightarrow \overline{\text{SCK2}}(1) \downarrow$  is the value when data has been completely written to SIO2.

	Parameter	Symbol	Standar	rd Mode	High-spe	ed Mode	Unit
			MIN.	MAX	MIN	MAX.	
SCL clock fr	CL clock frequency		0	100	0	400	kHz
Bus free tim	e (between stop and start	<b>t</b> BUF	4.7	-	1.3	-	μs
conditions)							
Hold time <sup>No</sup>	te 1	thd : sta	4.0	-	0.6	-	μs
SCL clock lo	ow-level width	tLOW	4.7	-	1.3	-	μs
SCL clock h	igh-level width	tніgн	4.0	_	0.6	_	μs
Start/restart condition setup time		tsu : sta	4.7	_	0.6	_	μs
Data hold	CBUS compatible master	thd : dat	5.0	-	-	_	μs
time	l <sup>2</sup> C bus		ONote 2	-	<sub>O</sub> Note 2	0.9 <sup>Note 2</sup>	μs
Data setup ti	me	tsu : dat	250	-	100 <sup>Note 4</sup>	-	ns
SDA and SC	L signal rise time	tĸ	-	1000	20+0.1Cb <sup>Note 5</sup>	300	ns
SDA and SC	L signal fall time	t⊧	_	300	20+0.1Cb <sup>Note 5</sup>	300	ns
Stop condition	on setup time	tsu : sto	4.0	_	0.6	—	μs
Pulse width	of spike restrained by input	tsp	-	-	0	50	ns
filter							
Each bus lin	e capacitative load	Cb		400	_	400	pF

## I<sup>2</sup>C bus mode (µPD784928Y subseries only)

Notes 1. The first clock pulse is generated at the start condition after this period.

- 2. The device needs to internally supply a hold time of at least 300 ns for the SDA signal to fill the undefined area at the falling edge of the SCL (VIHmin. of the SCL signal).
- **3.** Unless the device extends the low hold time (tLOW) of the SCL signal, it is necessary to fill only the maximum data hold time (tHD : DAT).
- 4. The high-speed mode I<sup>2</sup>C bus can be used in the standard mode I<sup>2</sup>C bus system. In this case, satisfy the following conditions:
  - When the device does not extend the low hold time of the SCL signal tsu :  $\mbox{dat} \geq 250 \mbox{ ns}$
  - When the device extends the low hold time of the SCL signal
    Send the next data bit to the SDA line before releasing the SCL line (tRmax. + tsu:DAT = 1000 + 250
    - = 1250 ns : in the standard mode I<sup>2</sup>C bus specification)
- 5. Cb: Total capacitance of one bus line (unit: pF)

## Other operations (T<sub>A</sub> = -10 to $+70^{\circ}$ C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.5 to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

F	Parameter	Symbol	С	ondition	MIN.	MAX.	Unit
Timer input sign	al low-level width	twc⊤∟	When DFGIN, CFC	GIN, DPGIN, REELOIN,	tclk1		ns
			or REEL1IN logic I	evel is input			
Timer input sign	al high-level width	twcтн	When DFGIN, CFC	GIN, DPGIN, REELOIN,	tclk1		ns
			or REEL1IN logic I	evel is input			
Timer input signal valid edge input cycle tPERIN When DFGIN, CFGIN, or DPGIN is inp		GIN, or DPGIN is input	2		μs		
CSYNCIN low-level width		twcr1L	When digital noise r	ejection circuit is not used	8tclk1		ns
			When digital noise	rejection circuit is used	108tcLK1		ns
			(Bit 4 of INTM2 = 0	))			
			When digital noise	rejection circuit is used	180tclk1		ns
			(Bit 4 of INTM2 = <sup>-</sup>	1)			
CSYNCIN high-l	evel width	twcr1H	When digital noise r	When digital noise rejection circuit is not used			ns
			When digital noise	rejection circuit is used	108tclk1		ns
			(Bit 4 of INTM2 = 0	))			
			When digital noise	rejection circuit is used	180tcLK1		ns
			(Bit 4 of INTM2 = $-$	1)			
Digital noise	Rejected pulse width	twsep	Bit 4 of INTM2 = 0			104tclk1	ns
rejection circuit			Bit 4 of INTM2 = 1			176tcLK1	ns
Passed pulse width			Bit 4 of INTM2 = 0		108tcLK1		ns
			Bit 4 of INTM2 = 1	Bit 4 of INTM2 = 1			ns
NMI low-level wi	dth	twnil	$V_{DD} = AV_{DD} = 2.7$ to 5.5 V		10		μs
NMI high-level w	vidth	twnih	$V_{DD} = AV_{DD} = 2.7$ to 5.5 V		10		μs
INTP0, INTP3 lo	w-level widths	twiplo			2tclk1		ns
INTP0, INTP3 hi	gh-level widths	twiph0			2tclk1		ns
INTP1, KEY0-KE	EY4 low-level widths	twipL1	Mode other than STOP mode		2tclk1		ns
			In STOP mode, for	releasing STOP mode	10		μs
INTP1, KEY0-KE	EY4 high-level widths	twiph1	Mode other than S	TOP mode	2tclk1		ns
			In STOP mode, for	releasing STOP mode	10		μs
INTP2 low-level	width	twipl2	In normal mode,	Sampling = fclk	2tcLK1		ns
			with main clock	Sampling = fclk/128	32Note		μs
			Normal mode,	Sampling = fclk	61		μs
			with subclock	Sampling = fcLK/128	7.9 <sup>Note</sup>		ms
			In STOP mode, for	releasing STOP mode	10		μs
INTP2 high-leve	el width	twiph2	In normal mode,	Sampling = fclk	2tclk1		ns
			with main clock	Sampling = fclk/128	32Note		μs
			Normal mode,	Sampling = fclk	61		μs
			with subclock	Sampling = fcLK/128	7.9 <sup>Note</sup>		ms
			In STOP mode, for	releasing STOP mode	10		μs
RESET low-leve	l width	twrsl			10		μs

**Note** If a high or low level is successively input two times during the sampling period, a high or low level is detected.

Remark tokut: operating clock cycle time of peripheral circuit (125 ns)

#### Clock output operation (TA = -10 to $+70^{\circ}$ C, VDD = AVDD = 4.5 to 5.5 V, Vss = AVss = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
CLO cycle time	tcyc∟	nT	125	16000	ns
CLO low-level width	tcll	tcvc∟/2 ± 25	37.5	8025	ns
CLO high-level width	tсьн	tcvc∟/2 ± 25	37.5	8025	ns
CLO rise time	<b>t</b> CLR			25	ns
CLO fall time	tclf			25	ns

Remarks 1. n: system clock division

2. T = 1/fclk

#### Data hold characteristics (TA = -10 to +70°C, VDD = AVDD = 2.5 to 5.5 V, Vss = AVss = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Low-level input voltage	VIL	Special pins (pins in Note)	0		0.1 Vdddr	V
High-level input voltage	VIH		0.9 VDDDR		VDDDR	V

Note RESET, IC, NMI, INTPO-INTP2, P61/SCK1/BUZ, P63/SI1, SCK2, SI2/BUSY, P65/HWIN, P91/KEY0-P95/ KEY4

#### Watch function (T<sub>A</sub> = -10 to $+70^{\circ}$ C, V<sub>DD</sub> = AV<sub>DD</sub> = 2.7 to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Subclock oscillation hold voltage	Vddxt		2.7		V
Hardware watch function operating voltage	Vddw		2.7		V

#### Subclock oscillation stop detection flag (TA = -10 to +70°C, VDD = AVDD = 4.5 to 5.5 V, Vss = AVss = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Oscillation stop detection width	toscr		45		μs

#### A/D converter characteristics (T<sub>A</sub> = -10 to +70°C, V<sub>DD</sub> = AV<sub>DD</sub> = AV<sub>REF</sub> = 4.5 to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			8			bit
Total error		AVREF = VDD			2.0	%
Quantization error					±1/2	LSB
Conversion time	tconv	Bit 4 of ADM = 0	160tclk1			μs
		Bit 4 of ADM = 1	80tclk1			μs
Sampling time	<b>t</b> samp	Bit 4 of ADM = 0	32tcLK1			μs
		Bit 4 of ADM = 1	16tclk1			μs
Analog input voltage	VIAN		0		AVREF	V
Analog input impedance	ZAN			1000		MΩ
AVREF current	AIREF			0.4	1.2	mA

## VREF amplifier (T<sub>A</sub> = $25^{\circ}$ C, V<sub>DD</sub> = AV<sub>DD</sub> = 5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reference voltage	VREF		2.35	2.50	2.65	V
Charge current	Існа	Sets AMPM0.0 to 1	300			μA
		(pins in <b>Note</b> )				

Note RECCTL+, RECCTL-, CFGIN, CFGCPIN, DFGIN, DPGIN, CSYNCIN, REEL0IN, REEL1IN

## CTL amplifier (TA = $25^{\circ}$ C, VDD = AVDD = 5 V, Vss = AVss = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CTL+, – input resistance	RICTL		2	5	10	kΩ
Feedback resistance	RFCTL		20	50	100	kΩ
Bias resistance	RBCTL		20	50	100	kΩ
Minimum voltage gain	GCTLMIN		17	20	22	dB
Maximum voltage gain	GCTLMAX		71	75		dB
Gain selecting step	Sgain			1.77		dB
Same phase signal elimination ratio	CMR	DC, voltage gain: 20 dB		50		dB
High comparator set voltage of waveform shaping	VPBCTLHS		VREF + 0.47	Vref + 0.50	Vref + 0.53	V
High comparator reset voltage of waveform shaping	VPBCTLHR		VREF + 0.27	Vref + 0.30	Vref + 0.33	V
Low comparator set voltage of waveform shaping	VPBCTLLS		Vref - 0.53	Vref - 0.50	Vref - 0.47	V
Low comparator reset voltage of waveform shaping	VPBCTLLR		V <sub>REF</sub> - 0.33	Vref - 0.30	Vref - 0.27	V
Comparator Schmitt width of waveform shaping	VPBSH		150	200	250	mV
High comparator voltage of CTL flag S	VFSH		VREF + 1.00	Vref + 1.05	Vref + 1.10	V
Low comparator voltage of CLT flag S	VFSL		VREF - 1.10	Vref - 1.05	Vref - 1.00	V
High comparator voltage of CTL flag L	VFLH		VREF + 1.40	Vref + 1.45	Vref + 1.50	V
Low comparator voltage of CTL flag L	Vfll		Vref - 1.50	Vref – 1.45	Vref - 1.40	V

CFG amplifier (AC coupling) (T<sub>A</sub> =  $25^{\circ}$ C, V<sub>DD</sub> = AV<sub>DD</sub> = 5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage gain 1	GCFG1	fi = 2 kHz, open loop	50			dB
Voltage gain 2	GCFG2	fi = 30 kHz, open loop	34			dB
CFGAMPO High-level output current	Іонсға	DC	-1			mA
CFGAMPO Low-level output current	IOLCFG	DC	0.1			mA
High comparator voltage	Vcfgh		V <sub>REF</sub> + 0.09	VREF + 0.12	VREF + 0.15	V
Low comparator voltage	VCFGL		Vref - 0.15	V <sub>REF</sub> – 0.12	Vref - 0.09	V
Duty accuracy	PDUTY	Note	49.7	50.0	50.3	%

Note The conditions include the following circuit and input signal.

Input signal : Sine wave input (5 mV\_{p-p})  $f_i = 1 \ kHz$  Voltage gain: 50 dB



DFG amplifier (AC coupling) (T<sub>A</sub> =  $25^{\circ}$ C, V<sub>DD</sub> = AV<sub>DD</sub> = 5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage gain	Gdfg	fi = 900 Hz, open loop	50			dB
Feedback resistance	RFDFG		160	400	640	kΩ
Input protection resistance	RIDFG			150		Ω
High comparator voltage	Vdfgh		Vref + 0.07	Vref + 0.10	VREF + 0.14	V
Low comparator voltage	VDFGL		VREF - 0.14	VREF - 0.10	Vref - 0.07	V

Caution Set the input resistance connected to the DFGIN pin to 16 k $\Omega$  or below. Connecting a resistor exceeding that value may cause the DFG amp to oscillate.

## DPG amplifier (AC coupling) ( $T_A = 25^{\circ}C$ , $V_{DD} = AV_{DD} = 5 V$ , $V_{SS} = AV_{SS} = 0 V$ )

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage gain	Gdpg	fi = 30 Hz		20		dB
High comparator voltage	VDPGH1	SELDPGHL0 = 0, SELDPGHL1 = 0	VREF + 0.02	Vref + 0.05	Vref + 0.08	V
	Vdpgh2	SELDPGHL0 = 1, SELDPGHL1 = 0	VREF + 0.56	Vref + 0.60	Vref + 0.64	V
	Vdpgh3	SELDPGHL0 = 0, SELDPGHL1 = 1	VREF - 0.44	Vref - 0.40	Vref - 0.36	V
Low comparator voltage	VDPGL1	SELDPGHL0 = 0, SELDPGHL1 = 0	Vref - 0.08	Vref – 0.05	Vref - 0.02	V
	VDPGL2	SELDPGHL0 = 1, SELDPGHL1 = 0	Vref + 0.36	Vref + 0.40	Vref + 0.44	V
	<b>V</b> DPGL3	SELDPGHL0 = 0, SELDPGHL1 = 1	VREF - 0.64	Vref – 0.60	Vref - 0.56	V

## Caution When both the SELDPGHL0 and SELDPGHL1 are set to 0, the DPG amplifier is not used. Therefore, be sure to set AMPC.7 (ENDPG) to 0.

## Ternary separation circuit (TA = 25°C, VDD = AVDD = 5 V, Vss = AVss = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input impedance	ZIPFG		20	50	100	kΩ
High comparator voltage	Vpfgh		Vref + 0.5	Vref + 0.7	Vref + 0.9	V
Low comparator voltage	VPFGL		VREF - 1.4	VREF - 1.2	VREF - 1.0	V

## CSYNC comparator (AC coupling) ( $T_A = 25^{\circ}C$ , $V_{DD} = AV_{DD} = 5 V$ , $V_{SS} = AV_{SS} = 0 V$ )

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input impedance	ZICSYN		20	50	100	kΩ
High comparator voltage	Vcsynh		VREF + 0.07	Vref + 0.10	VREF + 0.13	V
Low comparator voltage	VCSYNL		Vref – 0.13	Vref - 0.10	Vref - 0.07	V

## Reel FG comparator (AC coupling) (T<sub>A</sub> = 25°C, V<sub>DD</sub> = AV<sub>DD</sub> = 5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input impedance	Zirlfg		20	50	100	kΩ
High comparator voltage	Vrlfgh		VREF + 0.02	VREF + 0.05	VREF + 0.08	V
Low comparator voltage	Vrlfgl		Vref - 0.08	Vref - 0.05	Vref - 0.02	V

## **RECCTL driver** (T<sub>A</sub> = $25^{\circ}$ C, V<sub>DD</sub> = AV<sub>DD</sub> = 5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RECCTL+, - high-level output voltage	VCHREC	Іон = −4 mА	Vdd - 0.8			V
RECCTL+, - low-level output voltage	VOLREC	lol = 4 mA			0.8	V
CTLDLY internal resistance	RстL		40	70	140	kΩ
CTLDLY charge current	Іонсті	Use of internal resistor	-3			mA
CTLDLY discharge current	IOLCTL		-3			mA

## **Timing waveform**

AC timing test point



Serial transfer timing (SIOn: n = 1 or 2)



## Serial transfer timing (SIO2 only)

No busy processing



Continuation of busy processing



End of busy processing



Caution When an external clock is selected as the serial clock, do not use the busy control or strobe control.

 $I^2C$  bus mode ( $\mu$ PD784928Y subseries only)



## Super timer unit input timing



## Interrupt request input timing



## **Reset input timing**



## **Clock output timing**



## 7. PACKAGE DRAWING

## 100 PIN PLASTIC LQFP (FINE PITCH) (14×14)





Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
Α	16.00±0.20	0.630±0.008
в	14.00±0.20	0.551 <b>+0.009</b> -0.008
С	14.00±0.20	$0.551\substack{+0.009\\-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
н	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
к	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
М	$0.17\substack{+0.03 \\ -0.07}$	0.007+0.001 -0.003
Ν	0.08	0.003
Р	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	3°+7° -3°	3°+7° -3°
S	1.60 MAX.	0.063 MAX.
		S100GC-50-8EU

**Remark** The package dimensions and materials of ES versions are the same as those of mass-production versions.

## 100PIN PLASTIC QFP (14x20)





detail of lead end

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## NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
Α	23.6±0.4	0.929±0.016
В	20.0±0.2	$0.795 \substack{+0.009 \\ -0.008}$
С	14.0±0.2	$0.551\substack{+0.009\\-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
Н	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
К	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
М	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
Р	2.7±0.1	$0.106\substack{+0.005\\-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.
	F	P100GF-65-3BA1-3

**Remark** The package dimensions and materials of ES versions are the same as those of mass-production versions.

## 8. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions. For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

#### Table 8-1. Surface Mount Type Soldering Conditions

 (1) μPD784927GF-xxx-3BA : 100-pin plastic QFP (14 × 20 mm) μPD784928GF-xxx-3BA : 100-pin plastic QFP (14 × 20 mm) μPD784927YGF-xxx-3BA : 100-pin plastic QFP (14 × 20 mm) μPD784928YGF-xxx-3BA : 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 secs. max. (210°C min.), Number of times: three times max.	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 secs. max. (200°C min.), Number of times: three times max.	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 secs. max., Number of times: once, Preheating temperature: 120°C max.(Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 350°C max., Time: three secs. max. (per device side)	—

Caution Do not use two or more soldering methods in combination (except partial heating).

## ★ (2) μPD784927GF-∞∞-3BA-A : 100-pin plastic QFP (14 × 20 mm) μPD784928GF-∞∞-3BA-A : 100-pin plastic QFP (14 × 20 mm) μPD784927YGF-∞∞-3BA-A : 100-pin plastic QFP (14 × 20 mm) μPD784928YGF-∞∞-3BA-A : 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Wave soldering	For details, contact an NEC Electronics sales representative.	—
Partial heating	Pin temperature: 350°C max., Time: 3 seconds. max. (per pin row))	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

## Caution Do not use different soldering methods together (except for partial heating).

**Remark** Products that have the part numbers suffixed by "-A" are lead-free products.

## APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the  $\mu$ PD784927. Refer to (5) Cautions when the development tools are used.

#### (1) Language processing software

RA78K4	78K/IV series common assembler package
CC78K4	78K/IV series common C compiler package
DF784928	Device file for the $\mu$ PD784928, 784928Y subseries
CC78K4-L	78K/IV series common C compiler library source file

#### (2) Flash memory writing tools

Flashpro II, III	Dedicated flash programmer
(Part number: FL-PR2,	
FL-PR3, PG-FPIII)	
FA-100GC	Adapter for writing 100-pin plastic LQFP (GC-8EU type) flash memory. Be sure to
	connect depending on the target product.
FA-100GF	Adapter for writing 100-pin plastic QFP (GF-3BA type) flash memory. Be sure to
	connect depending on the target product.

## (3) Debugging tools

## • When using the IE-78K4-NS in-circuit emulator

	IE-78K4-NS	78K/IV series common in-circuit emulator
	IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
	IE-70000-98-IF-C	Interface adapter necessary when a PC-9800 series computer (except notebook personal computer) is used as host machine (C bus compatible)
*	IE-70000-CD-IF-A	PC card and interface cable necessary when a notebook personal computer is used as host machine (PCMCIA socket compatible)
	IE-70000-PC-IF-C	Interface adapter necessary when an IBM PC/AT <sup>™</sup> compatible machine is used as host machine (ISA bus compatible)
	IE-784928-NS-EM1	Emulation board for emulating the $\mu$ PD784928, 784928Y subseries
	EP-784915-GF-R	Emulation probe for $\mu$ PD784915 subseries common 100-pin plastic QFP (GC-3BA type) and 100-pin plastic LQFP (GC-8EU type).
	EV-9200GF-100	Conversion socket to be mounted on the board of the target system for 100-pin plastic QFP (GF-3BA type). It is used in LCC system.
	NQPACK100RB	Conversion socket to be mounted on the board of the target system for 100-pin plastic QFP (GF-3BA type). It is used in QFP system.
	ID78K4-NS	Integrated debugger for IE-78K4-NS
	SM78K4	78K/IV series common system simulator
	DF784928	Device file for the $\mu$ PD784928, 784928Y subseries

## • When using the IE-784000-R in-circuit emulator

IE-784000-R	78K/IV series common in-circuit emulator
IE-70000-98-IF-C	Interface adapter necessary when a PC-9800 series computer (except notebook personal computer) is used as host machine (C bus compatible)
IE-70000-PC-IF-C	Interface adapter necessary when an IBM PC/AT compatible machine is used as host machine (ISA bus compatible)
IE-78000-R-SV3	Interface adapter and cable necessary when an EWS is used as host machine
IE-784928-NS-EM1 IE-784915-R-EM1	Emulation board for emulating the $\mu PD784928,784928Y$ subseries and $\mu PD784915$ subseries
IE-784000-R-EM	78K/IV series common emulation board
IE-78K4-R-EX3	Conversion board for 100-pin products necessary when the IE-784928-NS-EM1 is used in the IE-784000-R. Not necessary when the IE-784915-R-EM1 is used.
EP-784915-GF-R	Emulation probe for $\mu$ PD784915 subseries common 100-pin plastic QFP (GC-3BA type) and 100-pin plastic LQFP (GC-8EU type).
EV-9200GF-100	Conversion socket to be mounted on the board of the target system for 100-pin plastic QFP (GF-3BA type). It is used in LCC system.
NQPACK100RB	Conversion socket to be mounted on the board of the target system for 100-pin plastic QFP (GF-3BA type). It is used in QFP system.
ID78K4	Integrated debugger for IE-784000-R
SM78K4	78K/IV series common system simulator
DF784928	Device file for the $\mu$ PD784928, 784928Y subseries

## (4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV series
MX78K4	OS for 78K/IV series

## (5) Cautions when the development tools are used

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784928.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 and DF784928.
- FL-PR2, FL-PR3, FA-100GC, and FA-100GF are products of Naito Densei Machida Mfg. Co., Ltd. (TEL: 044-822-3813). Contact an NEC distributor when purchasing these products.
- NQPACK100RB is a product of Tokyo Eletech Corp.
  Reference: Daimaru Kogyo, Ltd. Electronics Dept. (TEL: Tokyo 03-3820-7112)
  Electronics 2nd Dept. (TEL: Osaka 06-6244-6672)

Electronics 2nd Dept. (TEL: Osaka 06-6244-6

Host machines and OSs compatible with the software are as follows:

Host Machine [OS]	PC	EWS
	PC-9800 Series [Windows <sup>™</sup> ] IBM PC/AT compatible machines	HP9000 series 700 <sup>™</sup> [HP-UX <sup>™</sup> ] SPARCstation <sup>™</sup> [SunOS <sup>™</sup> , Solaris <sup>™</sup> ]
Software	[Japanese/English Windows]	NEWS™ (RISC) [NEWS-OS™]
RA78K4	O <sup>Note</sup>	0
CC78K4	O <sup>Note</sup>	0
ID78K4-NS	0	_
ID78K4	0	0
SM78K4	0	-
RX78K/IV	O <sup>Note</sup>	0
MX78K4	O <sup>Note</sup>	0

Note DOS based software

## APPENDIX B. RELATED DOCUMENTS

The documents referred to in this publication may include preliminary versions. However, preliminary versions are not marked as such.

#### **Device-related documents**

Document	Document No.	
	Japanese	English
$\mu$ PD784928, 784928Y Subseries User's Manual - Hardware	U12648J	U12648E
μPD784927, 784928, 784927Y, 784928Y Data Sheet	U12255J	This document
$\mu$ PD784928 Subseries Special Function Register Table	U12798J	-
µPD78F4928 Preliminary Product Information	U12188J	U12188E
$\mu$ PD784928Y Subseries Special Function Register Table	U12719J	-
µPD78F4928Y Preliminary Product Information	U12271J	U12271E
µPD784915, 784928, 784928Y Subseries Application Note - VCR Servo	U11361J	U11361E
78K/IV Series User's Manual - Instruction	U10905J	U10905E
78K/IV Series Instruction Table	U10594J	-
78K/IV Series Instruction Set	U10595J	_
78K/IV Series Application Note - Software Basics	U10095J	U10095E

## Development tool-related documents (User's Manuals)

Document		Document No.	
		Japanese	English
RA78K4 Assembler Package	Operation	U11334J	U11334E
	Language	U11162J	U11162E
RA78K4 Structured Assembler Preprocesso	or	U11743J	U11743E
CC78K4 C Compiler	Operation	U11572J	U11572E
	Language	U11571J	U11571E
IE-78K4-NS		U13356J	U13356E
IE-784000-R		U12903J	EEU-1534
IE-784928-NS-EM1		U13819J	U13819E
IE-784915-R-EM1, EP-784915GF-R		U10931J	U10931E
SM78K4 System Simulator Windows Based	Reference	U10093J	U10093E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K4-NS Integrated Debugger	Reference	U12796J	U12796E
ID78K4 Integrated Debugger Windows Based	Reference	U10440J	U10440E
ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS Based	Reference	U11960J	U11960E

# Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of the document when designing your system.

#### Embedded software-related documents (User's Manual)

Document		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Fundamental	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	_
78K/IV Series OS, MX78K4	Fundamental	U11779J	-

#### **Other Related Documents**

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products and Packages -	X13769X
Semiconductor Device Mount Manual	Note
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the "Semiconductor Device Mount Manual" website (http://www.necel.com/pkg/en/mount/index.html)

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## NOTES FOR CMOS DEVICES -

#### **1** VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

## **(2)** HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

## **③** PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

## **④** STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

#### 5 POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

## 6 INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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