

74HC138; 74HCT138

3-to-8 line decoder/demultiplexer; inverting

Rev. 4 — 27 June 2012

Product data sheet

1. General description

The 74HC138; 74HCT138 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC138; 74HCT138 decoder accepts three binary weighted address inputs (A_0 , A_1 and A_2) and when enabled, provides 8 mutually exclusive active LOW outputs (\bar{Y}_0 to \bar{Y}_7).

The 74HC138; 74HCT138 features three enable inputs: two active LOW (\bar{E}_1 and \bar{E}_2) and one active HIGH (E_3). Every output is HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74HC138; 74HCT138 to a 1-of-32 (5 lines to 32 lines) decoder with just four 74HC138; 74HCT138 ICs and one inverter.

The 74HC138; 74HCT138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Permanently tie unused enable inputs to their appropriate active HIGH- or LOW-state.

The 74HC138; 74HCT138 is identical to the 74HC238; 74HCT238 but has inverting outputs.

2. Features and benefits

- Demultiplexing capability
- Multiple input enable for easy expansion
- Complies with JEDEC standard no. 7A
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- ESD protection:
 - ◆ HBM EIA/JESD22-A114F exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$



3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74HC138N | -40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74HCT138N | | | | |
| 74HC138D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74 HCT138D | | | | |
| 74HC138DB | -40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HCT138DB | | | | |
| 74HC138PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT138PW | | | | |
| 74HC138BQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |
| 74HCT138BQ | | | | |

4. Functional diagram

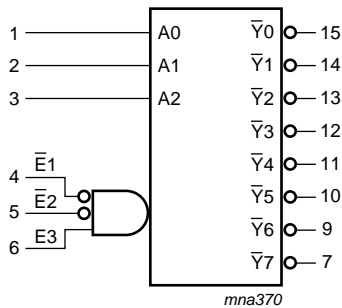


Fig 1. Logic symbol

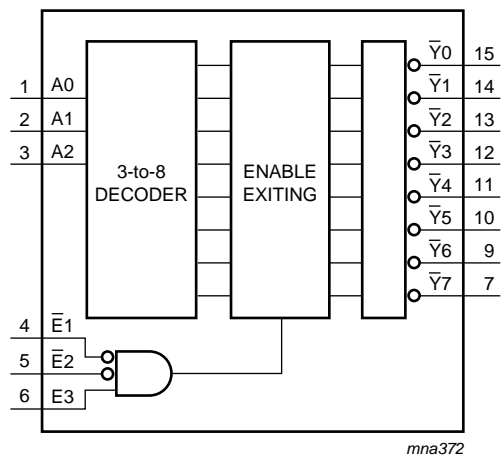


Fig 2. Functional diagram

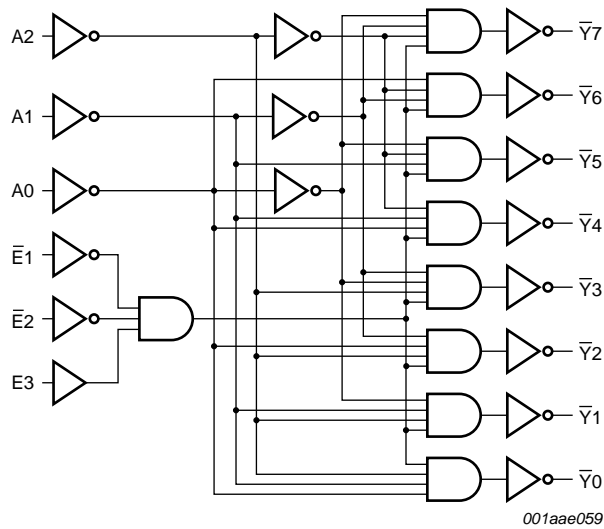


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

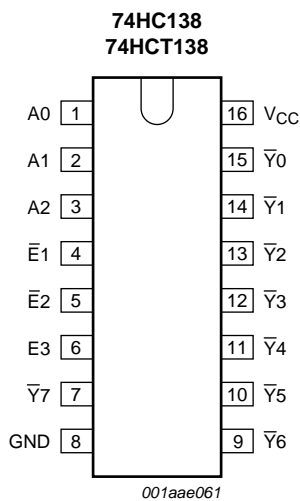
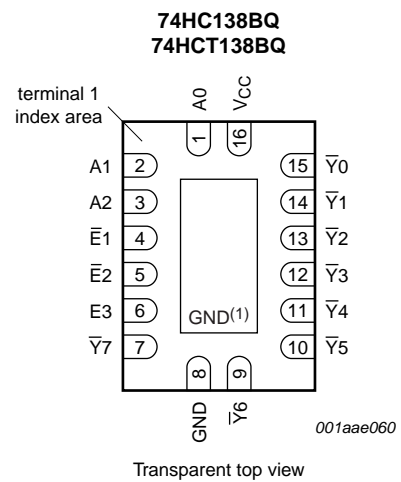


Fig 4. Pin configuration DIP16, SO16, SSOP16 and TSSOP16



- (1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as supply pin or input.

Fig 5. Pin configuration DHVQFN16

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--|------------------------------|--|
| A0, A1, A2 | 1, 2, 3 | address input A0, A1, A2 |
| $\bar{E}1, \bar{E}2$ | 4, 5 | enable input $\bar{E}1, \bar{E}2$ (active LOW) |
| E3 | 6 | enable input E3 (active HIGH) |
| $\bar{Y}0, \bar{Y}1, \bar{Y}2, \bar{Y}3, \bar{Y}4, \bar{Y}5, \bar{Y}6, \bar{Y}7$ | 15, 14, 13, 12, 11, 10, 9, 7 | output $\bar{Y}0, \bar{Y}1, \bar{Y}2, \bar{Y}3, \bar{Y}4, \bar{Y}5, \bar{Y}6, \bar{Y}7$ (active LOW) |
| GND | 8 | ground (0 V) |
| V _{CC} | 16 | positive supply voltage |

6. Functional description

Table 3. Function table^[1]

| Control | | | Input | | | Output | | | | | | | |
|------------|------------|----|-------|----|----|------------|------------|------------|------------|------------|------------|------------|------------|
| $\bar{E}1$ | $\bar{E}2$ | E3 | A2 | A1 | A0 | $\bar{Y}7$ | $\bar{Y}6$ | $\bar{Y}5$ | $\bar{Y}4$ | $\bar{Y}3$ | $\bar{Y}2$ | $\bar{Y}1$ | $\bar{Y}0$ |
| H | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | | | | | | | | | | | |
| X | X | L | | | | | | | | | | | |
| L | L | H | L | L | L | H | H | H | H | H | H | H | L |
| | | | L | L | H | H | H | H | H | H | H | L | H |
| | | | L | H | L | H | H | H | H | H | L | H | H |
| | | | L | H | H | H | H | H | H | L | H | H | H |
| | | | H | L | L | H | H | H | L | H | H | H | H |
| | | | H | L | H | H | H | L | H | H | H | H | H |
| | | | H | H | L | H | L | H | H | H | H | H | H |
| | | | H | H | H | L | H | H | H | H | H | H | H |

[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|--------------------------|---|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7 | V |
| I _{IK} | input clamping current | V _I < -0.5 V or V _I > V _{CC} + 0.5 V | - | ±20 | mA |
| I _{OK} | output clamping current | V _O < -0.5 V or V _O > V _{CC} + 0.5 V | - | ±20 | mA |
| I _O | output current | V _O = -0.5 V to (V _{CC} + 0.5 V) | - | ±25 | mA |
| I _{CC} | quiescent supply current | | - | 50 | mA |
| I _{GND} | ground current | | - | -50 | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|------------|-------|-----|------|
| P _{tot} | total power dissipation | | | | |
| | DIP16 package | | [1] - | 750 | mW |
| | SO16 package | | [2] - | 500 | mW |
| | SSOP16 package | | [3] - | 500 | mW |
| | TSSOP16 package | | [3] - | 500 | mW |
| | DHVQFN16 package | | [4] - | 500 | mW |

- [1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
- [2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
- [3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
- [4] For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC138 | | | 74HCT138 | | | Unit |
|------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | T _{amb} = -40 °C to +125 °C | | Unit |
|-----------------|--------------------------|-------------------------|--------------------------|-----|------|-------------------------------------|------|--------------------------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC138 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | T _{amb} = -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|---|--------------------------|------|------|-------------------------------------|------|--------------------------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | I _O = -5.2 mA; V _{CC} = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{OZ} | OFF-state output current | per input pin; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 6.0 V; I _O = 0 A | | | | ±0.5 | - | ±5.0 | - | ±10 |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| C _I | input capacitance | | - | 3.5 | - | | | | | pF |

74HCT138

| | | | | | | | | | | |
|-----------------|---------------------------|---|------|------|------|------|------|------|------|-----|
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{OZ} | OFF-state output current | per input pin; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A | | | | ±0.5 | - | ±5.0 | - | ±10 |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 8.0 | - | 80 | - | 160 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | T _{amb} = -40 °C to +125 °C | | Unit | |
|------------------|---------------------------|---|----------------------------------|-----|-----|-------------------------------------|-----|--------------------------------------|-----|-------|----|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A | per input pin; An inputs | - | 150 | 540 | - | 675 | - | 735 | μA |
| | | | per input pin; $\bar{E}n$ inputs | - | 125 | 450 | - | 562.5 | - | 612.5 | μA |
| | | | per input pin; E3 input | - | 100 | 360 | - | 450 | - | 490 | μA |
| C _I | input capacitance | | - | 3.5 | - | | | | | pF | |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see [Figure 8](#).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | T _{amb} = -40 °C to +125 °C | | Unit |
|--------|-----------|------------|--------------------------|-----|-----|-------------------------------------|-----|--------------------------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |

For type 74HC138

| | | | | | | | | | | |
|---|-------------------------------|--|----|----|-----|---|-----|----|-----|----|
| t _{pd} | propagation delay | An to $\bar{Y}n$; see Figure 6 ^[1] | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 41 | 150 | - | 190 | - | 225 | ns |
| | | V _{CC} = 4.5 V | - | 15 | 30 | - | 38 | - | 45 | ns |
| | | V _{CC} = 5 V; C _L = 15 pF | - | 12 | - | - | - | - | - | ns |
| | | V _{CC} = 6.0 V | - | 12 | 26 | - | 33 | - | 38 | ns |
| | | E3 to $\bar{Y}n$; see Figure 6 ^[1] | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 47 | 150 | - | 190 | - | 225 | ns |
| | | V _{CC} = 4.5 V | - | 17 | 20 | - | 38 | - | 45 | ns |
| | | V _{CC} = 5 V; C _L = 15 pF | - | 14 | - | - | - | - | - | ns |
| | | V _{CC} = 6.0 V | - | 14 | 26 | - | 33 | - | 38 | ns |
| | | $\bar{E}n$ to $\bar{Y}n$; see Figure 7 ^[1] | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 47 | 150 | - | 190 | - | 225 | ns |
| V _{CC} = 4.5 V | - | 17 | 20 | - | 38 | - | 45 | ns | | |
| V _{CC} = 5 V; C _L = 15 pF | - | 14 | - | - | - | - | - | ns | | |
| V _{CC} = 6.0 V | - | 14 | 26 | - | 33 | - | 38 | ns | | |
| t _t | transition time | $\bar{Y}n$; see Figure 6 and Figure 7 ^[2] | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | V _{CC} = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | V _{CC} = 6.0 V | - | 6 | 13 | - | 16 | - | 19 | ns |
| C _{PD} | power dissipation capacitance | C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} ^[3] | - | 67 | - | - | - | - | - | pF |

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 8](#).

| Symbol | Parameter | Conditions | $T_{amb} = 25\text{ }^\circ\text{C}$ | | | $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ | | $T_{amb} = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ | | Unit |
|--------------------------|--|--|--|-----|-----|---|-----|--|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| For type 74HCT138 | | | | | | | | | | |
| t_{pd} | propagation delay | An to \bar{Y}_n ; see Figure 6 [1] | | | | | | | | |
| | | $V_{CC} = 4.5\text{ V}$ | - | 20 | 35 | - | 44 | - | 53 | ns |
| | | $V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$ | - | 17 | - | - | - | - | - | ns |
| | E3 to \bar{Y}_n ; see Figure 6 [1] | $V_{CC} = 4.5\text{ V}$ | - | 18 | 40 | - | 50 | - | 60 | ns |
| | | $V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$ | - | 19 | - | - | - | - | - | ns |
| | \bar{E}_n to \bar{Y}_n ; see Figure 7 [1] | $V_{CC} = 4.5\text{ V}$ | - | 19 | 40 | - | 50 | - | 60 | ns |
| | | $V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$ | - | 19 | - | - | - | - | - | ns |
| | t_t | transition time | \bar{Y}_n ; see Figure 6 and Figure 7 [2] | | | | | | | |
| $V_{CC} = 4.5\text{ V}$ | | | - | 7 | 15 | - | 19 | - | 22 | ns |
| C_{PD} | power dissipation capacitance | $C_L = 50\text{ pF}; f = 1\text{ MHz}; V_1 = \text{GND to } V_{CC}$ [3] | - | 67 | - | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

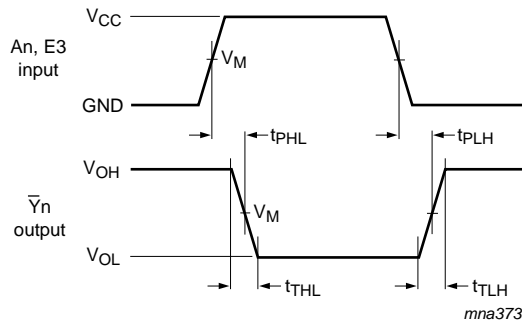
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

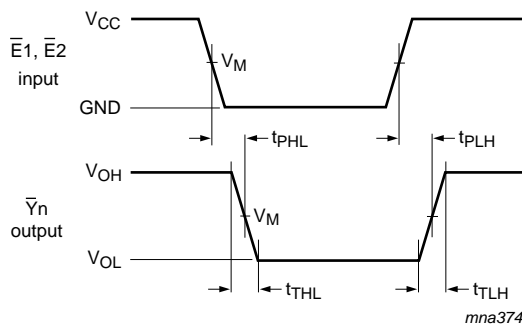
11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay input (A_n) and enable input (E_3) to output (\bar{Y}_n) and transition time output (\bar{Y}_n)



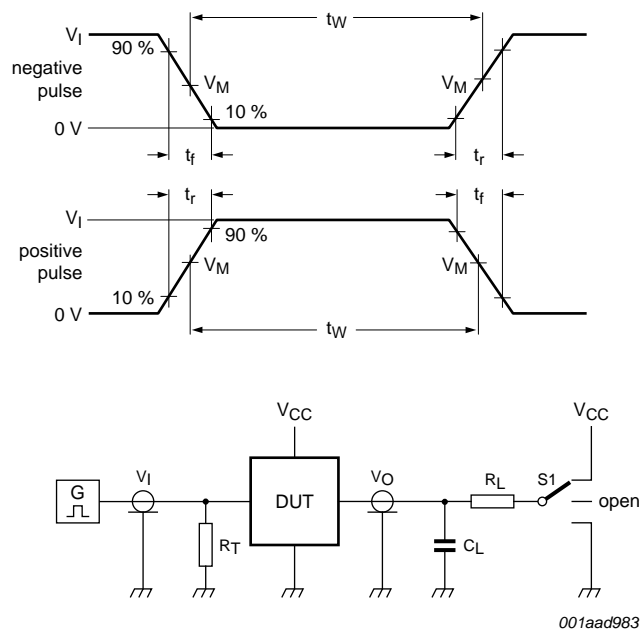
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Propagation delay enable input (\bar{E}_n) to output (\bar{Y}_n) and transition time output (\bar{Y}_n)

Table 8. Measurement points

| Type | Input | Output |
|----------|-------------|-------------|
| | V_M | V_M |
| 74HC138 | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT138 | 1.3 V | 1.3 V |



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 8. Load circuitry for measuring switching times

Table 9. Test data

| Type | Input | | Load | | S1 position | | |
|----------|----------|------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74HC138 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74HCT138 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

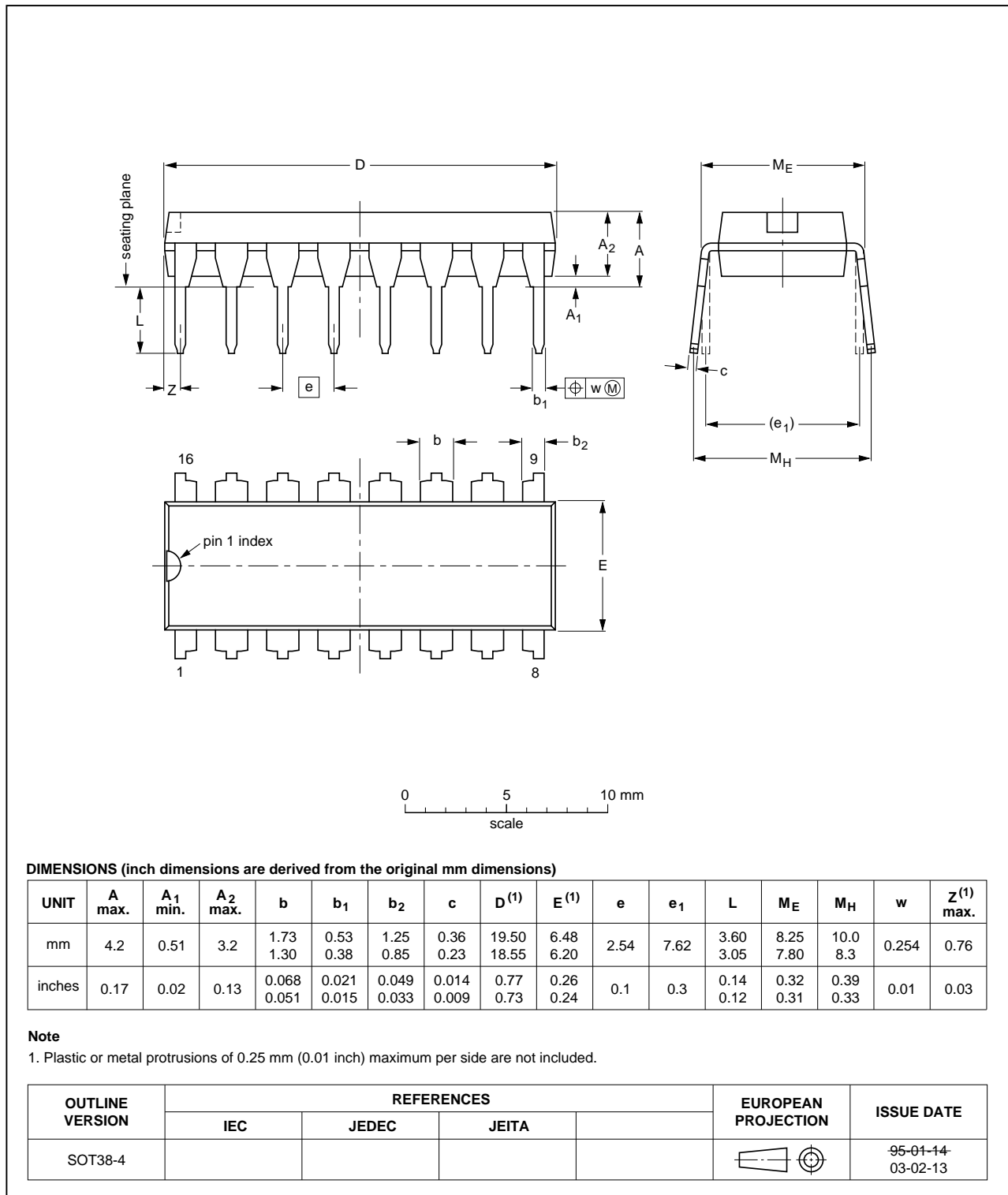


Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

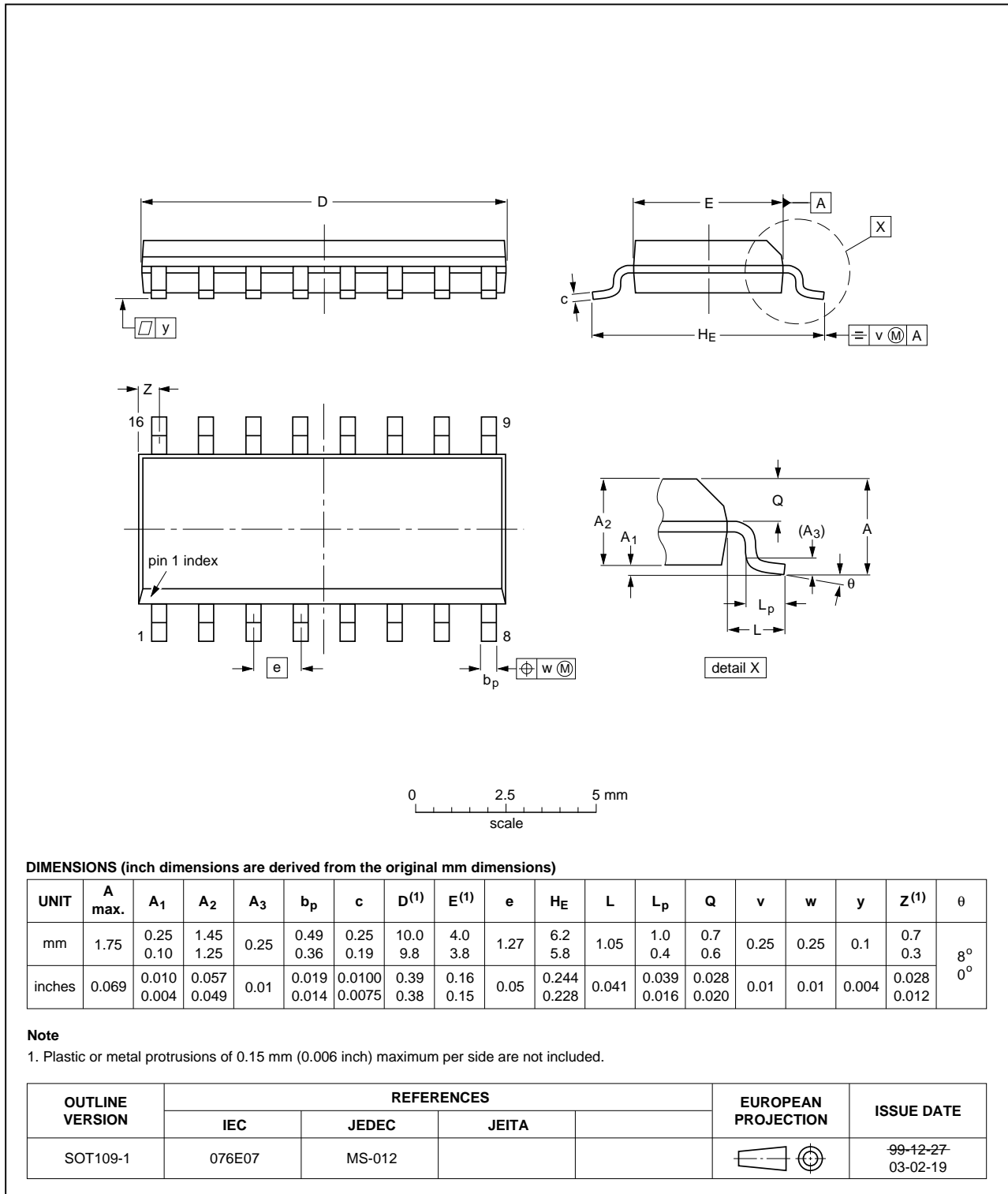


Fig 10. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

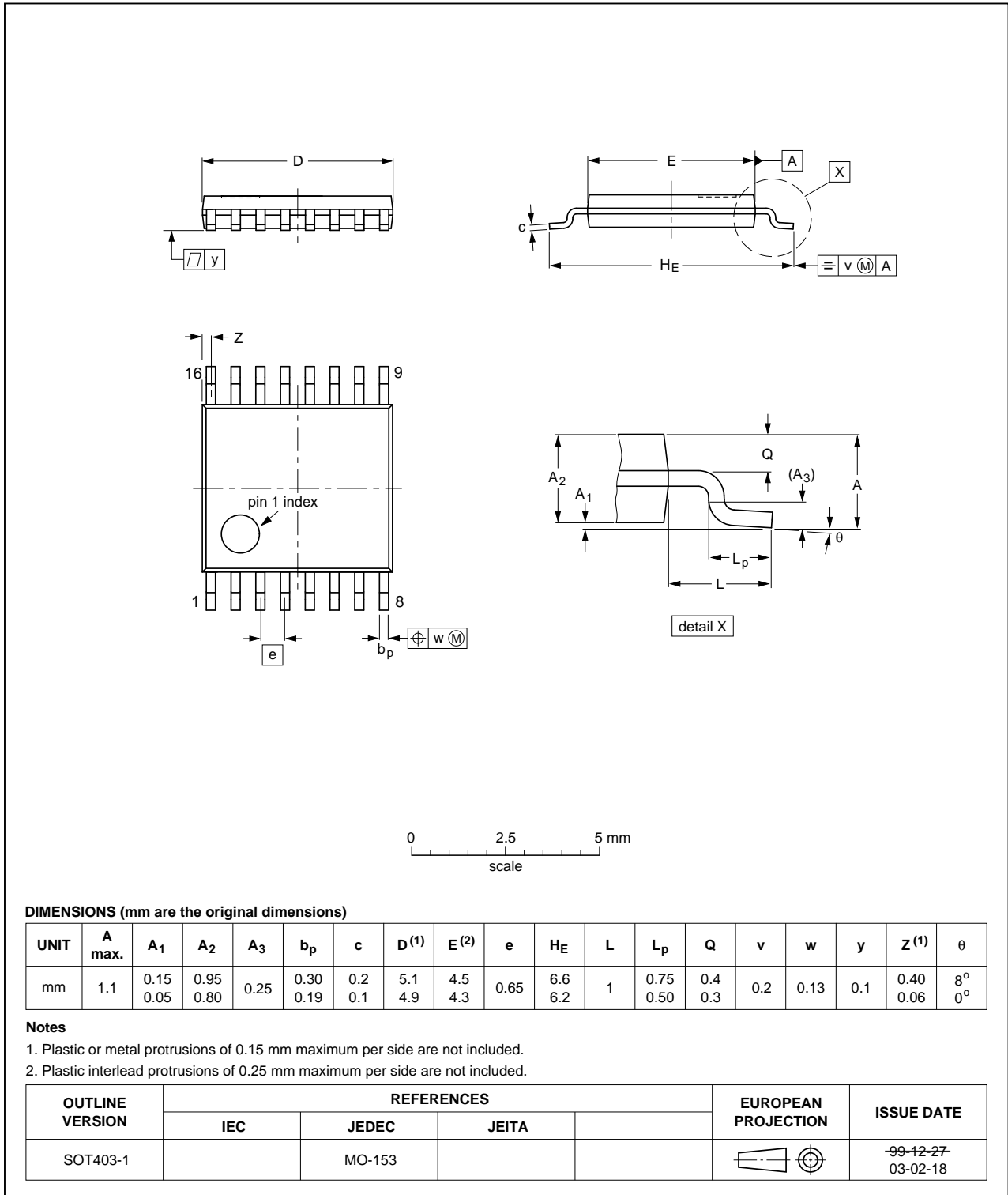


Fig 11. Package outline SOT403-1 (TSSOP16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

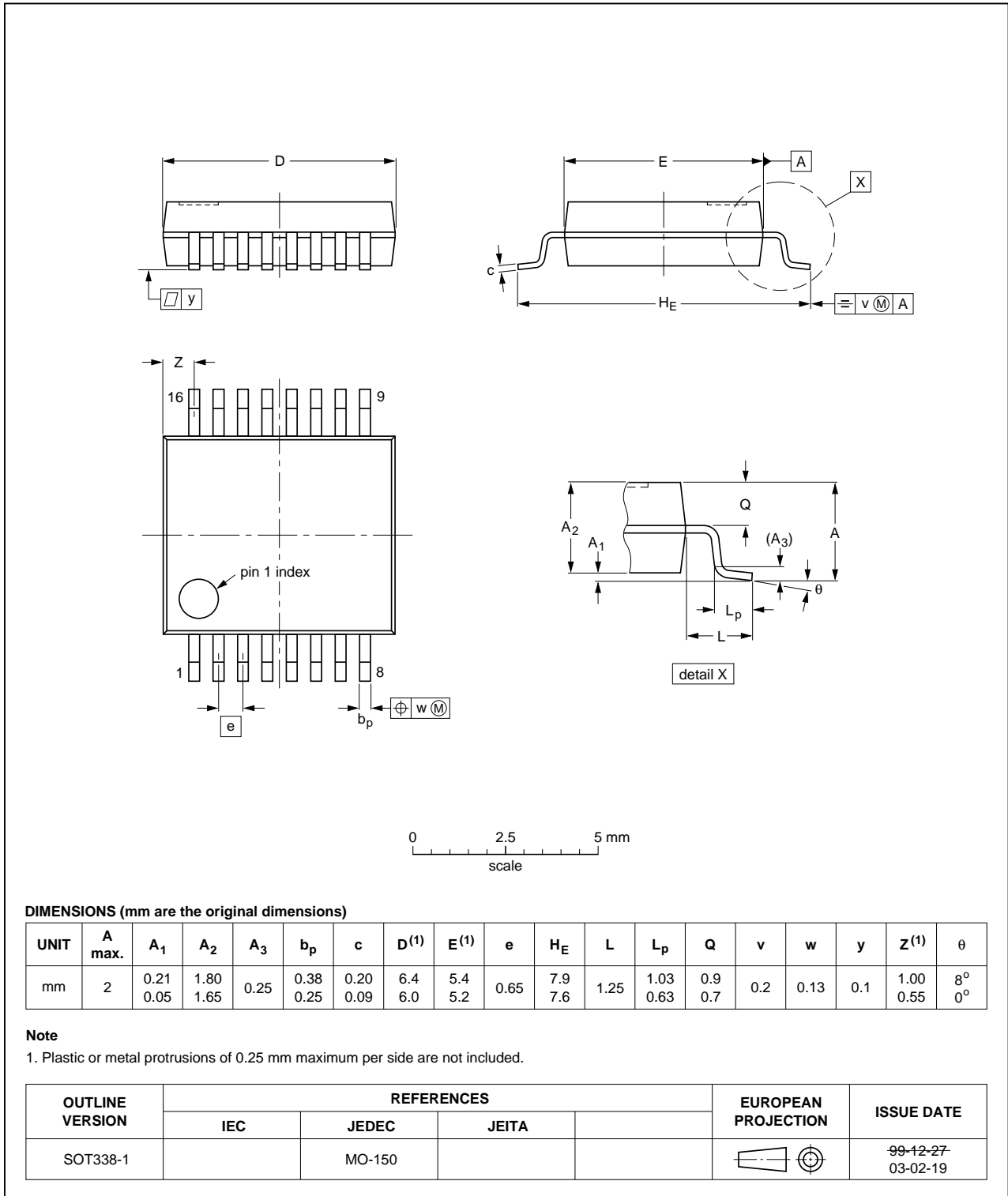


Fig 12. Package outline SOT338-1 (SSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

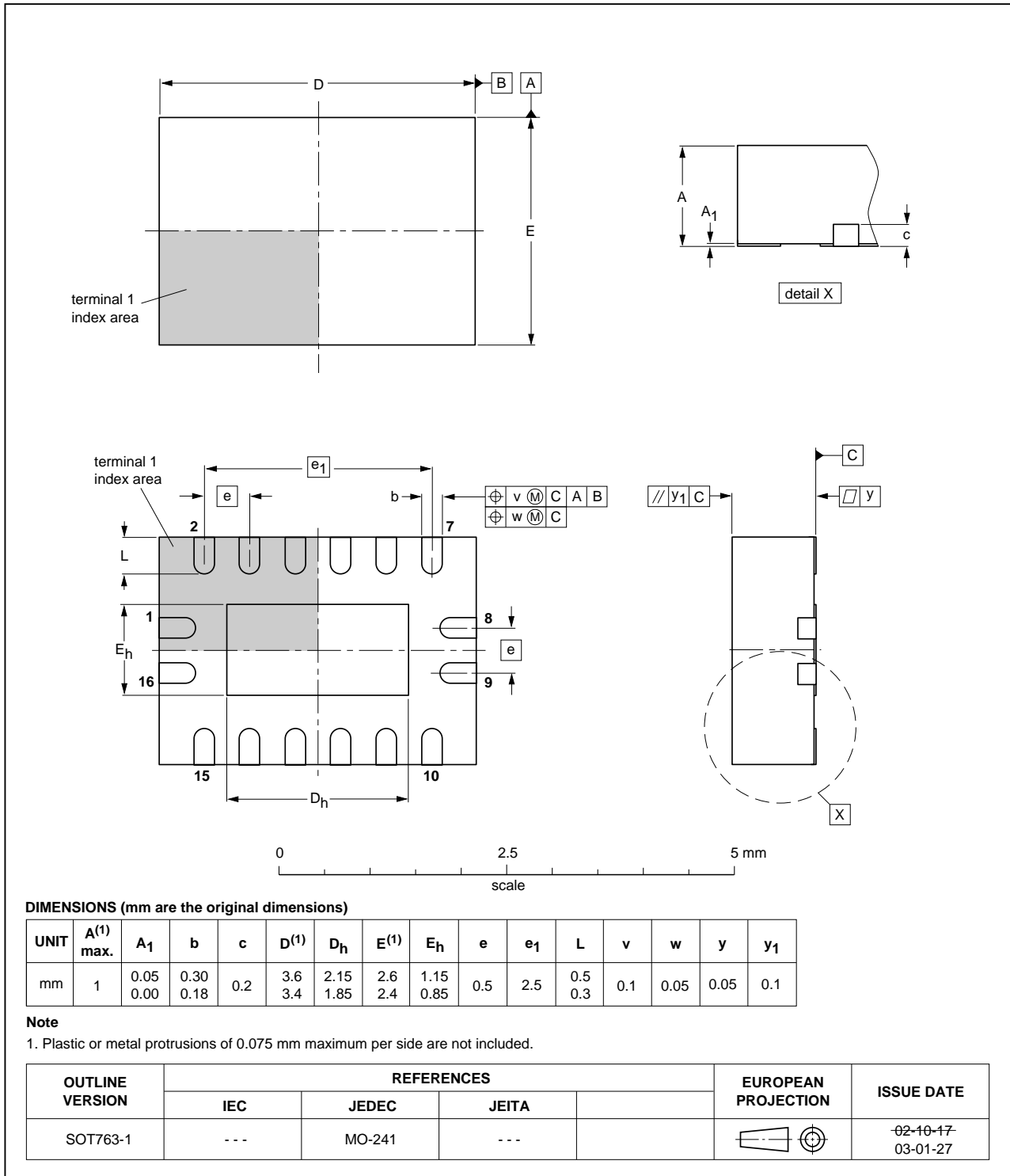


Fig 13. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|--|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| MM | Machine Model |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Doc. number | Supersedes |
|---------------------|--------------|-----------------------|---------------|-------------|--|
| 74HC_HCT138 v.4 | 20120627 | Product data sheet | - | - | 74HC_HCT138 v.3 |
| Modifications: | | | | | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. SOT38-1 changed to SOT38-4. |
| 74HC_HCT138 v.3 | 20051223 | Product data sheet | - | - | 74HC_HCT138_CNV v.2 |
| Modifications: | | | | | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 3 "Ordering information", Section 5 "Pinning information" and Section 12 "Package outline": Added DHVQFN package information Section 9 "Static characteristics": Added from the family specification |
| 74HC_HCT138_CNV v.2 | 19970827 | Product specification | - | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Ordering information | 2 |
| 4 | Functional diagram | 2 |
| 5 | Pinning information | 3 |
| 5.1 | Pinning | 3 |
| 5.2 | Pin description | 4 |
| 6 | Functional description | 4 |
| 7 | Limiting values | 4 |
| 8 | Recommended operating conditions | 5 |
| 9 | Static characteristics | 5 |
| 10 | Dynamic characteristics | 7 |
| 11 | Waveforms | 9 |
| 12 | Package outline | 11 |
| 13 | Abbreviations | 16 |
| 14 | Revision history | 16 |
| 15 | Legal information | 17 |
| 15.1 | Data sheet status | 17 |
| 15.2 | Definitions | 17 |
| 15.3 | Disclaimers | 17 |
| 15.4 | Trademarks | 18 |
| 16 | Contact information | 18 |
| 17 | Contents | 19 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 27 June 2012

Document identifier: 74HC_HCT138