AMD

Am29LV256M

256 Megabit (16 M x 16-Bit/32 M x 8-Bit) MirrorBit™ 3.0 Volt-only Uniform Sector Flash Memory with VersatileI/O™ Control

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

■ **Single power supply operation**
— 3 volt read, erase, and program operations

■ **VersatileI/O™ control**
— Device generates data output voltages and tolerates data input voltages on the CE# and DQ inputs/outputs as determined by the voltage on the V_{IO} pin; operates from 1.65 to 3.6 V

■ **Manufactured on 0.23 μm MirrorBit process technology**

■ **SecSi™ (Secured Silicon) Sector region**
— 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
— May be programmed and locked at the factory or by the customer

■ **Flexible sector architecture**
— Five hundred twelve 32 Kword (64 Kbyte) sectors

■ **Compatibility with JEDEC standards**
— Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection

■ **Minimum 100,000 erase cycle guarantee per sector**

■ **20-year data retention at 125°C**

PERFORMANCE CHARACTERISTICS

■ **High performance**
— 100 ns access time
— 30 ns page read times
— 0.5 s typical sector erase time
— 15 μs typical effective write buffer word programming time: 16-word/32-byte write buffer reduces overall programming time for multiple-word updates

— 4-word/8-byte page read buffer
— 16-word/32-byte write buffer

■ **Low power consumption (typical values at 3.0 V, 5 MHz)**
— 13 mA typical active read current
— 50 mA typical erase/program current
— 1 μA typical standby mode current

■ **Package options**
— 56-pin TSOP
— 64-ball Fortified BGA

SOFTWARE & HARDWARE FEATURES

■ **Software features**
— Program Suspend & Resume: read other sectors before programming operation is completed
— Erase Suspend & Resume: read/program other sectors before an erase operation is completed
— Data# polling & toggle bits provide status
— Unlock Bypass Program command reduces overall multiple-word or byte programming time
— CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices

■ **Hardware features**
— Sector Group Protection: hardware-level method of preventing write operations within a sector group
— Temporary Sector Group Unprotect: V_{ID}-level method of changing code in locked sector groups
— WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects first or last sector regardless of sector protection settings
— Hardware reset input (RESET#) resets device
— Ready/Busy# output (RY/BY#) detects program or erase cycle completion

GENERAL DESCRIPTION

The Am29LV256M is a 256 Mbit, 3.0 volt single power supply flash memory devices organized as 16,777,216 words or 33,554,432 bytes. The device has a 16-bit wide data bus that can also function as an 8-bit wide data bus by using the BYTE# input. The device can be programmed either in the host system or in standard EPROM programmers.

An access time of 100, 110, or 120 ns is available. Note that each access time has a specific operating voltage range (V_{CC}) and an I/O voltage range (V_{IO}), as specified in the Product Selector Guide and the Ordering Information sections. The device is offered in a 56-pin TSOP or Fortified BGA package. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0 volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (**WP#/**ACC)** input provides shorter programming times through increased current. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

The **VersatileI/O™** (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on the CE# control input and DQ I/Os to the same voltage level that is asserted on the V_{IO} pin. Refer to the Ordering Information section for valid V_{IO} options.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector group protection feature disables both program and erase operations in any combination of sector groups of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **SecSi™ (Secured Silicon) Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

The **Write Protect (WP#/ACC)** feature protects the first or last sector by asserting a logic low on the WP# pin.

AMD MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

RELATED DOCUMENTS

For a comprehensive information on MirrorBit products, including migration information, data sheets, application notes, and software drivers, please see www.amd.com→Flash Memory→Product Information→MirrorBit→Flash Information→Technical Documentation. The following is a partial list of documents closely related to this product:

MirrorBit™ Flash Memory Write Buffer Programming and Page Buffer Read

Implementing a Common Layout for AMD MirrorBit and Intel StrataFlash Memory Devices

Migrating from Single-byte to Three-byte Device IDs

TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

Part Number		Am29LV256M				
Speed/ Voltage Option	Regulated Voltage Range V_{CC} = 3.0–3.6 V	**103R** (Note 2) (V_{IO} = 2.7–3.6)		**113R** (V_{IO} = 1.65–3.6)		**123R** (V_{IO} = 1.65–3.6)
	Full Voltage Range V_{CC} = 2.7–3.6 V	**103** (Note 2) (V_{IO} = 2.7–3.6)	**113** (V_{IO} = 1.65–3.6)		**123** (V_{IO} = 1.65–3.6)	
Max. Access Time (ns)		100	110		120	
Max. CE# Access Time (ns)		100	110		120	
Max. Page access time (t_{PACC})		30	30	40	30	40
Max. OE# Access Time (ns)		30	30	40	30	40

Notes:

1. See "AC Characteristics" for full specifications.

2. Contact factory for availability and ordering information.

BLOCK DIAGRAM

CONNECTION DIAGRAMS

```
A23   1                                              56  NC
A22   2                                              55  NC
A15   3                                              54  A16
A14   4                                              53  BYTE#
A13   5                                              52  Vss
A12   6                                              51  DQ15/A-1
A11   7                                              50  DQ7
A10   8                                              49  DQ14
A9    9                                              48  DQ6
A8   10                                              47  DQ13
A19  11                                              46  DQ5
A20  12            56-Pin Standard TSOP              45  DQ12
WE#  13                                              44  DQ4
RESET# 14                                            43  Vcc
A21  15                                              42  DQ11
WP#/ACC 16                                           41  DQ3
RY/BY# 17                                            40  DQ10
A18  18                                              39  DQ2
A17  19                                              38  DQ9
A7   20                                              37  DQ1
A6   21                                              36  DQ8
A5   22                                              35  DQ0
A4   23                                              34  OE#
A3   24                                              33  Vss
A2   25                                              32  CE#
A1   26                                              31  A0
NC   27                                              30  NC
NC   28                                              29  VIO
```

```
NC    1                                              56  A23
NC    2                                              55  A22
A16   3                                              54  A15
BYTE# 4                                              53  A14
Vss   5                                              52  A13
DQ15/A-1 6                                           51  A12
DQ7   7                                              50  A11
DQ14  8                                              49  A10
DQ6   9                                              48  A9
DQ13 10                                              47  A8
DQ5  11                                              46  A19
DQ12 12            56-Pin Reverse TSOP               45  A20
DQ4  13                                              44  WE#
Vcc  14                                              43  RESET#
DQ11 15                                              42  A21
DQ3  16                                              41  WP#/ACC
DQ10 17                                              40  RY/BY#
DQ2  18                                              39  A18
DQ9  19                                              38  A17
DQ1  20                                              37  A7
DQ8  21                                              36  A6
DQ0  22                                              35  A5
OE#  23                                              34  A4
Vss  24                                              33  A3
CE#  25                                              32  A2
A0   26                                              31  A1
NC   27                                              30  NC
VIO  28                                              29  NC
```

CONNECTION DIAGRAMS

Fortified BGA
Top View, Balls Facing Down

A8 NC	B8 A22	C8 A23	D8 V_{IO}	E8 V_{SS}	F8 NC	G8 NC	H8 NC
A7 A13	B7 A12	C7 A14	D7 A15	E7 A16	F7 BYTE#	G7 DQ15/A-1	H7 V_{SS}
A6 A9	B6 A8	C6 A10	D6 A11	E6 DQ7	F6 DQ14	G6 DQ13	H6 DQ6
A5 WE#	B5 RESET#	C5 A21	D5 A19	E5 DQ5	F5 DQ12	G5 V_{CC}	H5 DQ4
A4 RY/BY#	B4 WP#/ACC	C4 A18	D4 A20	E4 DQ2	F4 DQ10	G4 DQ11	H4 DQ3
A3 A7	B3 A17	C3 A6	D3 A5	E3 DQ0	F3 DQ8	G3 DQ9	H3 DQ1
A2 A3	B2 A4	C2 A2	D2 A1	E2 A0	F2 CE#	G2 OE#	H2 V_{SS}
A1 NC	B1 NC	C1 NC	D1 NC	E1 NC	F1 V_{IO}	G1 NC	H1 NC

Note: The FBGA package pinout configuration shown is preliminary. The ball count and package physical dimensions have not yet been determined. Contact AMD for further information.

SPECIAL PACKAGE HANDLING INSTRUCTIONS

Special handling is required for Flash Memory products in molded packages (TSOP and BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A23–A0 = 24 Address inputs

DQ14–DQ0 = 15 Data inputs/outputs

DQ15/A-1 = DQ15 (Data input/output, word mode),
A-1 (LSB Address input, byte mode)

CE# = Chip Enable input

OE# = Output Enable input

WE# = Write Enable input

WP#/ACC = Hardware Write Protect input;
Acceleration input

RESET# = Hardware Reset Pin input

BYTE# = Selects 8-bit or 16-bit mode

RY/BY# = Ready/Busy output

V_{CC} = 3.0 volt-only single power supply
(see Product Selector Guide for
speed options and voltage
supply tolerances)

V_{IO} = Output Buffer power

V_{SS} = Device Ground

NC = Pin Not Connected Internally

LOGIC SYMBOL
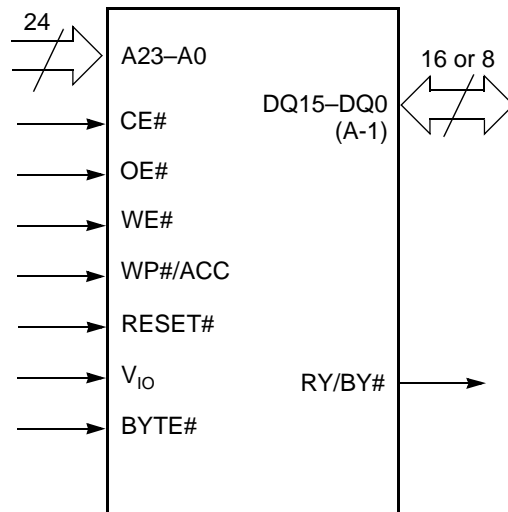
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29LV256M   H   123R   PG   I

TEMPERATURE RANGE

I   =   Industrial (–40°C to +85°C)

PACKAGE TYPE

E   =   56-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 056)

F   =   56-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR056)

PG   =   64-Ball Fortified Ball Grid Array, 1.0 mm pitch, 18 x 12 mm package (LAC064)

SPEED OPTION

See Product Selector Guide and Valid Combinations

SECTOR ARCHITECTURE AND SECTOR WRITE PROTECTION (WP# = V_{IL})

H   =   Uniform sector device, highest address sector protected

L   =   Uniform sector device, lowest address sector protected

DEVICE NUMBER/DESCRIPTION

Am29LV256MH/L

256 Megabit (16 M x 16-Bit/32 M x 8-Bit) MirrorBit Uniform Sector Flash Memory with VersatileIO™ Control 3.0 Volt-only Read, Program, and Erase

Valid Combinations for TSOP Package		Speed (ns)	V_{IO} Range	V_{CC} Range
Am29LV256MH113 Am29LV256ML113	EI, FI	110	1.65–3.6 V	2.7–3.6 V
Am29LV256MH123 Am29LV256ML123		120	1.65–3.6 V	
Am29LV256MH113R Am29LV256ML113R		110	1.65–3.6 V	3.0–3.6 V
Am29LV256MH123R Am29LV256ML123R		120	1.65–3.6 V	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations for Fortified BGA Package				Speed (ns)	V_{IO} Range	V_{CC} Range
Order Number	Package Marking					
Am29LV256MH113 Am29LV256ML113	L256MH113V L256ML113V	PG	I	110	1.65–3.6 V	2.7–3.6 V
Am29LV256MH123 Am29LV256ML123	L256MH123V L256ML123V			120	1.65–3.6 V	
Am29LV256MH113R Am29LV256ML113R	L256MH113R L256ML113R			110	1.65–3.6 V	3.0–3.6 V
Am29LV256MH123R Am29LV256ML123R	L256MH123R L256ML123R			120	1.65–3.6 V	

Note: For 103, 103R speed option shown in product selector guide, contact AMD for availability and ordering information.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1.   Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#	ACC	Addresses (Note 2)	DQ0–DQ7	DQ8–DQ15 BYTE# = V_{IH}	DQ8–DQ15 BYTE# = V_{IL}
Read	L	L	H	H	X	X	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write (Program/Erase)	L	H	L	H	(Note 3)	X	A_{IN}	(Note 4)	(Note 4)	
Accelerated Program	L	H	L	H	(Note 3)	V_{HH}	A_{IN}	(Note 4)	(Note 4)	
Standby	$V_{CC} \pm$ 0.3 V	X	X	$V_{CC} \pm$ 0.3 V	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	X	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	X	X	High-Z	High-Z	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	H	X	SA, A6 =L, A3=L, A2=L, A1=H, A0=L	(Note 4)	X	X
Sector Group Unprotect (Note 2)	L	H	L	V_{ID}	H	X	SA, A6=H, A3=L, A2=L, A1=H, A0=L	(Note 4)	X	X
Temporary Sector Group Unprotect	X	X	X	V_{ID}	H	X	A_{IN}	(Note 4)	(Note 4)	High-Z

Legend: L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 11.5–12.5V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

1. Addresses are A23:A0 in word mode; A23:A-1 in byte mode. Sector addresses are A23:A15 in both modes.

2. The sector group protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Unprotection" section.

3. If WP# = V_{IL}, the first or last sector group remains protected. If WP# = V_{IH}, the first or last sector will be protected or unprotected as determined by the method described in "Write Protect (WP#)". All sectors are unprotected when shipped from the factory (The SecSi Sector may be factory protected depending on version ordered.)

4. D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 2).

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ0–DQ15 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

VersatileIO™ (V_{IO}) Control

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on CE# and DQ I/Os to the same voltage level that is asserted on V_{IO}. See Ordering Information for V_{IO} options on this device.

For example, a $V_{I/O}$ of 1.65–3.6 volts allows for I/O at the 1.8 or 3 volt levels, driving and receiving signals to and from other 1.8 or 3 V devices on the same data bus.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 13 for the timing diagram. Refer to the DC Characteristics table for the active current specification on reading array data.

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 4 words/8 bytes. The appropriate page is selected by the higher address bits A(max)–A2. Address bits A1–A0 in word mode (A1–A-1 in byte mode) determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the "read-page addresses" constant and changing the "intra-read page" addresses.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The "Word/Byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address space that each sector occupies.

Refer to the DC Characteristics table for the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Write Buffer

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See "Write Buffer" for more information.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sector groups, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced,

and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{IO} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{IO} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the DC Characteristics table for the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to the DC Characteristics table for the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3$ V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 15 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2.   Sector Address Table

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	0	0	64/32	0000000–000FFFF	000000–007FFF
SA1	0	0	0	0	0	0	0	0	1	64/32	0010000–001FFFF	008000–00FFFF
SA2	0	0	0	0	0	0	0	1	0	64/32	0020000–002FFFF	010000–017FFF
SA3	0	0	0	0	0	0	0	1	1	64/32	0030000–003FFFF	018000–01FFFF
SA4	0	0	0	0	0	0	1	0	0	64/32	0040000–004FFFF	020000–027FFF
SA5	0	0	0	0	0	0	1	0	1	64/32	0050000–005FFFF	028000–02FFFF
SA6	0	0	0	0	0	0	1	1	0	64/32	0060000–006FFFF	030000–037FFF
SA7	0	0	0	0	0	0	1	1	1	64/32	0070000–007FFFF	038000–03FFFF
SA8	0	0	0	0	0	1	0	0	0	64/32	0080000–008FFFF	040000–047FFF
SA9	0	0	0	0	0	1	0	0	1	64/32	0090000–009FFFF	048000–04FFFF
SA10	0	0	0	0	0	1	0	1	0	64/32	00A0000–00AFFFF	050000–057FFF
SA11	0	0	0	0	0	1	0	1	1	64/32	00B0000–00BFFFF	058000–05FFFF
SA12	0	0	0	0	0	1	1	0	0	64/32	00C0000–00CFFFF	060000–067FFF
SA13	0	0	0	0	0	1	1	0	1	64/32	00D0000–00DFFFF	068000–06FFFF
SA14	0	0	0	0	0	1	1	1	0	64/32	00E0000–00EFFFF	070000–077FFF
SA15	0	0	0	0	0	1	1	1	1	64/32	00F0000–00FFFFF	078000–07FFFF
SA16	0	0	0	0	1	0	0	0	0	64/32	0100000–010FFFF	080000–087FFF
SA17	0	0	0	0	1	0	0	0	1	64/32	0110000–011FFFF	088000–08FFFF
SA18	0	0	0	0	1	0	0	1	0	64/32	0120000–012FFFF	090000–097FFF
SA19	0	0	0	0	1	0	0	1	1	64/32	0130000–013FFFF	098000–09FFFF
SA20	0	0	0	0	1	0	1	0	0	64/32	0140000–014FFFF	0A0000–0A7FFF
SA21	0	0	0	0	1	0	1	0	1	64/32	0150000–015FFFF	0A8000–0AFFFF
SA22	0	0	0	0	1	0	1	1	0	64/32	0160000–016FFFF	0B0000–0B7FFF
SA23	0	0	0	0	1	0	1	1	1	64/32	0170000–017FFFF	0B8000–0BFFFF
SA24	0	0	0	0	1	1	0	0	0	64/32	0180000–018FFFF	0C0000–0C7FFF
SA25	0	0	0	0	1	1	0	0	1	64/32	0190000–019FFFF	0C8000–0CFFFF
SA26	0	0	0	0	1	1	0	1	0	64/32	01A0000–01AFFFF	0D0000–0D7FFF
SA27	0	0	0	0	1	1	0	1	1	64/32	01B0000–01BFFFF	0D8000–0DFFFF
SA28	0	0	0	0	1	1	1	0	0	64/32	01C0000–01CFFFF	0E0000–0E7FFF
SA29	0	0	0	0	1	1	1	0	1	64/32	01D0000–01DFFFF	0E8000–0EFFFF
SA30	0	0	0	0	1	1	1	1	0	64/32	01E0000–01EFFFF	0F0000–0F7FFF
SA31	0	0	0	0	1	1	1	1	1	64/32	01F0000–01FFFFF	0F8000–0FFFFF
SA32	0	0	0	1	0	0	0	0	0	64/32	0200000–020FFFF	100000–107FFF
SA33	0	0	0	1	0	0	0	0	1	64/32	0210000–021FFFF	108000–10FFFF
SA34	0	0	0	1	0	0	0	1	0	64/32	0220000–022FFFF	110000–117FFF
SA35	0	0	0	1	0	0	0	1	1	64/32	0230000–023FFFF	118000–11FFFF
SA36	0	0	0	1	0	0	1	0	0	64/32	0240000–024FFFF	120000–127FFF
SA37	0	0	0	1	0	0	1	0	1	64/32	0250000–025FFFF	128000–12FFFF
SA38	0	0	0	1	0	0	1	1	0	64/32	0260000–026FFFF	130000–137FFF
SA39	0	0	0	1	0	0	1	1	1	64/32	0270000–027FFFF	138000–13FFFF
SA40	0	0	0	1	0	1	0	0	0	64/32	0280000–028FFFF	140000–147FFF
SA41	0	0	0	1	0	1	0	0	1	64/32	0290000–029FFFF	148000–14FFFF
SA42	0	0	0	1	0	1	0	1	0	64/32	02A0000–02AFFFF	150000–157FFF
SA43	0	0	0	1	0	1	0	1	1	64/32	02B0000–02BFFFF	158000–15FFFF
SA44	0	0	0	1	0	1	1	0	0	64/32	02C0000–02CFFFF	160000–167FFF
SA45	0	0	0	1	0	1	1	0	1	64/32	02D0000–02DFFFF	168000–16FFFF
SA46	0	0	0	1	0	1	1	1	0	64/32	02E0000–02EFFFF	170000–177FFF

Table 2.   Sector Address Table (Continued)

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA47	0	0	0	1	0	1	1	1	1	64/32	02F0000–02FFFFF	178000–17FFFF
SA48	0	0	0	1	1	0	0	0	0	64/32	0300000–030FFFF	180000–187FFF
SA49	0	0	0	1	1	0	0	0	1	64/32	0310000–031FFFF	188000–18FFFF
SA50	0	0	0	1	1	0	0	1	0	64/32	0320000–032FFFF	190000–197FFF
SA51	0	0	0	1	1	0	0	1	1	64/32	0330000–033FFFF	198000–19FFFF
SA52	0	0	0	1	1	0	1	0	0	64/32	0340000–034FFFF	1A0000–1A7FFF
SA53	0	0	0	1	1	0	1	0	1	64/32	0350000–035FFFF	1A8000–1AFFFF
SA54	0	0	0	1	1	0	1	1	0	64/32	0360000–036FFFF	1B0000–1B7FFF
SA55	0	0	0	1	1	0	1	1	1	64/32	0370000–037FFFF	1B8000–1BFFFF
SA56	0	0	0	1	1	1	0	0	0	64/32	0380000–038FFFF	1C0000–1C7FFF
SA57	0	0	0	1	1	1	0	0	1	64/32	0390000–039FFFF	1C8000–1CFFFF
SA58	0	0	0	1	1	1	0	1	0	64/32	03A0000–03AFFFF	1D0000–1D7FFF
SA59	0	0	0	1	1	1	0	1	1	64/32	03B0000–03BFFFF	1D8000–1DFFFF
SA60	0	0	0	1	1	1	1	0	0	64/32	03C0000–03CFFFF	1E0000–1E7FFF
SA61	0	0	0	1	1	1	1	0	1	64/32	03D0000–03DFFFF	1E8000–1EFFFF
SA62	0	0	0	1	1	1	1	1	0	64/32	03E0000–03EFFFF	1F0000–1F7FFF
SA63	0	0	0	1	1	1	1	1	1	64/32	03F0000–03FFFFF	1F8000–1FFFFF
SA64	0	0	1	0	0	0	0	0	0	64/32	0400000–040FFFF	200000–207FFF
SA65	0	0	1	0	0	0	0	0	1	64/32	0410000–041FFFF	208000–20FFFF
SA66	0	0	1	0	0	0	0	1	0	64/32	0420000–042FFFF	210000–217FFF
SA67	0	0	1	0	0	0	0	1	1	64/32	0430000–043FFFF	218000–21FFFF
SA68	0	0	1	0	0	0	1	0	0	64/32	0440000–044FFFF	220000–227FFF
SA69	0	0	1	0	0	0	1	0	1	64/32	0450000–045FFFF	228000–22FFFF
SA70	0	0	1	0	0	0	1	1	0	64/32	0460000–046FFFF	230000–237FFF
SA71	0	0	1	0	0	0	1	1	1	64/32	0470000–047FFFF	238000–23FFFF
SA72	0	0	1	0	0	1	0	0	0	64/32	0480000–048FFFF	240000–247FFF
SA73	0	0	1	0	0	1	0	0	1	64/32	0490000–049FFFF	248000–24FFFF
SA74	0	0	1	0	0	1	0	1	0	64/32	04A0000–04AFFFF	250000–257FFF
SA75	0	0	1	0	0	1	0	1	1	64/32	04B0000–04BFFFF	258000–25FFFF
SA76	0	0	1	0	0	1	1	0	0	64/32	04C0000–04CFFFF	260000–267FFF
SA77	0	0	1	0	0	1	1	0	1	64/32	04D0000–04DFFFF	268000–26FFFF
SA78	0	0	1	0	0	1	1	1	0	64/32	04E0000–04EFFFF	270000–277FFF
SA79	0	0	1	0	0	1	1	1	1	64/32	04F0000–04FFFFF	278000–27FFFF
SA80	0	0	1	0	1	0	0	0	0	64/32	0500000–050FFFF	280000–287FFF
SA81	0	0	1	0	1	0	0	0	1	64/32	0510000–051FFFF	288000–28FFFF
SA82	0	0	1	0	1	0	0	1	0	64/32	0520000–052FFFF	290000–297FFF
SA83	0	0	1	0	1	0	0	1	1	64/32	0530000–053FFFF	298000–29FFFF
SA84	0	0	1	0	1	0	1	0	0	64/32	0540000–054FFFF	2A0000–2A7FFF
SA85	0	0	1	0	1	0	1	0	1	64/32	0550000–055FFFF	2A8000–2AFFFF
SA86	0	0	1	0	1	0	1	1	0	64/32	0560000–056FFFF	2B0000–2B7FFF
SA87	0	0	1	0	1	0	1	1	1	64/32	0570000–057FFFF	2B8000–2BFFFF
SA88	0	0	1	0	1	1	0	0	0	64/32	0580000–058FFFF	2C0000–2C7FFF
SA89	0	0	1	0	1	1	0	0	1	64/32	0590000–059FFFF	2C8000–2CFFFF
SA90	0	0	1	0	1	1	0	1	0	64/32	05A0000–05AFFFF	2D0000–2D7FFF
SA91	0	0	1	0	1	1	0	1	1	64/32	05B0000–05BFFFF	2D8000–2DFFFF
SA92	0	0	1	0	1	1	1	0	0	64/32	05C0000–05CFFFF	2E0000–2E7FFF
SA93	0	0	1	0	1	1	1	0	1	64/32	05D0000–05DFFFF	2E8000–2EFFFF
SA94	0	0	1	0	1	1	1	1	0	64/32	05E0000–05EFFFF	2F0000–2F7FFF

Table 2. Sector Address Table (Continued)

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA95	0	0	1	0	1	1	1	1	1	64/32	05F0000–05FFFFF	2F8000–2FFFFF
SA96	0	0	1	1	0	0	0	0	0	64/32	0600000–060FFFF	300000–307FFF
SA97	0	0	1	1	0	0	0	0	1	64/32	0610000–061FFFF	308000–30FFFF
SA98	0	0	1	1	0	0	0	1	0	64/32	0620000–062FFFF	310000–317FFF
SA99	0	0	1	1	0	0	0	1	1	64/32	0630000–063FFFF	318000–31FFFF
SA100	0	0	1	1	0	0	1	0	0	64/32	0640000–064FFFF	320000–327FFF
SA101	0	0	1	1	0	0	1	0	1	64/32	0650000–065FFFF	328000–32FFFF
SA102	0	0	1	1	0	0	1	1	0	64/32	0660000–066FFFF	330000–337FFF
SA103	0	0	1	1	0	0	1	1	1	64/32	0670000–067FFFF	338000–33FFFF
SA104	0	0	1	1	0	1	0	0	0	64/32	0680000–068FFFF	340000–347FFF
SA105	0	0	1	1	0	1	0	0	1	64/32	0690000–069FFFF	348000–34FFFF
SA106	0	0	1	1	0	1	0	1	0	64/32	06A0000–06AFFFF	350000–357FFF
SA107	0	0	1	1	0	1	0	1	1	64/32	06B0000–06BFFFF	358000–35FFFF
SA108	0	0	1	1	0	1	1	0	0	64/32	06C0000–06CFFFF	360000–367FFF
SA109	0	0	1	1	0	1	1	0	1	64/32	06D0000–06DFFFF	368000–36FFFF
SA110	0	0	1	1	0	1	1	1	0	64/32	06E0000–06EFFFF	370000–377FFF
SA111	0	0	1	1	0	1	1	1	1	64/32	06F0000–06FFFFF	378000–37FFFF
SA112	0	0	1	1	1	0	0	0	0	64/32	0700000–070FFFF	380000–387FFF
SA113	0	0	1	1	1	0	0	0	1	64/32	0710000–071FFFF	388000–38FFFF
SA114	0	0	1	1	1	0	0	1	0	64/32	0720000–072FFFF	390000–397FFF
SA115	0	0	1	1	1	0	0	1	1	64/32	0730000–073FFFF	398000–39FFFF
SA116	0	0	1	1	1	0	1	0	0	64/32	0740000–074FFFF	3A0000–3A7FFF
SA117	0	0	1	1	1	0	1	0	1	64/32	0750000–075FFFF	3A8000–3AFFFF
SA118	0	0	1	1	1	0	1	1	0	64/32	0760000–076FFFF	3B0000–3B7FFF
SA119	0	0	1	1	1	0	1	1	1	64/32	0770000–077FFFF	3B8000–3BFFFF
SA120	0	0	1	1	1	1	0	0	0	64/32	0780000–078FFFF	3C0000–3C7FFF
SA121	0	0	1	1	1	1	0	0	1	64/32	0790000–079FFFF	3C8000–3CFFFF
SA122	0	0	1	1	1	1	0	1	0	64/32	07A0000–07AFFFF	3D0000–3D7FFF
SA123	0	0	1	1	1	1	0	1	1	64/32	07B0000–07BFFFF	3D8000–3DFFFF
SA124	0	0	1	1	1	1	1	0	0	64/32	07C0000–07CFFFF	3E0000–3E7FFF
SA125	0	0	1	1	1	1	1	0	1	64/32	07D0000–07DFFFF	3E8000–3EFFFF
SA126	0	0	1	1	1	1	1	1	0	64/32	07E0000–07EFFFF	3F0000–3F7FFF
SA127	0	0	1	1	1	1	1	1	1	64/32	07F0000–07FFFFF	3F8000–3FFFFF
SA128	0	1	0	0	0	0	0	0	0	64/32	0800000–080FFFF	400000–407FFF
SA129	0	1	0	0	0	0	0	0	1	64/32	0810000–081FFFF	408000–40FFFF
SA130	0	1	0	0	0	0	0	1	0	64/32	0820000–082FFFF	410000–417FFF
SA131	0	1	0	0	0	0	0	1	1	64/32	0830000–083FFFF	418000–41FFFF
SA132	0	1	0	0	0	0	1	0	0	64/32	0840000–084FFFF	420000–427FFF
SA133	0	1	0	0	0	0	1	0	1	64/32	0850000–085FFFF	428000–42FFFF
SA134	0	1	0	0	0	0	1	1	0	64/32	0860000–086FFFF	430000–437FFF
SA135	0	1	0	0	0	0	1	1	1	64/32	0870000–087FFFF	438000–43FFFF
SA136	0	1	0	0	0	1	0	0	0	64/32	0880000–088FFFF	440000–447FFF
SA137	0	1	0	0	0	1	0	0	1	64/32	0890000–089FFFF	448000–44FFFF
SA138	0	1	0	0	0	1	0	1	0	64/32	08A0000–08AFFFF	450000–457FFF
SA139	0	1	0	0	0	1	0	1	1	64/32	08B0000–08BFFFF	458000–45FFFF
SA140	0	1	0	0	0	1	1	0	0	64/32	08C0000–08CFFFF	460000–467FFF
SA141	0	1	0	0	0	1	1	0	1	64/32	08D0000–08DFFFF	468000–46FFFF
SA142	0	1	0	0	0	1	1	1	0	64/32	08E0000–08EFFFF	470000–477FFF

Table 2. Sector Address Table (Continued)

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA143	0	1	0	0	0	1	1	1	1	64/32	08F0000–08FFFFF	478000–47FFFF
SA144	0	1	0	0	1	0	0	0	0	64/32	0900000–090FFFF	480000–487FFF
SA145	0	1	0	0	1	0	0	0	1	64/32	0910000–091FFFF	488000–48FFFF
SA146	0	1	0	0	1	0	0	1	0	64/32	0920000–092FFFF	490000–497FFF
SA147	0	1	0	0	1	0	0	1	1	64/32	0930000–093FFFF	498000–49FFFF
SA148	0	1	0	0	1	0	1	0	0	64/32	0940000–094FFFF	4A0000–4A7FFF
SA149	0	1	0	0	1	0	1	0	1	64/32	0950000–095FFFF	4A8000–4AFFFF
SA150	0	1	0	0	1	0	1	1	0	64/32	0960000–096FFFF	4B0000–4B7FFF
SA151	0	1	0	0	1	0	1	1	1	64/32	0970000–097FFFF	4B8000–4BFFFF
SA152	0	1	0	0	1	1	0	0	0	64/32	0980000–098FFFF	4C0000–4C7FFF
SA153	0	1	0	0	1	1	0	0	1	64/32	0990000–099FFFF	4C8000–4CFFFF
SA154	0	1	0	0	1	1	0	1	0	64/32	09A0000–09AFFFF	4D0000–4D7FFF
SA155	0	1	0	0	1	1	0	1	1	64/32	09B0000–09BFFFF	4D8000–4DFFFF
SA156	0	1	0	0	1	1	1	0	0	64/32	09C0000–09CFFFF	4E0000–4E7FFF
SA157	0	1	0	0	1	1	1	0	1	64/32	09D0000–09DFFFF	4E8000–4EFFFF
SA158	0	1	0	0	1	1	1	1	0	64/32	09E0000–09EFFFF	4F0000–4F7FFF
SA159	0	1	0	0	1	1	1	1	1	64/32	09F0000–09FFFFF	4F8000–4FFFFF
SA160	0	1	0	1	0	0	0	0	0	64/32	0A00000–0A0FFFF	500000–507FFF
SA161	0	1	0	1	0	0	0	0	1	64/32	0A10000–0A1FFFF	508000–50FFFF
SA162	0	1	0	1	0	0	0	1	0	64/32	0A20000–0A2FFFF	510000–517FFF
SA163	0	1	0	1	0	0	0	1	1	64/32	0A30000–0A3FFFF	518000–51FFFF
SA164	0	1	0	1	0	0	1	0	0	64/32	0A40000–0A4FFFF	520000–527FFF
SA165	0	1	0	1	0	0	1	0	1	64/32	0A50000–0A5FFFF	528000–52FFFF
SA166	0	1	0	1	0	0	1	1	0	64/32	0A60000–0A6FFFF	530000–537FFF
SA167	0	1	0	1	0	0	1	1	1	64/32	0A70000–0A7FFFF	538000–53FFFF
SA168	0	1	0	1	0	1	0	0	0	64/32	0A80000–0A8FFFF	540000–547FFF
SA169	0	1	0	1	0	1	0	0	1	64/32	0A90000–0A9FFFF	548000–54FFFF
SA170	0	1	0	1	0	1	0	1	0	64/32	0AA0000–0AAFFFF	550000–557FFF
SA171	0	1	0	1	0	1	0	1	1	64/32	0AB0000–0ABFFFF	558000–55FFFF
SA172	0	1	0	1	0	1	1	0	0	64/32	0AC0000–0ACFFFF	560000–567FFF
SA173	0	1	0	1	0	1	1	0	1	64/32	0AD0000–0ADFFFF	568000–56FFFF
SA174	0	1	0	1	0	1	1	1	0	64/32	0AE0000–0AEFFFF	570000–577FFF
SA175	0	1	0	1	0	1	1	1	1	64/32	0AF0000–0AFFFFF	578000–57FFFF
SA176	0	1	0	1	1	0	0	0	0	64/32	0B00000–0B0FFFF	580000–587FFF
SA177	0	1	0	1	1	0	0	0	1	64/32	0B10000–0B1FFFF	588000–58FFFF
SA178	0	1	0	1	1	0	0	1	0	64/32	0B20000–0B2FFFF	590000–597FFF
SA179	0	1	0	1	1	0	0	1	1	64/32	0B30000–0B3FFFF	598000–59FFFF
SA180	0	1	0	1	1	0	1	0	0	64/32	0B40000–0B4FFFF	5A0000–5A7FFF
SA181	0	1	0	1	1	0	1	0	1	64/32	0B50000–0B5FFFF	5A8000–5AFFFF
SA182	0	1	0	1	1	0	1	1	0	64/32	0B60000–0B6FFFF	5B0000–5B7FFF
SA183	0	1	0	1	1	0	1	1	1	64/32	0B70000–0B7FFFF	5B8000–5BFFFF
SA184	0	1	0	1	1	1	0	0	0	64/32	0B80000–0B8FFFF	5C0000–5C7FFF
SA185	0	1	0	1	1	1	0	0	1	64/32	0B90000–0B9FFFF	5C8000–5CFFFF
SA186	0	1	0	1	1	1	0	1	0	64/32	0BA0000–0BAFFFF	5D0000–5D7FFF
SA187	0	1	0	1	1	1	0	1	1	64/32	0BB0000–0BBFFFF	5D8000–5DFFFF
SA188	0	1	0	1	1	1	1	0	0	64/32	0BC0000–0BCFFFF	5E0000–5E7FFF
SA189	0	1	0	1	1	1	1	0	1	64/32	0BD0000–0BDFFFF	5E8000–5EFFFF
SA190	0	1	0	1	1	1	1	1	0	64/32	0BE0000–0BEFFFF	5F0000–5F7FFF

Table 2. Sector Address Table (Continued)

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA191	0	1	0	1	1	1	1	1	1	64/32	0BF0000–0BFFFFF	5F8000–5FFFFF
SA192	0	1	1	0	0	0	0	0	0	64/32	0C00000–0C0FFFF	600000–607FFF
SA193	0	1	1	0	0	0	0	0	1	64/32	0C10000–0C1FFFF	608000–60FFFF
SA194	0	1	1	0	0	0	0	1	0	64/32	0C20000–0C2FFFF	610000–617FFF
SA195	0	1	1	0	0	0	0	1	1	64/32	0C30000–0C3FFFF	618000–61FFFF
SA196	0	1	1	0	0	0	1	0	0	64/32	0C40000–0C4FFFF	620000–627FFF
SA197	0	1	1	0	0	0	1	0	1	64/32	0C50000–0C5FFFF	628000–62FFFF
SA198	0	1	1	0	0	0	1	1	0	64/32	0C60000–0C6FFFF	630000–637FFF
SA199	0	1	1	0	0	0	1	1	1	64/32	0C70000–0C7FFFF	638000–63FFFF
SA200	0	1	1	0	0	1	0	0	0	64/32	0C80000–0C8FFFF	640000–647FFF
SA201	0	1	1	0	0	1	0	0	1	64/32	0C90000–0C9FFFF	648000–64FFFF
SA202	0	1	1	0	0	1	0	1	0	64/32	0CA0000–0CAFFFF	650000–657FFF
SA203	0	1	1	0	0	1	0	1	1	64/32	0CB0000–0CBFFFF	658000–65FFFF
SA204	0	1	1	0	0	1	1	0	0	64/32	0CC0000–0CCFFFF	660000–667FFF
SA205	0	1	1	0	0	1	1	0	1	64/32	0CD0000–0CDFFFF	668000–66FFFF
SA206	0	1	1	0	0	1	1	1	0	64/32	0CE0000–0CEFFFF	670000–677FFF
SA207	0	1	1	0	0	1	1	1	1	64/32	0CF0000–0CFFFFF	678000–67FFFF
SA208	0	1	1	0	1	0	0	0	0	64/32	0D00000–0D0FFFF	680000–687FFF
SA209	0	1	1	0	1	0	0	0	1	64/32	0D10000–0D1FFFF	688000–68FFFF
SA210	0	1	1	0	1	0	0	1	0	64/32	0D20000–0D2FFFF	690000–697FFF
SA211	0	1	1	0	1	0	0	1	1	64/32	0D30000–0D3FFFF	698000–69FFFF
SA212	0	1	1	0	1	0	1	0	0	64/32	0D40000–0D4FFFF	6A0000–6A7FFF
SA213	0	1	1	0	1	0	1	0	1	64/32	0D50000–0D5FFFF	6A8000–6AFFFF
SA214	0	1	1	0	1	0	1	1	0	64/32	0D60000–0D6FFFF	6B0000–6B7FFF
SA215	0	1	1	0	1	0	1	1	1	64/32	0D70000–0D7FFFF	6B8000–6BFFFF
SA216	0	1	1	0	1	1	0	0	0	64/32	0D80000–0D8FFFF	6C0000–6C7FFF
SA217	0	1	1	0	1	1	0	0	1	64/32	0D90000–0D9FFFF	6C8000–6CFFFF
SA218	0	1	1	0	1	1	0	1	0	64/32	0DA0000–0DAFFFF	6D0000–6D7FFF
SA219	0	1	1	0	1	1	0	1	1	64/32	0DB0000–0DBFFFF	6D8000–6DFFFF
SA220	0	1	1	0	1	1	1	0	0	64/32	0DC0000–0DCFFFF	6E0000–6E7FFF
SA221	0	1	1	0	1	1	1	0	1	64/32	0DD0000–0DDFFFF	6E8000–6EFFFF
SA222	0	1	1	0	1	1	1	1	0	64/32	0DE0000–0DEFFFF	6F0000–6F7FFF
SA223	0	1	1	0	1	1	1	1	1	64/32	0DF0000–0DFFFFF	6F8000–6FFFFF
SA224	0	1	1	1	0	0	0	0	0	64/32	0E00000–0E0FFFF	700000–707FFF
SA225	0	1	1	1	0	0	0	0	1	64/32	0E10000–0E1FFFF	708000–70FFFF
SA226	0	1	1	1	0	0	0	1	0	64/32	0E20000–0E2FFFF	710000–717FFF
SA227	0	1	1	1	0	0	0	1	1	64/32	0E30000–0E3FFFF	718000–71FFFF
SA228	0	1	1	1	0	0	1	0	0	64/32	0E40000–0E4FFFF	720000–727FFF
SA229	0	1	1	1	0	0	1	0	1	64/32	0E50000–0E5FFFF	728000–72FFFF
SA230	0	1	1	1	0	0	1	1	0	64/32	0E60000–0E6FFFF	730000–737FFF
SA231	0	1	1	1	0	0	1	1	1	64/32	0E70000–0E7FFFF	738000–73FFFF
SA232	0	1	1	1	0	1	0	0	0	64/32	0E80000–0E8FFFF	740000–747FFF
SA233	0	1	1	1	0	1	0	0	1	64/32	0E90000–0E9FFFF	748000–74FFFF
SA234	0	1	1	1	0	1	0	1	0	64/32	0EA0000–0EAFFFF	750000–757FFF
SA235	0	1	1	1	0	1	0	1	1	64/32	0EB0000–0EBFFFF	758000–75FFFF
SA236	0	1	1	1	0	1	1	0	0	64/32	0EC0000–0ECFFFF	760000–767FFF
SA237	0	1	1	1	0	1	1	0	1	64/32	0ED0000–0EDFFFF	768000–76FFFF
SA238	0	1	1	1	0	1	1	1	0	64/32	0EE0000–0EEFFFF	770000–777FFF

Table 2.   Sector Address Table (Continued)

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA239	0	1	1	1	0	1	1	1	1	64/32	0EF0000–0EFFFFF	778000–77FFFF
SA240	0	1	1	1	1	0	0	0	0	64/32	0F00000–0F0FFFF	780000–787FFF
SA241	0	1	1	1	1	0	0	0	1	64/32	0F10000–0F1FFFF	788000–78FFFF
SA242	0	1	1	1	1	0	0	1	0	64/32	0F20000–0F2FFFF	790000–797FFF
SA243	0	1	1	1	1	0	0	1	1	64/32	0F30000–0F3FFFF	798000–79FFFF
SA244	0	1	1	1	1	0	1	0	0	64/32	0F40000–0F4FFFF	7A0000–7A7FFF
SA245	0	1	1	1	1	0	1	0	1	64/32	0F50000–0F5FFFF	7A8000–7AFFFF
SA246	0	1	1	1	1	0	1	1	0	64/32	0F60000–0F6FFFF	7B0000–7B7FFF
SA247	0	1	1	1	1	0	1	1	1	64/32	0F70000–0F7FFFF	7B8000–7BFFFF
SA248	0	1	1	1	1	1	0	0	0	64/32	0F80000–0F8FFFF	7C0000–7C7FFF
SA249	0	1	1	1	1	1	0	0	1	64/32	0F90000–0F9FFFF	7C8000–7CFFFF
SA250	0	1	1	1	1	1	0	1	0	64/32	0FA0000–0FAFFFF	7D0000–7D7FFF
SA251	0	1	1	1	1	1	0	1	1	64/32	0FB0000–0FBFFFF	7D8000–7DFFFF
SA252	0	1	1	1	1	1	1	0	0	64/32	0FC0000–0FCFFFF	7E0000–7E7FFF
SA253	0	1	1	1	1	1	1	0	1	64/32	0FD0000–0FDFFFF	7E8000–7EFFFF
SA254	0	1	1	1	1	1	1	1	0	64/32	0FE0000–0FEFFFF	7F0000–7F7FFF
SA255	0	1	1	1	1	1	1	1	1	64/32	0FF0000–0FFFFFF	7F8000–7FFFFF
SA256	1	0	0	0	0	0	0	0	0	64/32	1000000–100FFFF	800000–807FFF
SA257	1	0	0	0	0	0	0	0	1	64/32	1010000–101FFFF	808000–80FFFF
SA258	1	0	0	0	0	0	0	1	0	64/32	1020000–102FFFF	810000–817FFF
SA259	1	0	0	0	0	0	0	1	1	64/32	1030000–103FFFF	818000–81FFFF
SA260	1	0	0	0	0	0	1	0	0	64/32	1040000–104FFFF	820000–827FFF
SA261	1	0	0	0	0	0	1	0	1	64/32	1050000–105FFFF	828000–82FFFF
SA262	1	0	0	0	0	0	1	1	0	64/32	1060000–106FFFF	830000–837FFF
SA263	1	0	0	0	0	0	1	1	1	64/32	1070000–107FFFF	838000–83FFFF
SA264	1	0	0	0	0	1	0	0	0	64/32	1080000–108FFFF	840000–847FFF
SA265	1	0	0	0	0	1	0	0	1	64/32	1090000–109FFFF	848000–84FFFF
SA266	1	0	0	0	0	1	0	1	0	64/32	10A0000–10AFFFF	850000–857FFF
SA267	1	0	0	0	0	1	0	1	1	64/32	10B0000–10BFFFF	858000–85FFFF
SA268	1	0	0	0	0	1	1	0	0	64/32	10C0000–10CFFFF	860000–867FFF
SA269	1	0	0	0	0	1	1	0	1	64/32	10D0000–10DFFFF	868000–86FFFF
SA270	1	0	0	0	0	1	1	1	0	64/32	10E0000–10EFFFF	870000–877FFF
SA271	1	0	0	0	0	1	1	1	1	64/32	10F0000–10FFFFF	878000–87FFFF
SA272	1	0	0	0	1	0	0	0	0	64/32	1100000–110FFFF	880000–887FFF
SA273	1	0	0	0	1	0	0	0	1	64/32	1110000–111FFFF	888000–88FFFF
SA274	1	0	0	0	1	0	0	1	0	64/32	1120000–112FFFF	890000–897FFF
SA275	1	0	0	0	1	0	0	1	1	64/32	1130000–113FFFF	898000–89FFFF
SA276	1	0	0	0	1	0	1	0	0	64/32	1140000–114FFFF	8A0000–8A7FFF
SA277	1	0	0	0	1	0	1	0	1	64/32	1150000–115FFFF	8A8000–8AFFFF
SA278	1	0	0	0	1	0	1	1	0	64/32	1160000–116FFFF	8B0000–8B7FFF
SA279	1	0	0	0	1	0	1	1	1	64/32	1170000–117FFFF	8B8000–8BFFFF
SA280	1	0	0	0	1	1	0	0	0	64/32	1180000–118FFFF	8C0000–8C7FFF
SA281	1	0	0	0	1	1	0	0	1	64/32	1190000–119FFFF	8C8000–8CFFFF
SA282	1	0	0	0	1	1	0	1	0	64/32	11A0000–11AFFFF	8D0000–8D7FFF
SA283	1	0	0	0	1	1	0	1	1	64/32	11B0000–11BFFFF	8D8000–8DFFFF
SA284	1	0	0	0	1	1	1	0	0	64/32	11C0000–11CFFFF	8E0000–8E7FFF
SA285	1	0	0	0	1	1	1	0	1	64/32	11D0000–11DFFFF	8E8000–8EFFFF
SA286	1	0	0	0	1	1	1	1	0	64/32	11E0000–11EFFFF	8F0000–8F7FFF

Table 2. Sector Address Table (Continued)

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA287	1	0	0	0	1	1	1	1	1	64/32	11F0000–11FFFFF	8F8000–8FFFFF
SA288	1	0	0	1	0	0	0	0	0	64/32	1200000–120FFFF	900000–907FFF
SA289	1	0	0	1	0	0	0	0	1	64/32	1210000–121FFFF	908000–90FFFF
SA290	1	0	0	1	0	0	0	1	0	64/32	1220000–122FFFF	910000–917FFF
SA291	1	0	0	1	0	0	0	1	1	64/32	1230000–123FFFF	918000–91FFFF
SA292	1	0	0	1	0	0	1	0	0	64/32	1240000–124FFFF	920000–927FFF
SA293	1	0	0	1	0	0	1	0	1	64/32	1250000–125FFFF	928000–92FFFF
SA294	1	0	0	1	0	0	1	1	0	64/32	1260000–126FFFF	930000–937FFF
SA295	1	0	0	1	0	0	1	1	1	64/32	1270000–127FFFF	938000–93FFFF
SA296	1	0	0	1	0	1	0	0	0	64/32	1280000–128FFFF	940000–947FFF
SA297	1	0	0	1	0	1	0	0	1	64/32	1290000–129FFFF	948000–94FFFF
SA298	1	0	0	1	0	1	0	1	0	64/32	12A0000–12AFFFF	950000–957FFF
SA299	1	0	0	1	0	1	0	1	1	64/32	12B0000–12BFFFF	958000–95FFFF
SA300	1	0	0	1	0	1	1	0	0	64/32	12C0000–12CFFFF	960000–967FFF
SA301	1	0	0	1	0	1	1	0	1	64/32	12D0000–12DFFFF	968000–96FFFF
SA302	1	0	0	1	0	1	1	1	0	64/32	12E0000–12EFFFF	970000–977FFF
SA303	1	0	0	1	0	1	1	1	1	64/32	12F0000–12FFFFF	978000–97FFFF
SA304	1	0	0	1	1	0	0	0	0	64/32	1300000–130FFFF	980000–987FFF
SA305	1	0	0	1	1	0	0	0	1	64/32	1310000–131FFFF	988000–98FFFF
SA306	1	0	0	1	1	0	0	1	0	64/32	1320000–132FFFF	990000–997FFF
SA307	1	0	0	1	1	0	0	1	1	64/32	1330000–133FFFF	998000–99FFFF
SA308	1	0	0	1	1	0	1	0	0	64/32	1340000–134FFFF	9A0000–9A7FFF
SA309	1	0	0	1	1	0	1	0	1	64/32	1350000–135FFFF	9A8000–9AFFFF
SA310	1	0	0	1	1	0	1	1	0	64/32	1360000–136FFFF	9B0000–9B7FFF
SA311	1	0	0	1	1	0	1	1	1	64/32	1370000–137FFFF	9B8000–9BFFFF
SA312	1	0	0	1	1	1	0	0	0	64/32	1380000–138FFFF	9C0000–9C7FFF
SA313	1	0	0	1	1	1	0	0	1	64/32	1390000–139FFFF	9C8000–9CFFFF
SA314	1	0	0	1	1	1	0	1	0	64/32	13A0000–13AFFFF	9D0000–9D7FFF
SA315	1	0	0	1	1	1	0	1	1	64/32	13B0000–13BFFFF	9D8000–9DFFFF
SA316	1	0	0	1	1	1	1	0	0	64/32	13C0000–13CFFFF	9E0000–9E7FFF
SA317	1	0	0	1	1	1	1	0	1	64/32	13D0000–13DFFFF	9E8000–9EFFFF
SA318	1	0	0	1	1	1	1	1	0	64/32	13E0000–13EFFFF	9F0000–9F7FFF
SA319	1	0	0	1	1	1	1	1	1	64/32	13F0000–13FFFFF	9F8000–9FFFFF
SA320	1	0	1	0	0	0	0	0	0	64/32	1400000–140FFFF	A00000–A07FFF
SA321	1	0	1	0	0	0	0	0	1	64/32	1410000–141FFFF	A08000–A0FFFF
SA322	1	0	1	0	0	0	0	1	0	64/32	1420000–142FFFF	A10000–A17FFF
SA323	1	0	1	0	0	0	0	1	1	64/32	1430000–143FFFF	A18000–A1FFFF
SA324	1	0	1	0	0	0	1	0	0	64/32	1440000–144FFFF	A20000–A27FFF
SA325	1	0	1	0	0	0	1	0	1	64/32	1450000–145FFFF	A28000–A2FFFF
SA326	1	0	1	0	0	0	1	1	0	64/32	1460000–146FFFF	A30000–A37FFF
SA327	1	0	1	0	0	0	1	1	1	64/32	1470000–147FFFF	A38000–A3FFFF
SA328	1	0	1	0	0	1	0	0	0	64/32	1480000–148FFFF	A40000–A47FFF
SA329	1	0	1	0	0	1	0	0	1	64/32	1490000–149FFFF	A48000–A4FFFF
SA330	1	0	1	0	0	1	0	1	0	64/32	14A0000–14AFFFF	A50000–A57FFF
SA331	1	0	1	0	0	1	0	1	1	64/32	14B0000–14BFFFF	A58000–A5FFFF
SA332	1	0	1	0	0	1	1	0	0	64/32	14C0000–14CFFFF	A60000–A67FFF
SA333	1	0	1	0	0	1	1	0	1	64/32	14D0000–14DFFFF	A68000–A6FFFF
SA334	1	0	1	0	0	1	1	1	0	64/32	14E0000–14EFFFF	A70000–A77FFF

Table 2. Sector Address Table (Continued)

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA335	1	0	1	0	0	1	1	1	1	64/32	14F0000–14FFFFF	A78000–A7FFFF
SA336	1	0	1	0	1	0	0	0	0	64/32	1500000–150FFFF	A80000–A87FFF
SA337	1	0	1	0	1	0	0	0	1	64/32	1510000–151FFFF	A88000–A8FFFF
SA338	1	0	1	0	1	0	0	1	0	64/32	1520000–152FFFF	A90000–A97FFF
SA339	1	0	1	0	1	0	0	1	1	64/32	1530000–153FFFF	A98000–A9FFFF
SA340	1	0	1	0	1	0	1	0	0	64/32	1540000–154FFFF	AA0000–AA7FFF
SA341	1	0	1	0	1	0	1	0	1	64/32	1550000–155FFFF	AA8000–AAFFFF
SA342	1	0	1	0	1	0	1	1	0	64/32	1560000–156FFFF	AB0000–AB7FFF
SA343	1	0	1	0	1	0	1	1	1	64/32	1570000–157FFFF	AB8000–ABFFFF
SA344	1	0	1	0	1	1	0	0	0	64/32	1580000–158FFFF	AC0000–AC7FFF
SA345	1	0	1	0	1	1	0	0	1	64/32	1590000–159FFFF	AC8000–ACFFFF
SA346	1	0	1	0	1	1	0	1	0	64/32	15A0000–15AFFFF	AD0000–AD7FFF
SA347	1	0	1	0	1	1	0	1	1	64/32	15B0000–15BFFFF	AD8000–ADFFFF
SA348	1	0	1	0	1	1	1	0	0	64/32	15C0000–15CFFFF	AE0000–AE7FFF
SA349	1	0	1	0	1	1	1	0	1	64/32	15D0000–15DFFFF	AE8000–AEFFFF
SA350	1	0	1	0	1	1	1	1	0	64/32	15E0000–15EFFFF	AF0000–AF7FFF
SA351	1	0	1	0	1	1	1	1	1	64/32	15F0000–15FFFFF	AF8000–AFFFFF
SA352	1	0	1	1	0	0	0	0	0	64/32	1600000–160FFFF	B00000–B07FFF
SA353	1	0	1	1	0	0	0	0	1	64/32	1610000–161FFFF	B08000–B0FFFF
SA354	1	0	1	1	0	0	0	1	0	64/32	1620000–162FFFF	B10000–B17FFF
SA355	1	0	1	1	0	0	0	1	1	64/32	1630000–163FFFF	B18000–B1FFFF
SA356	1	0	1	1	0	0	1	0	0	64/32	1640000–164FFFF	B20000–B27FFF
SA357	1	0	1	1	0	0	1	0	1	64/32	1650000–165FFFF	B28000–B2FFFF
SA358	1	0	1	1	0	0	1	1	0	64/32	1660000–166FFFF	B30000–B37FFF
SA359	1	0	1	1	0	0	1	1	1	64/32	1670000–167FFFF	B38000–B3FFFF
SA360	1	0	1	1	0	1	0	0	0	64/32	1680000–168FFFF	B40000–B47FFF
SA361	1	0	1	1	0	1	0	0	1	64/32	1690000–169FFFF	B48000–B4FFFF
SA362	1	0	1	1	0	1	0	1	0	64/32	16A0000–16AFFFF	B50000–B57FFF
SA363	1	0	1	1	0	1	0	1	1	64/32	16B0000–16BFFFF	B58000–B5FFFF
SA364	1	0	1	1	0	1	1	0	0	64/32	16C0000–16CFFFF	B60000–B67FFF
SA365	1	0	1	1	0	1	1	0	1	64/32	16D0000–16DFFFF	B68000–B6FFFF
SA366	1	0	1	1	0	1	1	1	0	64/32	16E0000–16EFFFF	B70000–B77FFF
SA367	1	0	1	1	0	1	1	1	1	64/32	16F0000–16FFFFF	B78000–B7FFFF
SA368	1	0	1	1	1	0	0	0	0	64/32	1700000–170FFFF	B80000–B87FFF
SA369	1	0	1	1	1	0	0	0	1	64/32	1710000–171FFFF	B88000–B8FFFF
SA370	1	0	1	1	1	0	0	1	0	64/32	1720000–172FFFF	B90000–B97FFF
SA371	1	0	1	1	1	0	0	1	1	64/32	1730000–173FFFF	B98000–B9FFFF
SA372	1	0	1	1	1	0	1	0	0	64/32	1740000–174FFFF	BA0000–BA7FFF
SA373	1	0	1	1	1	0	1	0	1	64/32	1750000–175FFFF	BA8000–BAFFFF
SA374	1	0	1	1	1	0	1	1	0	64/32	1760000–176FFFF	BB0000–BB7FFF
SA375	1	0	1	1	1	0	1	1	1	64/32	1770000–177FFFF	BB8000–BBFFFF
SA376	1	0	1	1	1	1	0	0	0	64/32	1780000–178FFFF	BC0000–BC7FFF
SA377	1	0	1	1	1	1	0	0	1	64/32	1790000–179FFFF	BC8000–BCFFFF
SA378	1	0	1	1	1	1	0	1	0	64/32	17A0000–17AFFFF	BD0000–BD7FFF
SA379	1	0	1	1	1	1	0	1	1	64/32	17B0000–17BFFFF	BD8000–BDFFFF
SA380	1	0	1	1	1	1	1	0	0	64/32	17C0000–17CFFFF	BE0000–BE7FFF
SA381	1	0	1	1	1	1	1	0	1	64/32	17D0000–17DFFFF	BE8000–BEFFFF
SA382	1	0	1	1	1	1	1	1	0	64/32	17E0000–17EFFFF	BF0000–BF7FFF

Table 2.   Sector Address Table (Continued)

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA383	1	0	1	1	1	1	1	1	1	64/32	17F0000–17FFFFF	BF8000–BFFFFF
SA384	1	1	0	0	0	0	0	0	0	64/32	1800000–180FFFF	C00000–C07FFF
SA385	1	1	0	0	0	0	0	0	1	64/32	1810000–181FFFF	C08000–C0FFFF
SA386	1	1	0	0	0	0	0	1	0	64/32	1820000–182FFFF	C10000–C17FFF
SA387	1	1	0	0	0	0	0	1	1	64/32	1830000–183FFFF	C18000–C1FFFF
SA388	1	1	0	0	0	0	1	0	0	64/32	1840000–184FFFF	C20000–C27FFF
SA389	1	1	0	0	0	0	1	0	1	64/32	1850000–185FFFF	C28000–C2FFFF
SA390	1	1	0	0	0	0	1	1	0	64/32	1860000–186FFFF	C30000–C37FFF
SA391	1	1	0	0	0	0	1	1	1	64/32	1870000–187FFFF	C38000–C3FFFF
SA392	1	1	0	0	0	1	0	0	0	64/32	1880000–188FFFF	C40000–C47FFF
SA393	1	1	0	0	0	1	0	0	1	64/32	1890000–189FFFF	C48000–C4FFFF
SA394	1	1	0	0	0	1	0	1	0	64/32	18A0000–18AFFFF	C50000–C57FFF
SA395	1	1	0	0	0	1	0	1	1	64/32	18B0000–18BFFFF	C58000–C5FFFF
SA396	1	1	0	0	0	1	1	0	0	64/32	18C0000–18CFFFF	C60000–C67FFF
SA397	1	1	0	0	0	1	1	0	1	64/32	18D0000–18DFFFF	C68000–C6FFFF
SA398	1	1	0	0	0	1	1	1	0	64/32	18E0000–18EFFFF	C70000–C77FFF
SA399	1	1	0	0	0	1	1	1	1	64/32	18F0000–18FFFFF	C78000–C7FFFF
SA400	1	1	0	0	1	0	0	0	0	64/32	1900000–190FFFF	C80000–C87FFF
SA401	1	1	0	0	1	0	0	0	1	64/32	1910000–191FFFF	C88000–C8FFFF
SA402	1	1	0	0	1	0	0	1	0	64/32	1920000–192FFFF	C90000–C97FFF
SA403	1	1	0	0	1	0	0	1	1	64/32	1930000–193FFFF	C98000–C9FFFF
SA404	1	1	0	0	1	0	1	0	0	64/32	1940000–194FFFF	CA0000–CA7FFF
SA405	1	1	0	0	1	0	1	0	1	64/32	1950000–195FFFF	CA8000–CAFFFF
SA406	1	1	0	0	1	0	1	1	0	64/32	1960000–196FFFF	CB0000–CB7FFF
SA407	1	1	0	0	1	0	1	1	1	64/32	1970000–197FFFF	CB8000–CBFFFF
SA408	1	1	0	0	1	1	0	0	0	64/32	1980000–198FFFF	CC0000–CC7FFF
SA409	1	1	0	0	1	1	0	0	1	64/32	1990000–199FFFF	CC8000–CCFFFF
SA410	1	1	0	0	1	1	0	1	0	64/32	19A0000–19AFFFF	CD0000–CD7FFF
SA411	1	1	0	0	1	1	0	1	1	64/32	19B0000–19BFFFF	CD8000–CDFFFF
SA412	1	1	0	0	1	1	1	0	0	64/32	19C0000–19CFFFF	CE0000–CE7FFF
SA413	1	1	0	0	1	1	1	0	1	64/32	19D0000–19DFFFF	CE8000–CEFFFF
SA414	1	1	0	0	1	1	1	1	0	64/32	19E0000–19EFFFF	CF0000–CF7FFF
SA415	1	1	0	0	1	1	1	1	1	64/32	19F0000–19FFFFF	CF8000–CFFFFF
SA416	1	1	0	1	0	0	0	0	0	64/32	1A00000–1A0FFFF	D00000–D07FFF
SA417	1	1	0	1	0	0	0	0	1	64/32	1A10000–1A1FFFF	D08000–D0FFFF
SA418	1	1	0	1	0	0	0	1	0	64/32	1A20000–1A2FFFF	D10000–D17FFF
SA419	1	1	0	1	0	0	0	1	1	64/32	1A30000–1A3FFFF	D18000–D1FFFF
SA420	1	1	0	1	0	0	1	0	0	64/32	1A40000–1A4FFFF	D20000–D27FFF
SA421	1	1	0	1	0	0	1	0	1	64/32	1A50000–1A5FFFF	D28000–D2FFFF
SA422	1	1	0	1	0	0	1	1	0	64/32	1A60000–1A6FFFF	D30000–D37FFF
SA423	1	1	0	1	0	0	1	1	1	64/32	1A70000–1A7FFFF	D38000–D3FFFF
SA424	1	1	0	1	0	1	0	0	0	64/32	1A80000–1A8FFFF	D40000–D47FFF
SA425	1	1	0	1	0	1	0	0	1	64/32	1A90000–1A9FFFF	D48000–D4FFFF
SA426	1	1	0	1	0	1	0	1	0	64/32	1AA0000–1AAFFFF	D50000–D57FFF
SA427	1	1	0	1	0	1	0	1	1	64/32	1AB0000–1ABFFFF	D58000–D5FFFF
SA428	1	1	0	1	0	1	1	0	0	64/32	1AC0000–1ACFFFF	D60000–D67FFF
SA429	1	1	0	1	0	1	1	0	1	64/32	1AD0000–1ADFFFF	D68000–D6FFFF
SA430	1	1	0	1	0	1	1	1	0	64/32	1AE0000–1AEFFFF	D70000–D77FFF

Table 2. Sector Address Table (Continued)

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA431	1	1	0	1	0	1	1	1	1	64/32	1AF0000–1AFFFFF	D78000–D7FFFF
SA432	1	1	0	1	1	0	0	0	0	64/32	1B00000–1B0FFFF	D80000–D87FFF
SA433	1	1	0	1	1	0	0	0	1	64/32	1B10000–1B1FFFF	D88000–D8FFFF
SA434	1	1	0	1	1	0	0	1	0	64/32	1B20000–1B2FFFF	D90000–D97FFF
SA435	1	1	0	1	1	0	0	1	1	64/32	1B30000–1B3FFFF	D98000–D9FFFF
SA436	1	1	0	1	1	0	1	0	0	64/32	1B40000–1B4FFFF	DA0000–DA7FFF
SA437	1	1	0	1	1	0	1	0	1	64/32	1B50000–1B5FFFF	DA8000–DAFFFF
SA438	1	1	0	1	1	0	1	1	0	64/32	1B60000–1B6FFFF	DB0000–DB7FFF
SA439	1	1	0	1	1	0	1	1	1	64/32	1B70000–1B7FFFF	DB8000–DBFFFF
SA440	1	1	0	1	1	1	0	0	0	64/32	1B80000–1B8FFFF	DC0000–DC7FFF
SA441	1	1	0	1	1	1	0	0	1	64/32	1B90000–1B9FFFF	DC8000–DCFFFF
SA442	1	1	0	1	1	1	0	1	0	64/32	1BA0000–1BAFFFF	DD0000–DD7FFF
SA443	1	1	0	1	1	1	0	1	1	64/32	1BB0000–1BBFFFF	DD8000–DDFFFF
SA444	1	1	0	1	1	1	1	0	0	64/32	1BC0000–1BCFFFF	DE0000–DE7FFF
SA445	1	1	0	1	1	1	1	0	1	64/32	1BD0000–1BDFFFF	DE8000–DEFFFF
SA446	1	1	0	1	1	1	1	1	0	64/32	1BE0000–1BEFFFF	DF0000–DF7FFF
SA447	1	1	0	1	1	1	1	1	1	64/32	1BF0000–1BFFFFF	DF8000–DFFFFF
SA448	1	1	1	0	0	0	0	0	0	64/32	1C00000–1C0FFFF	E00000–E07FFF
SA449	1	1	1	0	0	0	0	0	1	64/32	1C10000–1C1FFFF	E08000–E0FFFF
SA450	1	1	1	0	0	0	0	1	0	64/32	1C20000–1C2FFFF	E10000–E17FFF
SA451	1	1	1	0	0	0	0	1	1	64/32	1C30000–1C3FFFF	E18000–E1FFFF
SA452	1	1	1	0	0	0	1	0	0	64/32	1C40000–1C4FFFF	E20000–E27FFF
SA453	1	1	1	0	0	0	1	0	1	64/32	1C50000–1C5FFFF	E28000–E2FFFF
SA454	1	1	1	0	0	0	1	1	0	64/32	1C60000–1C6FFFF	E30000–E37FFF
SA455	1	1	1	0	0	0	1	1	1	64/32	1C70000–1C7FFFF	E38000–E3FFFF
SA456	1	1	1	0	0	1	0	0	0	64/32	1C80000–1C8FFFF	E40000–E47FFF
SA457	1	1	1	0	0	1	0	0	1	64/32	1C90000–1C9FFFF	E48000–E4FFFF
SA458	1	1	1	0	0	1	0	1	0	64/32	1CA0000–1CAFFFF	E50000–E57FFF
SA459	1	1	1	0	0	1	0	1	1	64/32	1CB0000–1CBFFFF	E58000–E5FFFF
SA460	1	1	1	0	0	1	1	0	0	64/32	1CC0000–1CCFFFF	E60000–E67FFF
SA461	1	1	1	0	0	1	1	0	1	64/32	1CD0000–1CDFFFF	E68000–E6FFFF
SA462	1	1	1	0	0	1	1	1	0	64/32	1CE0000–1CEFFFF	E70000–E77FFF
SA463	1	1	1	0	0	1	1	1	1	64/32	1CF0000–1CFFFFF	E78000–E7FFFF
SA464	1	1	1	0	1	0	0	0	0	64/32	1D00000–1D0FFFF	E80000–E87FFF
SA465	1	1	1	0	1	0	0	0	1	64/32	1D10000–1D1FFFF	E88000–E8FFFF
SA466	1	1	1	0	1	0	0	1	0	64/32	1D20000–1D2FFFF	E90000–E97FFF
SA467	1	1	1	0	1	0	0	1	1	64/32	1D30000–1D3FFFF	E98000–E9FFFF
SA468	1	1	1	0	1	0	1	0	0	64/32	1D40000–1D4FFFF	EA0000–EA7FFF
SA469	1	1	1	0	1	0	1	0	1	64/32	1D50000–1D5FFFF	EA8000–EAFFFF
SA470	1	1	1	0	1	0	1	1	0	64/32	1D60000–1D6FFFF	EB0000–EB7FFF
SA471	1	1	1	0	1	0	1	1	1	64/32	1D70000–1D7FFFF	EB8000–EBFFFF
SA472	1	1	1	0	1	1	0	0	0	64/32	1D80000–1D8FFFF	EC0000–EC7FFF
SA473	1	1	1	0	1	1	0	0	1	64/32	1D90000–1D9FFFF	EC8000–ECFFFF
SA474	1	1	1	0	1	1	0	1	0	64/32	1DA0000–1DAFFFF	ED0000–ED7FFF
SA475	1	1	1	0	1	1	0	1	1	64/32	1DB0000–1DBFFFF	ED8000–EDFFFF
SA476	1	1	1	0	1	1	1	0	0	64/32	1DC0000–1DCFFFF	EE0000–EE7FFF
SA477	1	1	1	0	1	1	1	0	1	64/32	1DD0000–1DDFFFF	EE8000–EEFFFF
SA478	1	1	1	0	1	1	1	1	0	64/32	1DE0000–1DEFFFF	EF0000–EF7FFF

Table 2. Sector Address Table (Continued)

Sector	A23–A15									Sector Size (Kbytes/Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA479	1	1	1	0	1	1	1	1	1	64/32	1DF0000–1DFFFFF	EF8000–EFFFFF
SA480	1	1	1	1	0	0	0	0	0	64/32	1E00000–1E0FFFF	F00000–F07FFF
SA481	1	1	1	1	0	0	0	0	1	64/32	1E10000–1E1FFFF	F08000–F0FFFF
SA482	1	1	1	1	0	0	0	1	0	64/32	1E20000–1E2FFFF	F10000–F17FFF
SA483	1	1	1	1	0	0	0	1	1	64/32	1E30000–1E3FFFF	F18000–F1FFFF
SA484	1	1	1	1	0	0	1	0	0	64/32	1E40000–1E4FFFF	F20000–F27FFF
SA485	1	1	1	1	0	0	1	0	1	64/32	1E50000–1E5FFFF	F28000–F2FFFF
SA486	1	1	1	1	0	0	1	1	0	64/32	1E60000–1E6FFFF	F30000–F37FFF
SA487	1	1	1	1	0	0	1	1	1	64/32	1E70000–1E7FFFF	F38000–F3FFFF
SA488	1	1	1	1	0	1	0	0	0	64/32	1E80000–1E8FFFF	F40000–F47FFF
SA489	1	1	1	1	0	1	0	0	1	64/32	1E90000–1E9FFFF	F48000–F4FFFF
SA490	1	1	1	1	0	1	0	1	0	64/32	1EA0000–1EAFFFF	F50000–F57FFF
SA491	1	1	1	1	0	1	0	1	1	64/32	1EB0000–1EBFFFF	F58000–F5FFFF
SA492	1	1	1	1	0	1	1	0	0	64/32	1EC0000–1ECFFFF	F60000–F67FFF
SA493	1	1	1	1	0	1	1	0	1	64/32	1ED0000–1EDFFFF	F68000–F6FFFF
SA494	1	1	1	1	0	1	1	1	0	64/32	1EE0000–1EEFFFF	F70000–F77FFF
SA495	1	1	1	1	0	1	1	1	1	64/32	1EF0000–1EFFFFF	F78000–F7FFFF
SA496	1	1	1	1	1	0	0	0	0	64/32	1F00000–1F0FFFF	F80000–F87FFF
SA497	1	1	1	1	1	0	0	0	1	64/32	1F10000–1F1FFFF	F88000–F8FFFF
SA498	1	1	1	1	1	0	0	1	0	64/32	1F20000–1F2FFFF	F90000–F97FFF
SA499	1	1	1	1	1	0	0	1	1	64/32	1F30000–1F3FFFF	F98000–F9FFFF
SA500	1	1	1	1	1	0	1	0	0	64/32	1F40000–1F4FFFF	FA0000–FA7FFF
SA501	1	1	1	1	1	0	1	0	1	64/32	1F50000–1F5FFFF	FA8000–FAFFFF
SA502	1	1	1	1	1	0	1	1	0	64/32	1F60000–1F6FFFF	FB0000–FB7FFF
SA503	1	1	1	1	1	0	1	1	1	64/32	1F70000–1F7FFFF	FB8000–FBFFFF
SA504	1	1	1	1	1	1	0	0	0	64/32	1F80000–1F8FFFF	FC0000–FC7FFF
SA505	1	1	1	1	1	1	0	0	1	64/32	1F90000–1F9FFFF	FC8000–FCFFFF
SA506	1	1	1	1	1	1	0	1	0	64/32	1FA0000–1FAFFFF	FD0000–FD7FFF
SA507	1	1	1	1	1	1	0	1	1	64/32	1FB0000–1FBFFFF	FD8000–FDFFFF
SA508	1	1	1	1	1	1	1	0	0	64/32	1FC0000–1FCFFFF	FE0000–FE7FFF
SA509	1	1	1	1	1	1	1	0	1	64/32	1FD0000–1FDFFFF	FE8000–FEFFFF
SA510	1	1	1	1	1	1	1	1	0	64/32	1FE0000–1FEFFFF	FF0000–FF7FFF
SA511	1	1	1	1	1	1	1	1	1	64/32	1FF0000–1FFFFFF	FF8000–FFFFFF

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector group protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins A6, A3, A2, A1, and A0 must be as shown in Table 3.

In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 2). Table 3 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Tables 11 and 12. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 3. Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE#	A22 to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15 BYTE# = V_{IH}	DQ8 to DQ15 BYTE# = V_{IL}	DQ7 to DQ0
Manufacturer ID: AMD		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00	X	01h
Device ID	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	12h
	Cycle 3										H	H	H	22	X	01h
Sector Group Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)
SecSi Sector Indicator Bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	98h (factory locked), 18h (not factory locked)
SecSi Sector Indicator Bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	88h (factory locked), 08h (not factory locked)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.*

Sector Group Protection and Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection can be implemented via two methods.

Sector group protection/unprotection requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 23 shows the timing diagram. For sector group unprotect, all unprotected sector groups must first be protected prior to the first sector group unprotect write cycle. *Note that the sector group unprotect algorithm unprotects all sector groups in parallel. All previously protected sector groups must be individually re-protected.*

The device is shipped with all sector groups unprotected. AMD offers the option of programming and protecting sector groups at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector group is protected or unprotected. See the Autoselect Mode section for details.

Table 4. Sector Group Protection/Unprotection Address Table

Sector Group	A23–A15
SA0	000000000
SA1	000000001
SA2	000000010
SA3	000000011
SA4–SA7	0000001xx
SA8–SA11	0000010xx
SA12–SA15	0000011xx
SA16–SA19	0000100xx
SA20–SA23	0000101xx
SA24–SA27	0000110xx
SA28–SA31	0000111xx
SA32–SA35	0001000xx
SA36–SA39	0001001xx
SA40–SA43	0001010xx
SA44–SA47	0001011xx
SA48–SA51	0001100xx
SA52–SA55	0001101xx
SA56–SA59	0001110xx
SA60–SA63	0001111xx
SA64–SA67	0010000xx

Sector Group	A23–A15
SA68–SA71	0010001xx
SA72–SA75	0010010xx
SA76–SA79	0010011xx
SA80–SA83	0010100xx
SA84–SA87	0010101xx
SA88–SA91	0010110xx
SA92–SA95	0010111xx
SA96–SA99	0011000xx
SA100–SA103	0011001xx
SA104–SA107	0011010xx
SA108–SA111	0011011xx
SA112–SA115	0011100xx
SA116–SA119	0011101xx
SA120–SA123	0011110xx
SA124–SA127	0011111xx
SA128–SA131	0100000xx
SA132–SA135	0100001xx
SA136–SA139	0100010xx
SA140–SA143	0100011xx
SA144–SA147	0100100xx
SA148–SA151	0100101xx
SA152–SA155	0100110xx
SA156–SA159	0100111xx
SA160–SA163	0101000xx
SA164–SA167	0101001xx
SA168–SA171	0101010xx
SA172–SA175	0101011xx
SA176–SA179	0101100xx
SA180–SA183	0101101xx
SA184–SA187	0101110xx
SA188–SA191	0101111xx
SA192–SA195	0110000xx
SA196–SA199	0110001xx
SA200–SA203	0110010xx
SA204–SA207	0110011xx
SA208–SA211	0110100xx
SA212–SA215	0110101xx
SA216–SA219	0110110xx
SA220–SA223	0110111xx
SA224–SA227	0111000xx
SA228–SA231	0111001xx
SA232–SA235	0111010xx
SA236–SA239	0111011xx
SA240–SA243	0111100xx
SA244–SA247	0111101xx

Sector Group	A23–A15
SA248–SA251	0111110xx
SA252–SA255	0111111xx
SA256–SA259	1000000xx
SA260–SA263	1000001xx
SA264–SA267	1000010xx
SA268–SA271	1000011xx
SA272–SA275	1000100xx
SA276–SA279	1000101xx
SA280–SA283	1000110xx
SA284–SA287	1000111xx
SA288–SA291	1001000xx
SA292–SA295	1001001xx
SA296–SA299	1001010xx
SA300–SA303	1001011xx
SA304–SA307	1001100xx
SA308–SA311	1001101xx
SA312–SA315	1001110xx
SA316–SA319	1001111xx
SA320–SA323	1010000xx
SA324–SA327	1010001xx
SA328–SA331	1010010xx
SA332–SA335	1010011xx
SA336–SA339	1010100xx
SA340–SA343	1010101xx
SA344–SA347	1010110xx
SA348–SA351	1010111xx
SA352–SA355	1011000xx
SA356–SA359	1011001xx
SA360–SA363	1011010xx
SA364–SA367	1011011xx
SA368–SA371	1011100xx
SA372–SA375	1011101xx
SA376–SA379	1011110xx
SA380–SA383	1011111xx
SA384–SA387	1100000xx
SA388–SA391	1100001xx
SA392–SA395	1100010xx
SA396–SA399	1100011xx
SA400–SA403	1100100xx
SA404–SA407	1100101xx
SA408–SA411	1100110xx
SA412–SA415	1100111xx
SA416–SA419	1101000xx
SA420–SA423	1101001xx
SA424–SA427	1101010xx

Sector Group	A23–A15
SA428–SA431	1101011xx
SA432–SA435	1101100xx
SA436–SA439	1101101xx
SA440–SA443	1101110xx
SA444–SA447	1101111xx
SA448–SA451	1110000xx
SA452–SA455	1110001xx
SA456–SA459	1110010xx
SA460–SA463	1110011xx
SA464–SA467	1110100xx
SA468–SA471	1110101xx
SA472–SA475	1110110xx
SA476–SA479	1110111xx
SA480–SA483	1111000xx
SA484–SA487	1111001xx
SA488–SA491	1111010xx
SA492–SA495	1111011xx
SA496–SA499	1111100xx
SA500–SA503	1111101xx
SA504–SA507	1111110xx
SA508	111111100
SA509	111111101
SA510	111111110
SA511	111111111

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting the first or last sector without using V_{ID}. Write Protect is one of two functions provided by the WP#/ACC input.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the first or last sector independently of whether those sectors were protected or unprotected using the method described in "Sector Group Protection and Unprotection". Note that if WP#/ACC is at V_{IL} when the device is in the standby mode, the maximum input load current is increased. See the table in "DC Characteristics".

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the first or last sector was previously set to be protected or unprotected using the method described in "Sector Group Protection and Unprotection". *Note that WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sector groups can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sector groups are protected again. Figure 1 shows the algorithm, and Figure 22 shows the timing diagrams, for this feature.
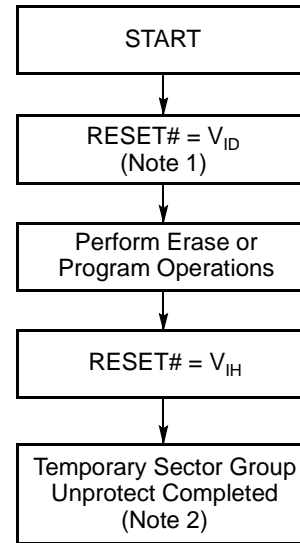
Notes:
1. *All protected sector groups unprotected (If WP# = V_{IL}, the first or last sector will remain protected).*
2. *All previously protected sector groups are protected once again.*

Figure 1. Temporary Sector Group Unprotect Operation

Sector Group Protect Algorithm

START

PLSCNT = 1

RESET# = V_{ID}

Wait 1 µs

First Write Cycle = 60h? — No → Temporary Sector Group Unprotect Mode

Yes

Set up sector group address

Sector Group Protect: Write 60h to sector group address with A6 = 0, A1 = 1, A0 = 0

Wait 150 µs

Verify Sector Group Protect: Write 40h to sector group address twith A6 = 0, A1 = 1, A0 = 0

Read from sector group address with A6 = 0, A1 = 1, A0 = 0

Data = 01h? — No → PLSCNT = 25? — No → Increment PLSCNT

PLSCNT = 25? — Yes → Device failed

Data = 01h? — Yes → Protect another sector group? — Yes → Set up sector group address

Protect another sector group? — No

Remove V_{ID} from RESET#

Write reset command

Sector Group Protect complete

Sector Group Unprotect Algorithm

START

PLSCNT = 1

RESET# = V_{ID}

Wait 1 µs

First Write Cycle = 60h? — No → Temporary Sector Group Unprotect Mode

Yes

All sector groups protected? — No → **Protect all sector groups:** The indicated portion of the sector group protect algorithm must be performed for all unprotected sector groups prior to issuing the first sector group unprotect address

Reset PLSCNT = 1

All sector groups protected? — Yes

Set up first sector group address

Sector Group Unprotect: Write 60h to sector group address with A6 = 1, A1 = 1, A0 = 0

Wait 15 ms

Verify Sector Group Unprotect: Write 40h to sector group address with A6 = 1, A1 = 1, A0 = 0

Read from sector group address with A6 = 1, A1 = 1, A0 = 0

Data = 00h? — No → PLSCNT = 1000? — No → Increment PLSCNT

PLSCNT = 1000? — Yes → Device failed

Data = 00h? — Yes → Last sector group verified? — No → Set up next sector group address

Last sector group verified? — Yes

Remove V_{ID} from RESET#

Write reset command

Sector Group Unprotect complete

Figure 2.   In-System Sector Group Protect/Unprotect Algorithms

SecSi (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 256 bytes in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

AMD offers the device with the SecSi Sector either customer lockable (standard shipping option) or factory locked (contact an AMD sales representative for ordering information). The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the SecSi Sector Indicator Bit permanently set to a "0." The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "1." Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

The SecSi sector address space in this device is allocated as follows:

Table 5.   SecSi Sector Contents

SecSi Sector Address Range	Customer Lockable	ESN Factory Locked	ExpressFlash Factory Locked
000000h–000007h	Determined by customer	ESN	ESN or determined by customer
000008h–00007Fh		Unavailable	Determined by customer

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte SecSi sector.

The system may program the SecSi Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions.

Programming and protecting the SecSi Sector must be used with caution since, once protected, there is no procedure available for unprotecting the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either V_{IH} or V_{ID}.* This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.

- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 3.

Once the SecSi Sector is programmed, locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing within the remainder of the array.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In devices with an ESN, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. An ESN Factory Locked device has an 16-byte random ESN at addresses 000000h–000007h. Please contact your local AMD sales representative for details on ordering ESN Factory Locked devices.

Customers may opt to have their code programmed by AMD through the AMD ExpressFlash service (Express Flash Factory Locked). The devices are then shipped from AMD's factory with the SecSi Sector permanently locked. Contact an AMD representative for details on using AMD's ExpressFlash service.

for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Figure 3. SecSi Sector Protect Verify

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Tables 11 and 12

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 6–9. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device

enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 6–9. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact an AMD representative for copies of these documents.

Table 6.   CFI Query Identification String

Addresses (x16)	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 7.   System Interface String

Addresses (x16)	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0007h	Typical timeout per single byte/word write 2^N µs
20h	0007h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	000Ah	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0001h	Max. timeout for byte/word write 2^N times typical
24h	0005h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 8.   Device Geometry Definition

Addresses (x16)	Data	Description
27h	0019h	Device Size = 2^N byte
28h 29h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0005h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0001h	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	00FFh 0001h 0000h 0001h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information (refer to CFI publication 100)
35h 36h 37h 38h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

Table 9. Primary Vendor-Specific Extended Query

Addresses (x16)	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string "PRI"
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0008h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0010b = 0.23 µm MirrorBit
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0004h	Sector Protect/Unprotect scheme 04 = 29LV800 mode
4Ah	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors in Bank
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0001h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0004h/ 0005h	Top/Bottom Boot Sector Flag 00h = Uniform Device without WP# protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Tables 11 and 12 define the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state.* A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens

first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any

non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations table provides the read parameters, and Figure 13 shows the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected.

Table 12 shows the address and data requirements. This method is an alternative to that shown in Table 3, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence:

■ A read cycle at address XX00h returns the manufacturer code.

■ Three read cycles at addresses 01h, 0Eh, and 0Fh return the device code.

■ A read cycle to an address containing a sector address (SA), and the address 02h on A7–A0 in word mode returns 01h if the sector is protected, or 00h if it is unprotected.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Enter SecSi Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing an 8-word/16-byte random Electronic Serial Number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. Tables 11 and 12 show the address and data requirements for both command sequences. See also "SecSi (Secured Silicon) Sector Flash Memory Region" for further information. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Word/Byte Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Tables 11 and 12 show the

address and data requirements for the word program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.* Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Tables 11 and 12 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. (See Table 9).

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initi-

ated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}–A_4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

■ Load a value that is greater than the page buffer size during the Number of Locations to Program step.

■ Write to an address in a sector different than the one specified during the Write-Buffer-Load command.

■ Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.

■ Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Accelerated Program

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

Figure 5 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 16 for timing diagrams.

Figure 4.   Write Buffer Programming Operation
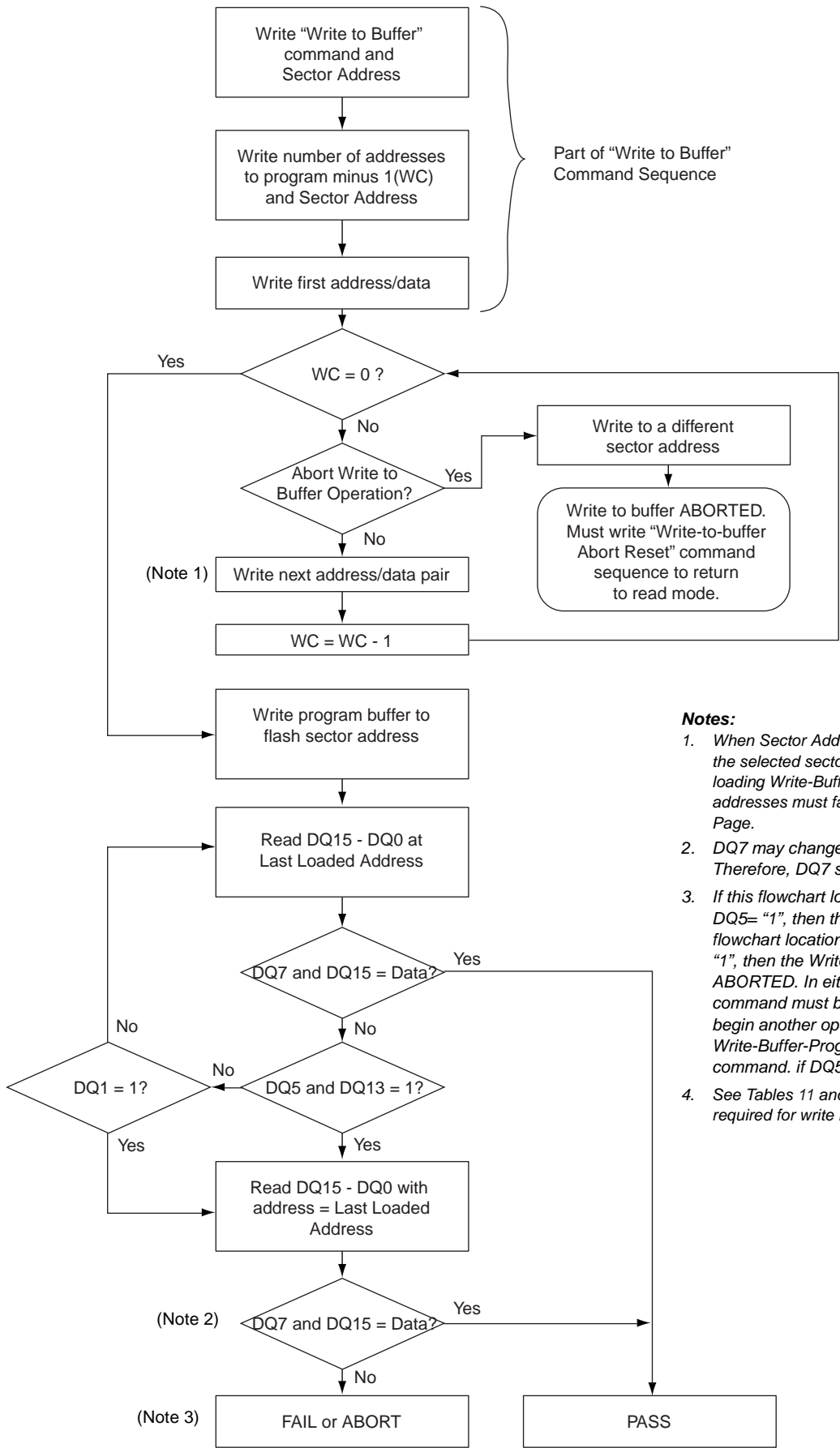
Notes:

1. When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.

2. DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.

3. If this flowchart location was reached because DQ5= "1", then the device FAILED. If this flowchart location was reached because DQ1= "1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If DQ1=1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5=1, write the Reset command.

4. See Tables 11 and 12 for command sequences required for write buffer programming.

Note: *See Tables 11 and 12 for program command sequence.*

Figure 5.   Program Operation

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 μs maximum (5μs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the SecSi Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

```
┌─────────────────────────┐
│   Program Operation      │
│   or Write-to-Buffer     │
│   Sequence in Progress   │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐        Write Program Suspend
│   Write address/data     │        Command Sequence
│   XXXh/B0B0h             │        Command is also valid for
└─────────────────────────┘        Erase-suspended-program
            │                       operations
            ▼
┌─────────────────────────┐
│   Wait 15 µs             │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐        Autoselect and SecSi Sector
│   Read data as           │        read operations are also allowed
│   required               │        Data cannot be read from erase- or
└─────────────────────────┘        program-suspended sectors
            │
            ▼
         ◇ Done ◇
  No ◇── reading? ──◇
            │
            │ Yes
            ▼
┌─────────────────────────┐        Write Program Resume
│   Write address/data     │        Command Sequence
│   XXXh/3030h             │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│   Device reverts to      │
│   operation prior to     │
│   Program Suspend        │
└─────────────────────────┘
```

Figure 6.   Program Suspend/Program Resume

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Tables 11 and 12 show the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 10 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 12 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** The system must rewrite the command sequence and any additional addresses and commands. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation in is progress.*

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3:

Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 10 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.
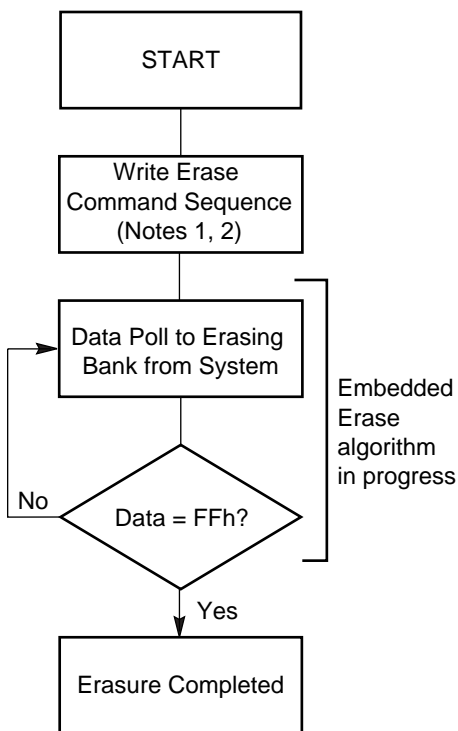
Notes:
1. *See Tables 11 and 12 for program command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Table 10.　Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5 µs (maximum of 20 µs) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Command Definitions

Table 11. Command Definitions (x16 Mode, BYTE# = V_{IH})

Command Sequence (Note 1)		Cycles	First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
	Device ID (Note 9)	4	555	AA	2AA	55	555	90	X01	227E	X0E	2212	X0F	2201
	SecSi™ Sector Factory Protect (Note 10)	4	555	AA	2AA	55	555	90	X03	(Note 10)				
	Sector Group Protect Verify (Note 12)	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
Enter SecSi Sector Region		3	555	AA	2AA	55	555	88						
Exit SecSi Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (Note 11)		3	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (Note 13)		3	555	AA	2AA	55	555	F0						
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 14)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 15)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (Note 16)		1	BA	B0										
Program/Erase Resume (Note 17)		1	BA	30										
CFI Query (Note 18)		1	55	98										

Legend:

X = Don't care

RA = Read Address of the memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A23–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes:

1. See Table 1 for description of bus operations.

2. All values are in hexadecimal.

3. Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.

4. Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD and WC.

5. Unless otherwise noted, address bits A23–A11 are don't cares.

6. No unlock or command cycles required when device is in read mode.

7. The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high while the device is providing status information.

8. The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See the Autoselect Command Sequence section for more information.

9. The device ID must be read in three cycles.

10. If WP# protects the highest address sector, the data is 98h for factory locked and 18h for not factory locked. If WP# protects the lowest address sector, the data is 88h for factory locked and 08h for not factor locked.

11. The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 21.

12. The data is 00h for an unprotected sector and 01h for a protected sector.

13. Command sequence resets device for next command after aborted write-to-buffer operation.

14. The Unlock Bypass command is required prior to the Unlock Bypass Program command.

15. The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.

16. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.

17. The Erase Resume command is valid only during the Erase Suspend mode.

18. Command is valid when device is ready to read array data or when device is in autoselect mode.

Table 12. Command Definitions (x8 Mode, BYTE# = V_IL)

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
	Device ID (Note 9)	4	AAA	AA	555	55	AAA	90	X02	7E	X1C	12	X1E	01
	SecSi™ Sector Factory Protect (Note 10)	4	AAA	AA	555	55	AAA	90	X06	(Note 10)				
	Sector Group Protect Verify (Note 12)	4	AAA	AA	555	55	AAA	90	(SA)X04	00/01				
Enter SecSi Sector Region		3	AAA	AA	555	55	AAA	88						
Exit SecSi Sector Region		4	AAA	AA	555	55	AAA	90	XXX	00				
Program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Write to Buffer (Note 11)		3	AAA	AA	555	55	SA	25	SA	BC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (Note 13)		3	AAA	AA	555	55	AAA	F0						
Unlock Bypass		3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program (Note 14)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 15)		2	XXX	90	XXX	00								
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Program/Erase Suspend (Note 16)		1	BA	B0										
Program/Erase Resume (Note 17)		1	BA	30										
CFI Query (Note 18)		1	AA	98										

Legend:

X = Don't care

RA = Read Address of the memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A23–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

BC = Byte Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 1 for description of bus operations.*

2. *All values are in hexadecimal.*

3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*

4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*

5. *Unless otherwise noted, address bits A22–A11 are don't cares.*

6. *No unlock or command cycles required when device is in read mode.*

7. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high while the device is providing status information.*

8. *The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See the Autoselect Command Sequence section for more information.*

9. *The device ID must be read in three cycles.*

10. *If WP# protects the highest address sector, the data is 98h for factory locked and 18h for not factory locked. If WP# protects the*

lowest address sector, the data is 88h for factory locked and 08h for not factor locked.

11. *The total number of cycles in the command sequence is determined by the number of bytes written to the write buffer. The maximum number of cycles in the command sequence is 37.*

12. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*

13. *Command sequence resets device for next command after aborted write-to-buffer operation.*

14. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*

15. *The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.*

16. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*

17. *The Erase Resume command is valid only during the Erase Suspend mode.*

18. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 13 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has

valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 13 shows the outputs for Data# Polling on DQ7. Figure 7 shows the Data# Polling algorithm. Figure 19 in the AC Characteristics section shows the Data# Polling timing diagram.
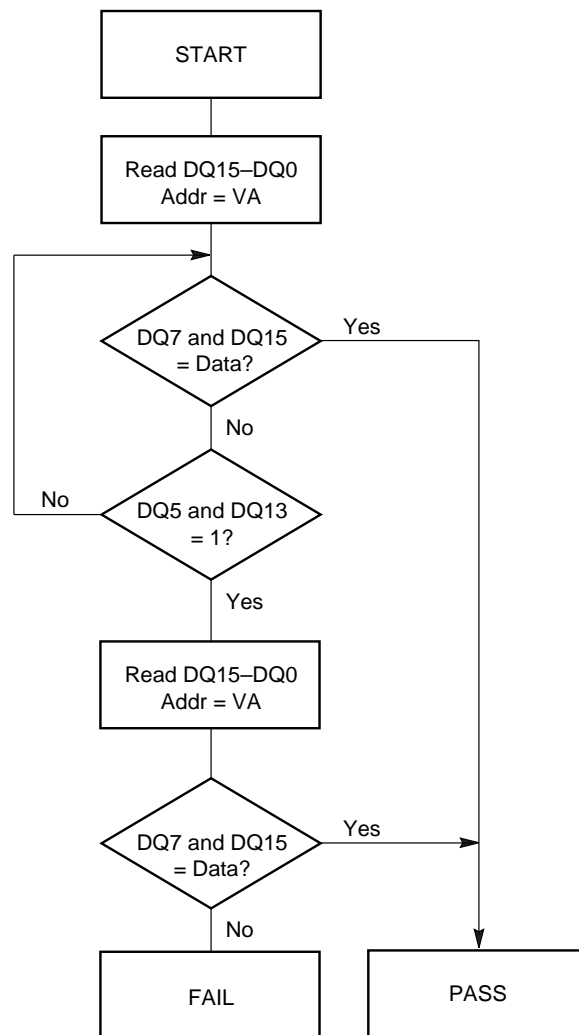
Notes:

1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.

2. DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Figure 7.   Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 13 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 13 shows the outputs for Toggle Bit I on DQ6. Figure 8 shows the toggle bit algorithm. Figure 20 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 21 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.
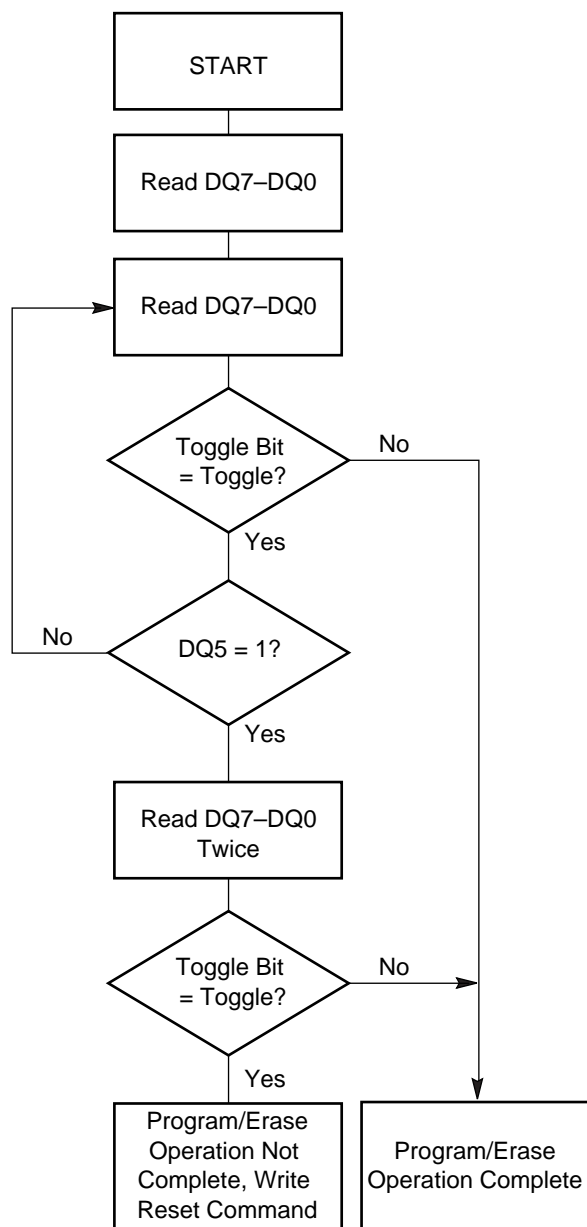
Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 8.   Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 13 to compare outputs for DQ2 and DQ6.

Figure 8 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the RY/BY#: Ready/Busy# subsection. Figure 20 shows the toggle bit timing diagram. Figure 21 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 8 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform

other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 8).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase com-

mand. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 μs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 13 shows the status of DQ3 relative to the other status bits.

DQ1: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer

Table 13.   Write Operation Status

	Status		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)						1
		Non-Program Suspended Sector	Data						1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						1
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer	Busy (Note 3)		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort (Note 4)		DQ7#	Toggle	0	N/A	N/A	1	0

Notes:

1. DQ5 switches to '1' when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.

2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

3. The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.

4. DQ1 switches to '1' when the device has aborted the write-to-buffer operation.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . .–0.5 V to +4.0 V

V_{IO}. . . . .–0.5 V to +4.0 V

A9, OE#, ACC, and RESET#
(Note 2). . . . .–0.5 V to +12.5 V

All other pins (Note 1) . . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 9. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 10.*

2. *Minimum DC input voltage on pins A9, OE#, ACC, and RESET# is –0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC input voltage on pin A9, OE#, ACC, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns.*

3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.
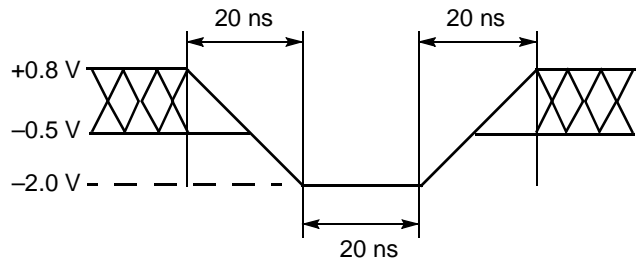

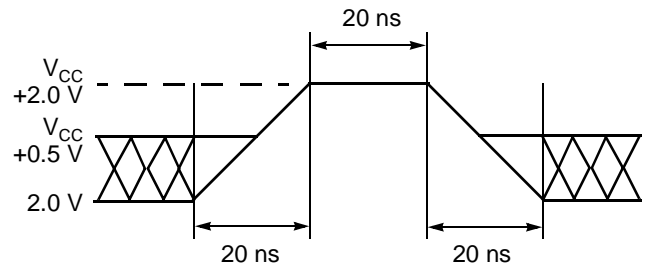**Figure 9.　Maximum Negative Overshoot Waveform**

Figure 10.　Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . –40°C to +85°C

Supply Voltages

V_{CC} (regulated voltage range) . . . . 3.0–3.6 V

V_{CC} (full voltage range) . . . . 2.7–3.6 V

V_{IO} (Note 2) . . . . 1.65–3.6 V

Notes:

1. *Operating ranges define those limits between which the functionality of the device is guaranteed.*

2. *See Ordering Information section for valid V_{CC}/V_{IO} range combinations. The I/Os will not operate at 3 V when V_{IO}=1.8 V.*

DC CHARACTERISTICS

CMOS Compatible

Parameter Symbol	Parameter Description (Notes)	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, ACC Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\ max}$; RESET# = 12.5 V				35	µA
I_{CC1}	V_{CC} Active Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH},	1 MHz		3	34	mA
			5 MHz		13	43	
I_{CC2}	V_{CC} Initial Page Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}	1 MHz		4	50	mA
			10 MHz		40	80	
I_{CC3}	V_{CC} Intra-Page Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}	10 MHz		3	20	mA
			33 MHz		6	40	
I_{CC4}	V_{CC} Active Write Current (3, 4)	CE# = V_{IL}, OE# = V_{IH}			50	60	mA
I_{CC5}	V_{CC} Standby Current (3)	CE#, RESET# = V_{CC} ± 0.3 V, WP# = V_{IH}			1	5	µA
I_{CC6}	V_{CC} Reset Current (3)	RESET# = V_{SS} ± 0.3 V, WP# = V_{IH}			1	5	µA
I_{CC7}	Automatic Sleep Mode (3, 5)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V, WP# = V_{IH}			1	5	µA
V_{IL1}	Input Low Voltage 1(6, 7)			−0.5		0.8	V
V_{IH1}	Input High Voltage 1 (6, 7)			1.9		V_{CC} + 0.5	V
V_{IL2}	Input Low Voltage 2 (6, 8)			−0.5		0.3 x V_{IO}	V
V_{IH2}	Input High Voltage 2 (6, 8)			1.9		V_{IO} + 0.5	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 2.7 –3.6 V		11.5		12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 2.7 –3.6 V		11.5		12.5	V
V_{OL}	Output Low Voltage (10)	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min} = V_{IO}$				0.15 x V_{IO}	V
V_{OH1}	Output High Voltage	I_{OH} = −2.0 mA, $V_{CC} = V_{CC\ min} = V_{IO}$		0.85 V_{IO}			V
V_{OH2}		I_{OH} = −100 µA, $V_{CC} = V_{CC\ min} = V_{IO}$		V_{IO}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (9)			2.3		2.5	V

Notes:

1. On the WP#/ACC pin only, the maximum input load current when WP# = V_{IL} is ± 5.0 µA.

2. The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.

3. Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.

4. I_{CC} active while Embedded Erase or Embedded Program is in progress.

5. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.

6. If $V_{IO} < V_{CC}$, maximum V_{IL} for CE# and DQ I/Os is 0.3 V_{IO}. Maximum V_{IH} for these connections is V_{IO} + 0.3 V

7. V_{CC} voltage requirements.

8. V_{IO} voltage requirements.

9. Not 100% tested

10. Includes RY/BY#

TEST CONDITIONS
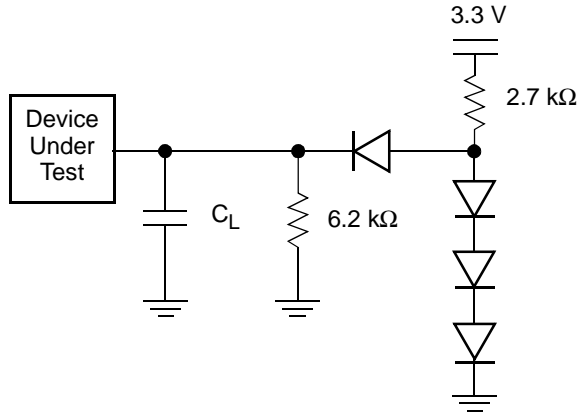
**Note:** *Diodes are IN3064 or equivalent.*

Figure 11.   Test Setup

Table 14.   Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels (See Note)	1.5	V
Output timing measurement reference levels	0.5 V_{IO}	V

Note: *If $V_{IO} < V_{CC}$, the reference level is 0.5 V_{IO}.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)
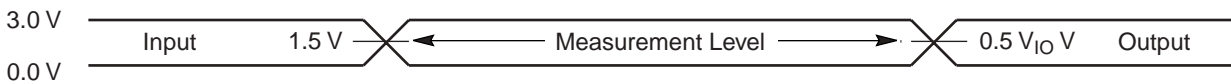
Note: *If $V_{IO} < V_{CC}$, the input measurement reference level is 0.5 V_{IO}.*

Figure 12.   Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read-Only Operations

Parameter						Speed Options					
JEDEC	Std.	Description	Test Setup			103, 103R	113R	113	123R	123	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)		Min	100	110		120			ns
t_{AVQV}	t_{ACC}	Address to Output Delay	CE#, OE# = V_{IL}	Max	100	110		120			ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	Max	100	110		120			ns
	t_{PACC}	Page Access Time		Max	30	30	40	30	40	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	30	30	40	30	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)		Max	16					ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)		Max	16					ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First		Min	0					ns
	t_{OEH}	Output Enable Hold Time (Note 1) — Read		Min	0					ns
		Output Enable Hold Time (Note 1) — Toggle and Data# Polling		Min	10					ns

Notes:

1. Not 100% tested.

2. See Figure 11 and Table 14 for test specifications.

3. AC specifications listed are tested with $V_{IO} = V_{CC}$. Contact AMD for information on AC operation with $V_{IO} \neq V_{CC}$
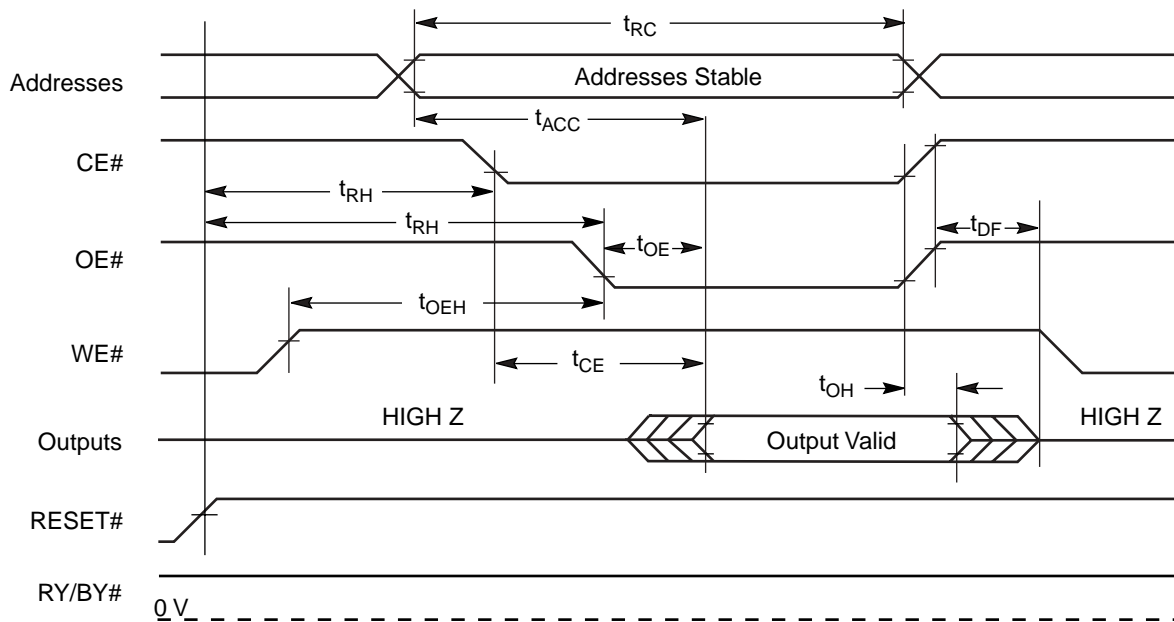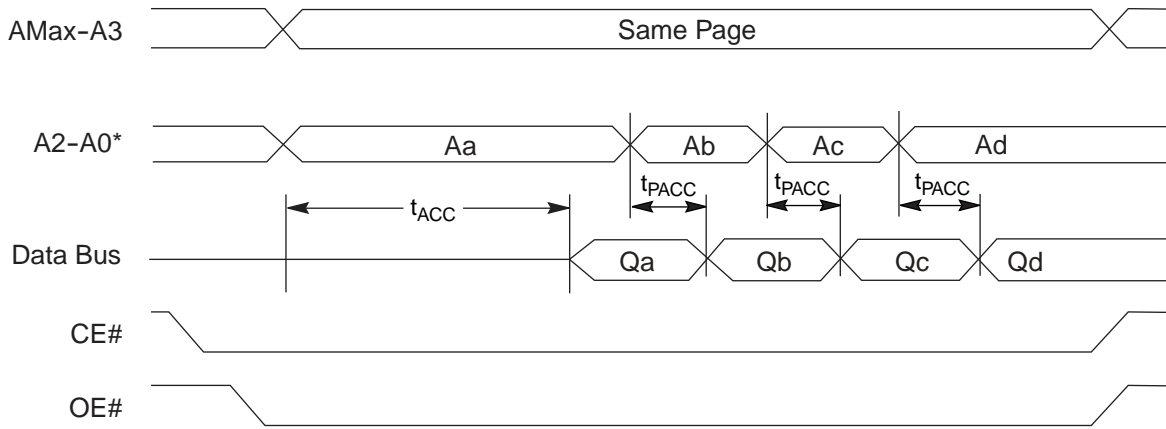

Figure 13.   Read Operation Timings

AC CHARACTERISTICS

* Figure shows word mode. Addresses are A1–A-1 for byte mode.

Figure 14.   Page Read Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note:

1. Not 100% tested.

2. AC specifications listed are tested with $V_{IO} = V_{CC}$. Contact AMD for information on AC operation with $V_{IO} \neq V_{CC}$.
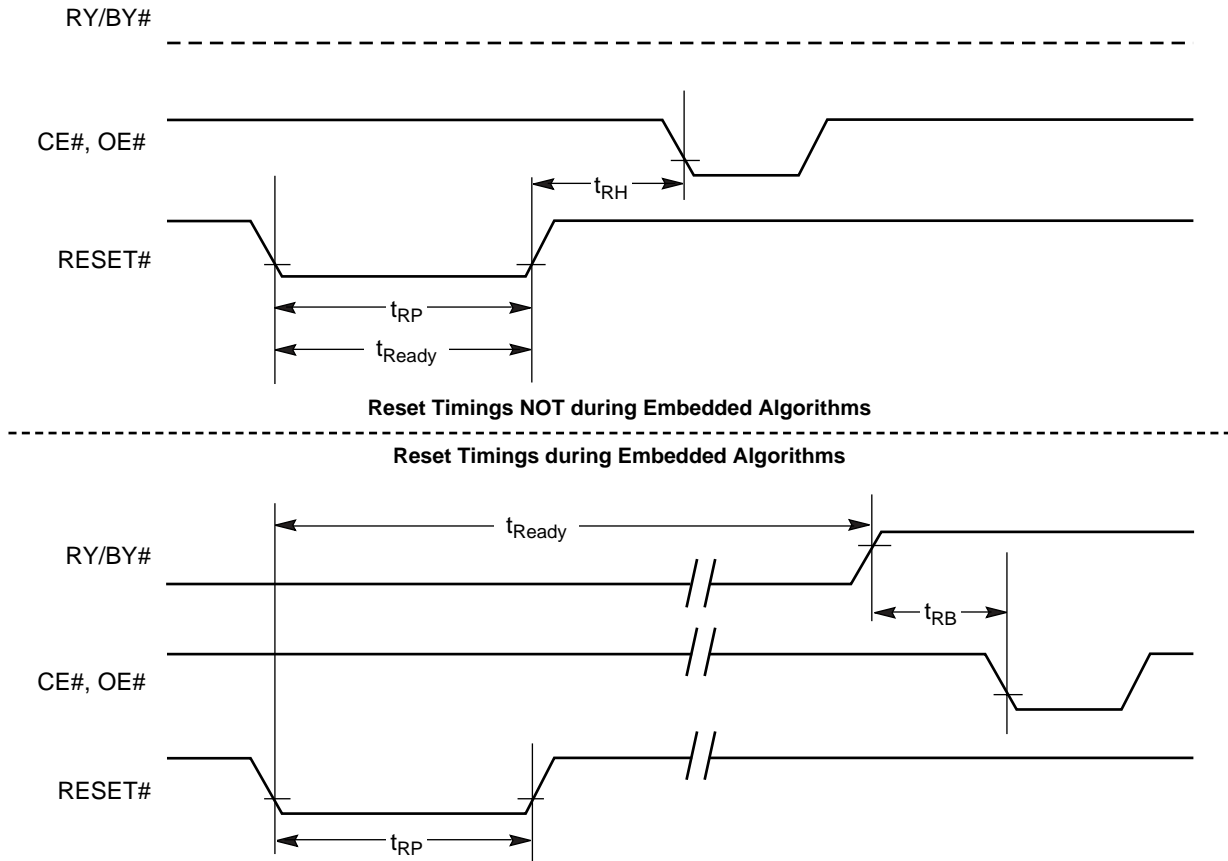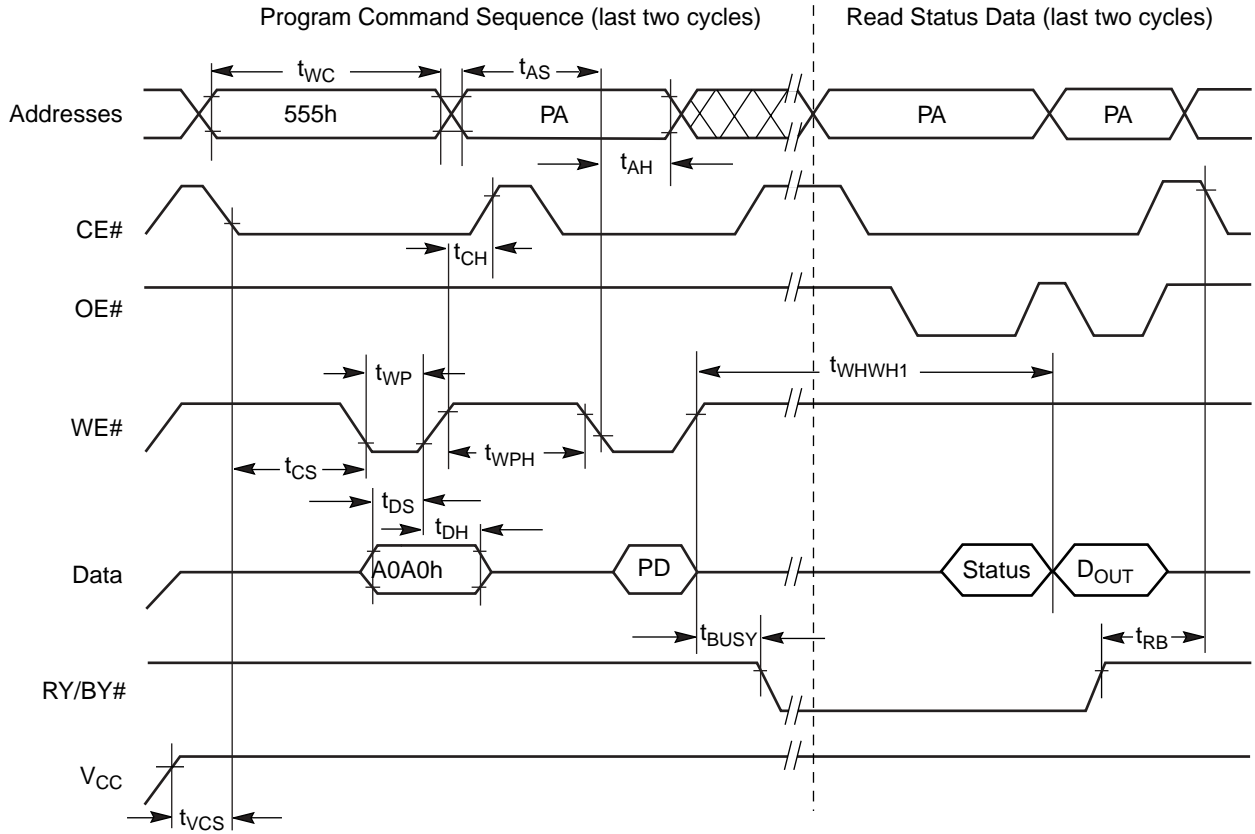

Reset Timings NOT during Embedded Algorithms

Reset Timings during Embedded Algorithms

Figure 15.   Reset Timings

AC CHARACTERISTICS

Erase and Program Operations

Parameter					Speed Options			
JEDEC	Std.	Description			103, 103R	113, 113R	123, 123R	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	100	110	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0			ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15			ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45			ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0			ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45			ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0			ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20			ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0			ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35			ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30			ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240			µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Byte	Typ	7.5			µs
			Per Word	Typ	15			µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Byte	Typ	6.25			µs
			Per Word	Typ	12.5			µs
		Single Byte/Word Program Operation (Note 2, 5)	Byte	Typ	60			µs
			Word	Typ	60			µs
		Accelerated Single Byte/Word Programming Operation (Note 2, 5)	Byte	Typ	54			µs
			Word	Typ	54			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5			sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)		Min	250			ns
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50			µs

Notes:

1. *Not 100% tested.*

2. *See the "Erase And Programming Performance" section for more information.*

3. *For 1–16 words/1–32 bytes programmed.*

4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*

5. *Byte/Word programming specification is based upon a single word/byte programming operation not utilizing the write buffer.*

6. *AC specifications listed are tested with $V_{IO} = V_{CC}$. Contact AMD for information on AC operation with $V_{IO} \neq V_{CC}$.*

AMD ◢

AC CHARACTERISTICS

Program Command Sequence (last two cycles) | Read Status Data (last two cycles)

Notes:
1. PA = program address, PD = program data, D_{OUT} is the true data at the program address.
2. Illustration shows device in word mode.
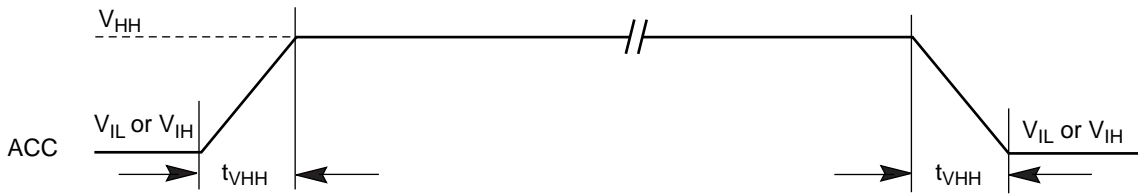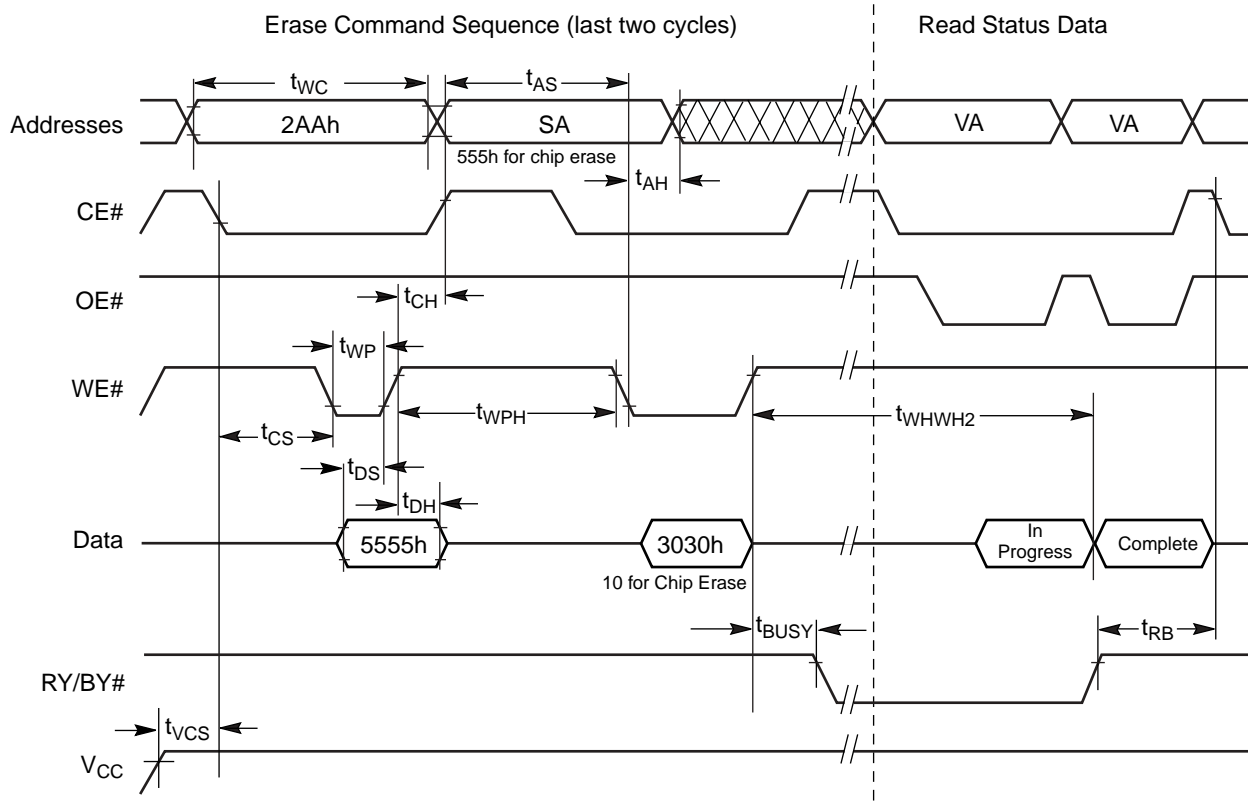
Figure 16. Program Operation Timings

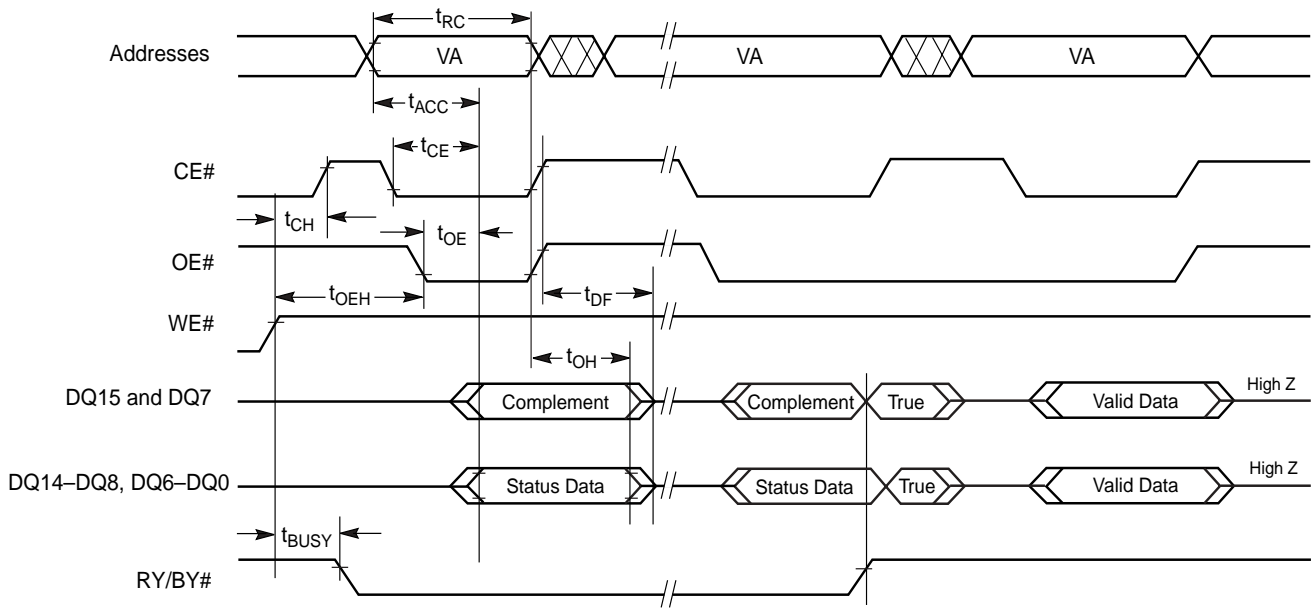**Figure 17. Accelerated Program Timing Diagram**

AC CHARACTERISTICS

Notes:

1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status".

2. These waveforms are for the word mode.

Figure 18.   Chip/Sector Erase Operation Timings

AC CHARACTERISTICS

Note: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 19.   Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS
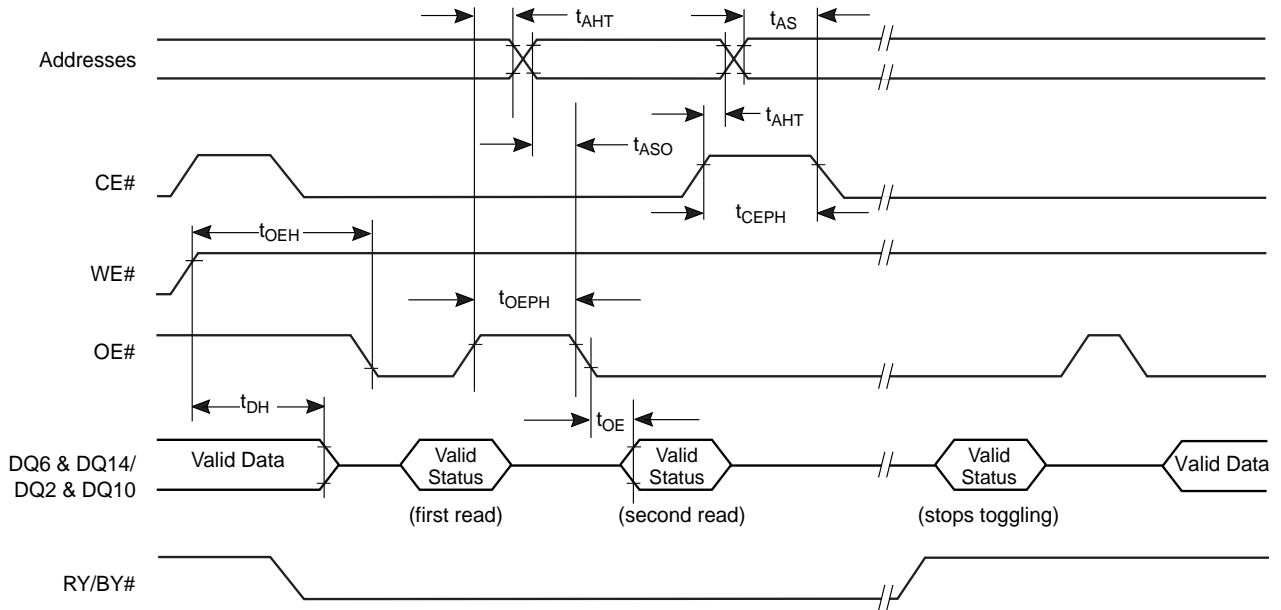
Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

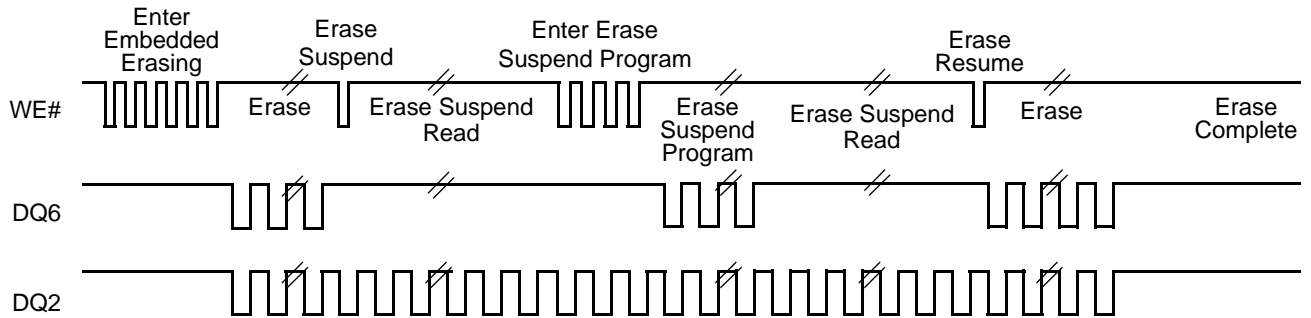**Figure 20.   Toggle Bit Timings (During Embedded Algorithms)**

Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 21.   DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

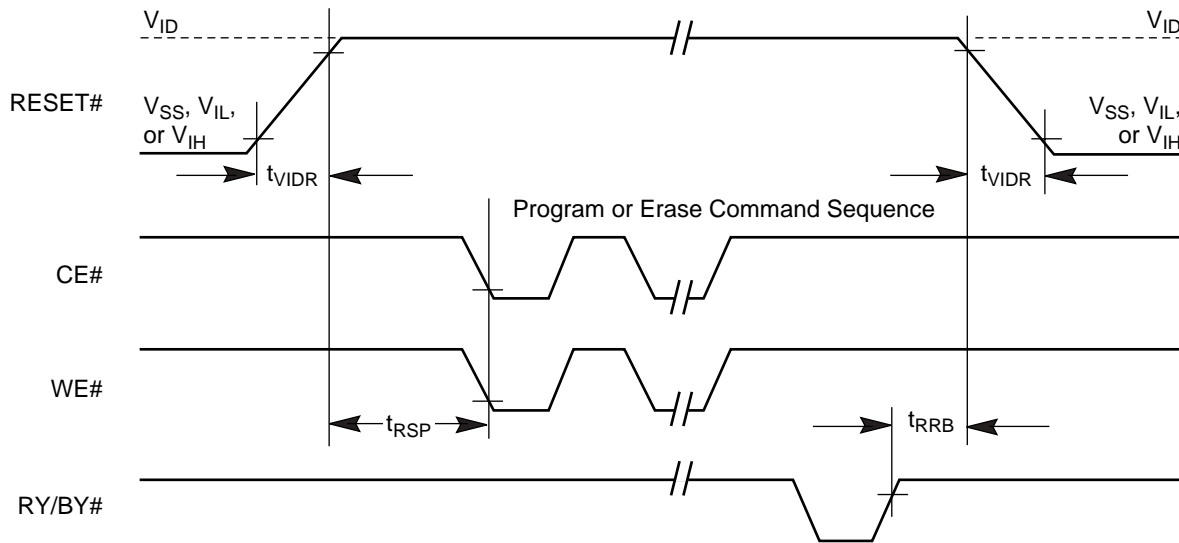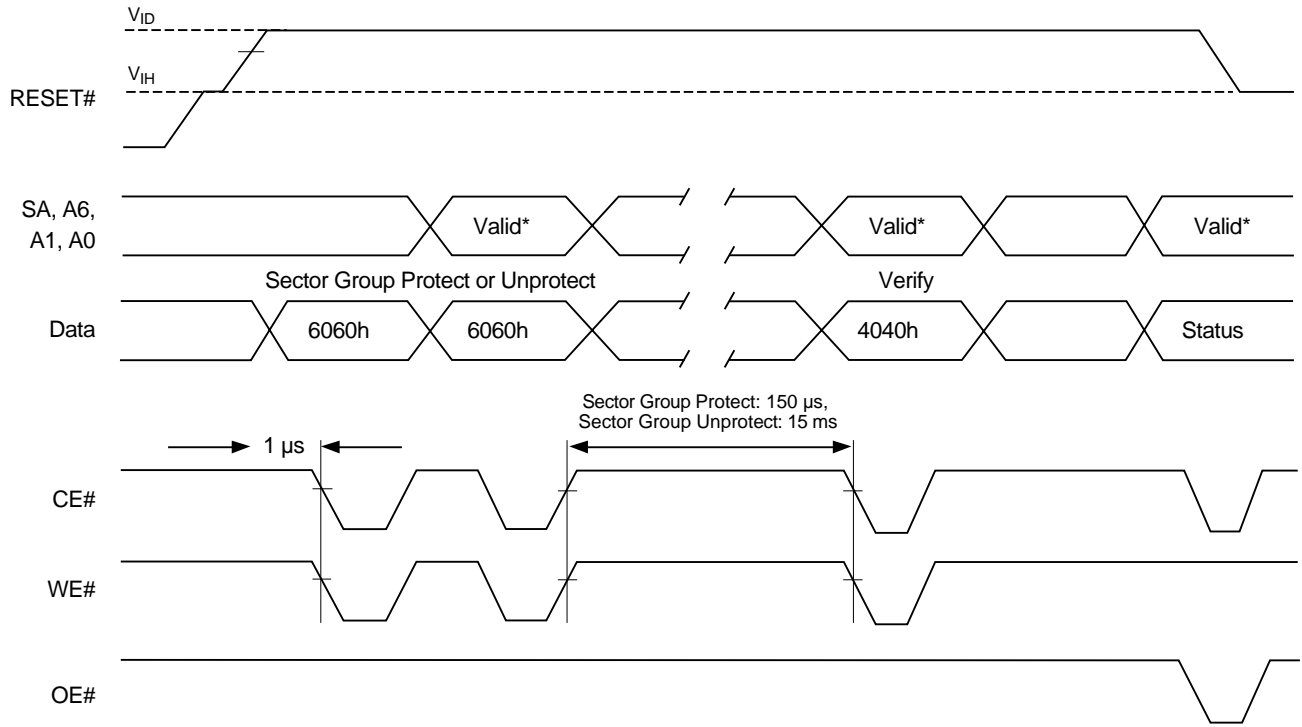| Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note: Not 100% tested.

Figure 22.   Temporary Sector Group Unprotect Timing Diagram

AC CHARACTERISTICS

* For sector group protect, A6 = 0, A1 = 1, A0 = 0. For sector group unprotect, A6 = 1, A1 = 1, A0 = 0.

**Figure 23.   Sector Group Protect and Unprotect Timing Diagram**

AC CHARACTERISTICS

Alternate CE# Controlled Erase and Program Operations

Parameter		Description			Speed Options			Unit
JEDEC	Std.				103, 103R	113, 113R	123, 123R	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	100	110	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min		0		ns
t_{ELAX}	t_{AH}	Address Hold Time		Min		45		ns
t_{DVEH}	t_{DS}	Data Setup Time		Min		45		ns
t_{EHDX}	t_{DH}	Data Hold Time		Min		0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min		0		ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min		0		ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min		0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min		45		ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min		30		ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ		240		µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Byte	Typ		7.5		µs
			Per Word	Typ		15		µs
		Effective Accelerated Write Buffer Program Operation (Notes 2, 4)	Per Byte	Typ		6.25		µs
			Per Word	Typ		12.5		µs
		Single Byte/Word Program Operation (Note 2, 5)	Byte	Typ		60		µs
			Word	Typ		60		µs
		Accelerated Single Byte/Word Programming Operation (Note 2, 5)	Byte	Typ		54		µs
			Word	Typ		54		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ		0.5		sec

Notes:

1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.
3. For 1–16 words/1–32 bytes programmed.
4. Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.
5. Byte/Word programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
6. AC specifications listed are tested with $V_{IO} = V_{CC}$. Contact AMD for information on AC operation with $V_{IO} \neq V_{CC}$

AC CHARACTERISTICS
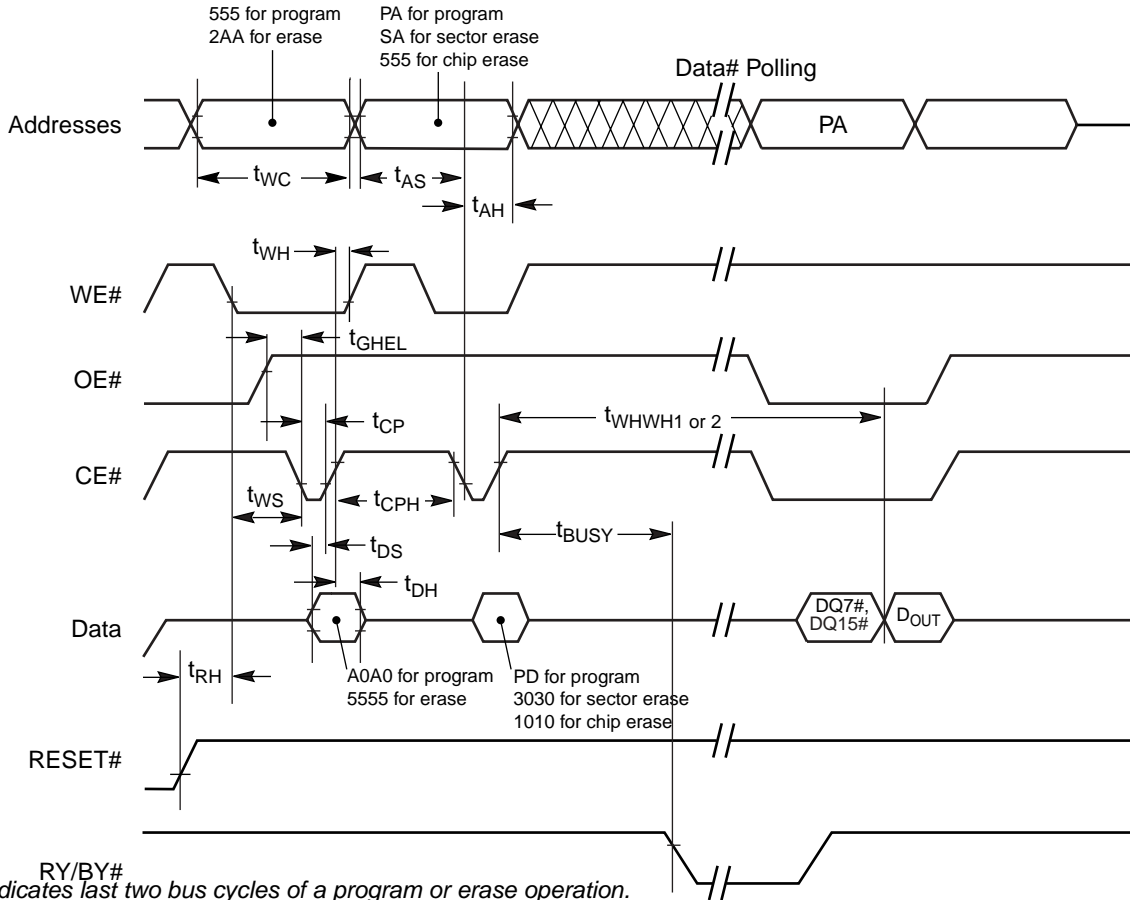
Notes:

1. Figure indicates last two bus cycles of a program or erase operation.

2. PA = program address, SA = sector address, PD = program data.

3. DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.

4. Waveforms are for the word mode.

**Figure 24.   Alternate CE# Controlled Write (Erase/Program)
Operation Timings**

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	−1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	−1.0 V	V_{CC} + 1.0 V
V_{CC} Current	−100 mA	+100 mA

Note: Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	3.5	sec	Excludes 00h programming prior to erasure (Note 6)
Chip Erase Time		256	512	sec	
Single Byte/Word Program Time (Note 3)	Byte	60	600	µs	Excludes system level overhead (Note 7)
	Word	60	600	µs	
Accelerated Single Byte/Word Program Time (Note 3)	Byte	54	540	µs	
	Word	54	540	µs	
Total Write Buffer Program Time (Note 4)		240	1200	µs	
Effective Write Buffer Program Time (Note 5)	Per Byte	7.5	38	µs	
	Per Word	15	75	µs	
Total Accelerated Write Buffer Program Time (Note 4)		200	1040	µs	
Effective Accelerated Write Buffer Program Time (Note 5)	Per Byte	6.25	33	µs	
	Per Word	12.5	65	µs	
Chip Program Time		252	584	sec	

Notes:
1. Typical program and erase times assume the following conditions: $25°C$, 3.0 V V_{CC}. Programming specifications assume that all bits are programmed to 00h.
2. Maximum values are measured at VCC = 3.0, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Byte/Word programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
4. For 1-16 words or 1-32 bytes programmed in a single write buffer programming operation.
5. Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.
6. In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.
7. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 11 for further information on command definitions.
8. The device has a minimum erase and program cycle endurance of 100,000 cycles.

TSOP PIN AND BGA PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	TSOP	6	7.5	pF
			BGA	4.2	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	TSOP	8.5	12	pF
			BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	TSOP	7.5	9	pF
			BGA	3.9	4.7	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, f = 1.0 MHz.

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

TS056/TSR056—56-Pin Standard/Reverse Thin Small Outline Package (TSOP)
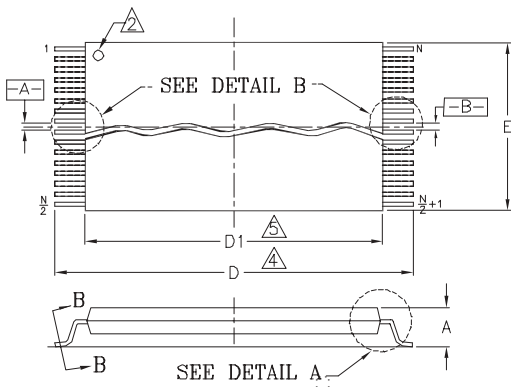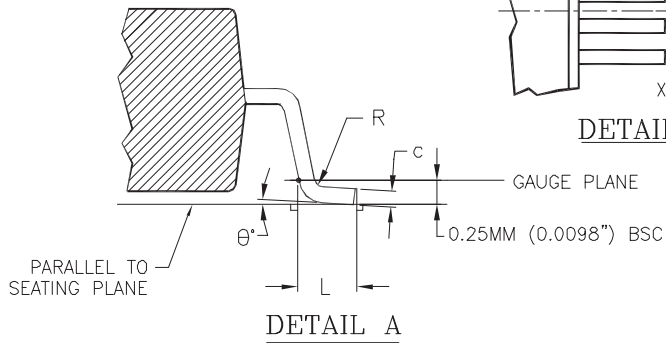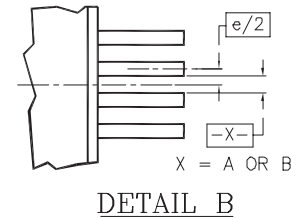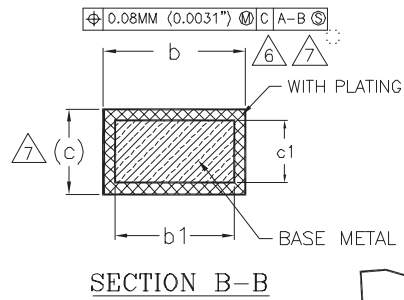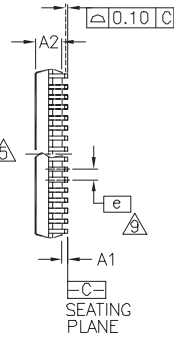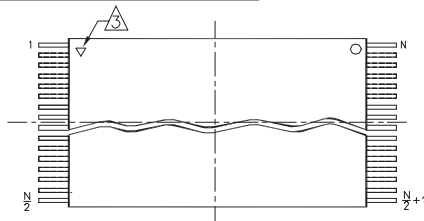
PACKAGE	TS/TSR 56		
JEDEC	MO-142 (B) EC		
SYMBOL	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	---	0.16
c	0.10	---	0.21
D	19.90	20.00	20.20
D1	18.30	18.40	18.50
E	13.90	14.00	14.10
e	0.50 BASIC		
L	0.50	0.60	0.70
Ø	0°	3°	5°
R	0.08	---	0.20
N	56		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982.)

2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).

3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.

4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.

5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15 mm PER SIDE.

6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 mm TOTAL IN EXCESS OF b DIMENSION AT MAX MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 mm.

7. THESE DIMESIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.

8. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

3160\38.10A

PHYSICAL DIMENSIONS

LAC064—64-Ball Fortified Ball Grid Array
18 x 12 mm Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW

PACKAGE	LAC 064			
JEDEC	N/A			
	18.00 mm x 12.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE HEIGHT
A1	0.40	---	---	STANDOFF
A2	0.60	---	---	BODY THICKNESS
D	18.00 BSC.			BODY SIZE
E	12.00 BSC.			BODY SIZE
D1	7.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	64			BALL COUNT
φb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC.			BALL PITCH - D DIRECTION
eE	1.00 BSC.			BALL PITCH - E DIRECTION
SD / SE	0.50 BSC.			SOLDER BALL PLACEMENT
	NONE			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).

4. e REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $e/2$

8. NOT USED.

9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

3243 \ 16-038.12d

REVISION SUMMARY

Revision A (August 3, 2001)

Initial release as abbreviated Advance Information data sheet.

Revision A+1 (September 12, 2001)

Ordering Information

Changed package part number designation from WH to PC.

Physical Dimensions

Added the TS056 and LAA064 packages.

Revision A+2 (October 3, 2001)

Global

Corrected title from 64 Mbit to 256 Mbit. Added 120 ns speed option.

Distinctive Characteristics

SecSi™ (Secured Silicon) Sector region: Corrected 64-byte to 256-byte.

Connection Diagram

Modified Fortified BGA ball grid to an 8 x 8 ball matrix. Changed RFU (reserved for future use) balls to NC (No Connection).

Ordering Information

Changed operating voltage range on 90 ns speed option to 3.0–3.6 V.

Pin Description

Added A-1 description.

Revision A+3 (March 25, 2002)

Distinctive Characteristics

Clarified description of Enhanced VersatileIO control.

Physical Dimensions

Added drawing that shows both TS056 and TSR056 specifications.

Revision B (July 1, 2002)

Expanded data sheet to full specification version.

Revision B+1 (July 10, 2002)

Ordering Information, Physical Dimensions

Corrected package description to LAC064, 18 x 12 mm Fortified BGA.

DC Characteristics table

Deleted I_{ACC} specification.

Revision B+2 (September 9, 2002)

Product Selector Guide, Ordering Information, Read-Only Operations, Erase and Program Operations, and Alternate CE# Controlled Erase and Program Operations

Added regulated OPNs.

Changed all OPNs that end with 4 or 9 to end with 3 or 8.

Changed all package markings that contain combinations that end with 4 or 9 to end with 3 or 8.

CFI

Modified wording of last paragraph to read: "reading array data."

Program Suspend/Program Resume Command Sequence

Changed 15 µs typical to maximum and added 5 µs typical.

Erase Suspend/Erase Resume Commands

Changed typical from 20 µs to 5 µs and added a maximum of 20 µs.

LAC064—64-Ball Fortified Ball Grid Array

Added final package drawing.

Revision B+3 (October 23, 2002)

SecSi (Secured Silicon) Sector Flash Memory Region

Added x8 address range.

Physical Dimensions

Modified drawing to show the actual number of balls on device package.

Revision B+4 (November 6, 2002)

Global

Removed the Enhanced VI/O option and changed it to VI/O only.

Product Selector Guide

Removed the 98R, 108, 108R, 118, 118R, 128, and 128R Speed Options.

Modified Note #2.

Moved V_{IO} from far left side of the block diagram and moved it to Input/Output Buffers.

Ordering Information

Modified Order numbers and package markings to reflect the removal of speed options.

Table 4. SecSi Sector Contents

Added x8 and x16

Operating Ranges

Changed the V_{IO} supply range to 1.65–3.6 V.

Erase and Programming Performance

Changed the typicals and/or maximums of Chip Erase Time, Effective Write Buffer Program Time, and Program Time to TBD.

Customer Lockable: SecSi Sector NOT Programmed or Protected at the factory.

Added second bullet, SecSi sector-protect verify text and figure 3.

Table 7. Device Geometry Definition

Changed the x16 data for 2Dh to 00FFh.

SecSi Sector Flash Memory Region, and Enter SecSi Sector/Exit SecSi Sector Command Sequence

Noted that the ACC function and unlock bypass modes are not available when the SecSi sector is enabled.

Byte/Word Program Command Sequence, Sector Erase Command Sequence, and Chip Erase Command Sequence

Noted that the SecSi Sector, autoselect, and CFI functions are unavailable when a program or erase operation is in progress.

Common Flash Memory Interface (CFI)

Changed CFI website address.

Revision B+5 (November 11, 2002)

Product Selector Guide and Read Only Operations

Added a 30 ns Page Access time and Output Enable Access time to the 113R and 123R Speed Options.

Revision B+6 (December 2, 2002)

Global

Added Sector Group Protection and added Table 4.

Product Selector Guide

Added V_{IO}s to table and removed Note #2

Ordering Information

Corrected typos in V_{IO} ranges.

Removed Note.

Figure 6. Program Suspend/Program Resume

Change wait time to 15 µs.

Operating Ranges

Corrected typos in V_{IO} ranges.

Removed full voltage range.

CMOS Compatible

Changed V_{IH1} and V_{IH2} minimum to 1.9.

Removed typos in notes.

Read-Only Characteristics

Added note #3.

Hardware Reset, Erase and Program Operations, Temporary Sector Unprotect, and Alternate CE# Controlled Erase and Program Operations

Added Note.

Revision C (February 14, 2003)

Distinctive Characteristics

Corrected performance characteristics.

Product Selector Guide

Removed 93R speed option.

Added note 2.

Ordering Information

Corrected Valid Combination to reflect speed option changes.

Added Note.

AC Characteristics

Removed 93, 93R speed option.

Added Note

Input values in the $t_{WHWH}1$ and $t_{WHWH}2$ parameters in the Erase and Program Options table that were previously TBD. Also added notes 5 and 6.

Input values in the $t_{WHWH}1$ and $t_{WHWH}2$ parameters in the Alternate CE# Controlled Erase and Program Options table that were previously TBD. Also added notes 5.

Erase and Programming Performance

Input values into table that were previously TBD.

Added note 4.

Revision C+1 (May 28, 2003)

Global

Converted to full datasheet version.

Modified SecSi Sector Flash Memory Region section to include ESN references.

Erase and Programming Performance

Input values into table that were previously TBD.

Modified notes.

CMOS Compatible

Corrected typos in table.

Erase and Program Operations and Alternate CE# Controlled Erase and Program Operations

Changed the typical for the Accelerated Effective Write Buffer Program Operation for Byte and Word to 6.25 and 12.5.

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