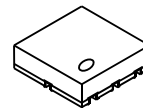# SP3T SWITCH GaAs MMIC

## ■ GENERAL DESCRIPTION

NJG1650HB6 is a SP3T switch IC featured low insertion loss, high isolation and small size package.

This switch is suitable for W-LAN, Bluetooth, and sub-microwave applications.

A small and thin package of USB8-B6 is adopted.

## ■ PACKAGE OUTLINE

NJG1650HB6

## ■ FEATURES

- Control voltage range      +2.0~+5.0V
- Low insertion loss      0.38dB typ. @f=1.0GHz, $P_{IN}$=23dBm, $V_{CTL(H)}$=2.7V
       0.42dB typ. @f=2.0GHz, $P_{IN}$=23dBm, $V_{CTL(H)}$=2.7V
       0.45dB typ. @f=2.5GHz. $P_{IN}$=23dBm, $V_{CTL(H)}$=2.7V
- High isolation      21dB typ. @f=2.5GHz, $P_{IN}$=23dBm, $V_{CTL(H)}$=2.7V
- Input power at 0.2dB compression point      28dBm typ. @f=2.5GHz, $V_{CTL(H)}$=2.7V
- Low current consumption      5μA typ.    @ $V_{CTL(H)}$=2.7V
- Small & thin package      USB8-B6 (package Size: 1.5 x 1.5 x 0.55mm typ.)

## ■ PIN CONFIGURATION

USB8-B6 Type
(Top view)
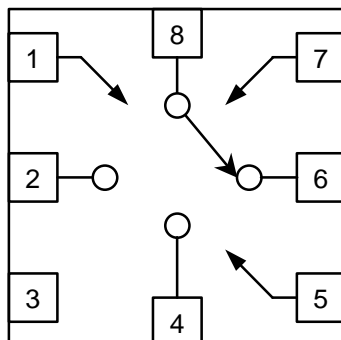


Pin connection

1. VCTL3
2. P3
3. GND
4. P2
5. VCTL2
6. P1
7. VCTL1
8. PC

## ■ TRUTH TABLE

"H"=$V_{CTL}$(H), "L"=$V_{CTL}$(L)

| VCTL1 | VCTL2 | VCTL3 | PATH |
|-------|-------|-------|-------|
| H | L | L | PC-P1 |
| L | H | L | PC-P2 |
| L | L | H | PC-P3 |

NOTE: The information on this datasheet is subject to change without notice.

*New Japan Radio Co., Ltd.*

# NJG1650HB6

## ■ ABSOLUTE MAXIMUM RATINGS

$(T_a=+25°C, Z_s=Z_l=50\Omega)$

| PARAMETERS | SYMBOL | CONDITIONS | RATINGS | UNITS |
|---|---|---|---|---|
| Input Power | $P_{IN}$ | $V_{CTL}(H)=2.7V$ | 30 | dBm |
| Control Voltage | $V_{CTL}$ | | 6.0 | V |
| Power Dissipation | $P_D$ | On PCB Board | 150 | mW |
| Operating Temp. | $T_{opr}$ | | -40~+85 | °C |
| Storage Temp. | $T_{stg}$ | | -55~+150 | °C |

## ■ ELECTRICAL CHARACTERISTICS

$(V_{CTL(L)}=0V,\ V_{CTL(H)}=2.7V,\ Z_S=Z_l=50\Omega,\ T_a=+25°C,\ \text{with application circuit})$

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Control voltage(LOW) | $V_{CTL}(L)$ | | -0.2 | - | +0.2 | V |
| Control voltage (HIGH) | $V_{CTL}(H)$ | | 2.0 | 2.7 | 5.0 | V |
| Control current | $I_{CTL}$ | | - | 5 | 10 | µA |
| Insertion Loss 1 | LOSS1 | f=1.0GHz, $P_{IN}$=23dBm | - | 0.38 | 0.55 | dB |
| Insertion Loss 2 | LOSS2 | f=2.0GHz, $P_{IN}$=23dBm | - | 0.42 | 0.60 | dB |
| Insertion Loss 3 | LOSS3 | f=2.5GHz, $P_{IN}$=23dBm | - | 0.45 | 0.60 | dB |
| Isolation 1 | ISL1 | f=1.0GHz, $P_{IN}$=23dBm | 27 | 29 | - | dB |
| Isolation 2 | ISL2 | f=2.0GHz, $P_{IN}$=23dBm | 21 | 23 | - | dB |
| Isolation 3 | ISL3 | f=2.5GHz, $P_{IN}$=23dBm | 19 | 21 | - | dB |
| Input power at 0.2dB compression point | $P_{-0.2dB}$ | f=2.5GHz | 25 | 28 | - | dBm |
| VSWR (PC, P1, P2, P3) | VSWR | f=2.5GHz, On state | - | 1.1 | 1.3 | |
| Switching time | $T_{SW}$ | 50% CTL to 10/90% RF | - | 150 | 500 | ns |

■ **TERMINAL INFORMATION**

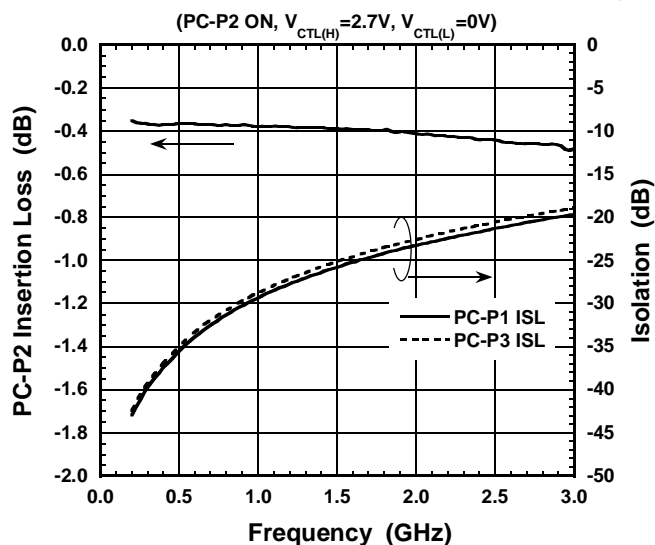| No. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | VCTL3 | Control port. This port is set to $V_{CTL(H)}$ (+2.0~+5.0V) or $V_{CTL(L)}$ (-0.2~+0.2V). For good RF performance, please place a bypass capacitor between this port and GND, close to this port. Please choose optimum capacitance value from 10pF to 1000pF because this capacitor influences a switching time. |
| 2 | P3 | RF port. This port is connected to PC port by control voltage of $V_{CTL(H)}$ at 1st pin, $V_{CTL(L)}$ at 5th and 7th pins. In order to block DC bias voltage of internal circuit, an external capacitor is required. |
| 3 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance. |
| 4 | P2 | RF port. This port is connected to PC port by control voltage of $V_{CTL(H)}$ at 5th pin, $V_{CTL(L)}$ at 1st and 7th pins. In order to block DC bias voltage of internal circuit, an external capacitor is required. |
| 5 | VCTL2 | Control port. This port is set to $V_{CTL(H)}$ (+2.0~+5.0V) or $V_{CTL(L)}$ (-0.2~+0.2V). For good RF performance, please place a bypass capacitor between this port and GND, close to this port. Please choose optimum capacitance value from 10pF to 1000pF because this capacitor influences a switching time. |
| 6 | P1 | RF port. This port is connected to PC port by control voltage of $V_{CTL(H)}$ at 7th pin, $V_{CTL(L)}$ at 1st and 5th pins. In order to block DC bias voltage of internal circuit, an external capacitor is required. |
| 7 | VCTL1 | Control port. This port is set to $V_{CTL(H)}$ (+2.0~+5.0V) or $V_{CTL(L)}$ (-0.2~+0.2V). For good RF performance, please place a bypass capacitor between this port and GND, close to this port. Please choose optimum capacitance value from 10pF to 1000pF because this capacitor influences a switching time. |
| 8 | PC | Common RF port. This PC port is connected with either of P1, P2 and P3 by logical control voltage of VCTL1 to 3. In order to block DC bias voltage of internal circuit, an external capacitor is required. |

# NJG1650HB6

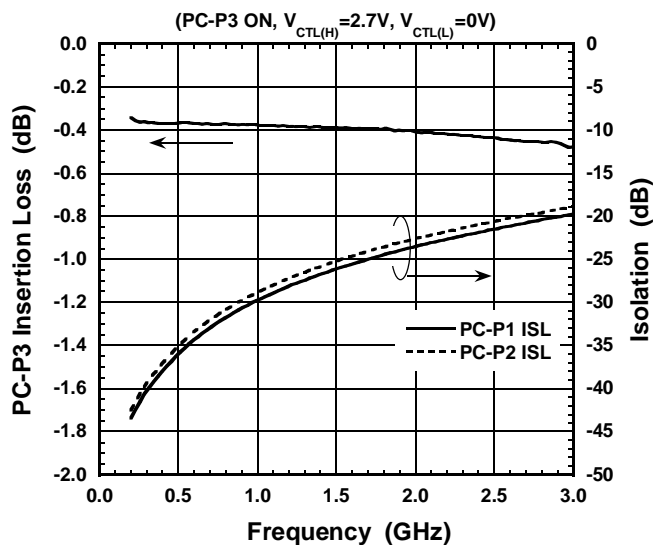■ **ELECTRICAL CHARACTERISTICS**   (With Application circuit, Loss of external circuit are excluded)
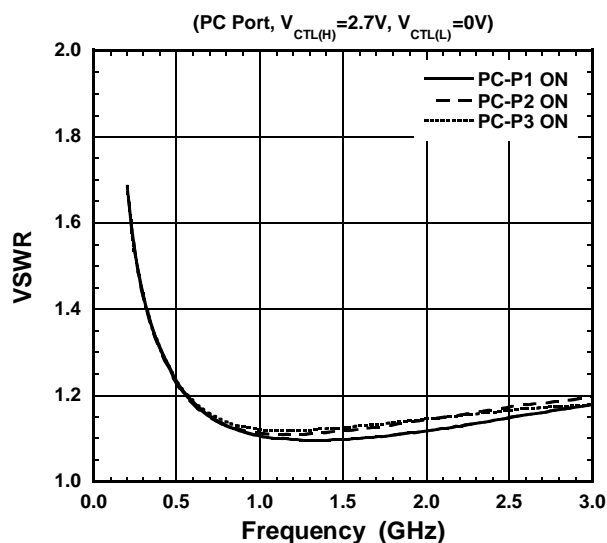
## Insertion Loss, Isolation vs Frequency
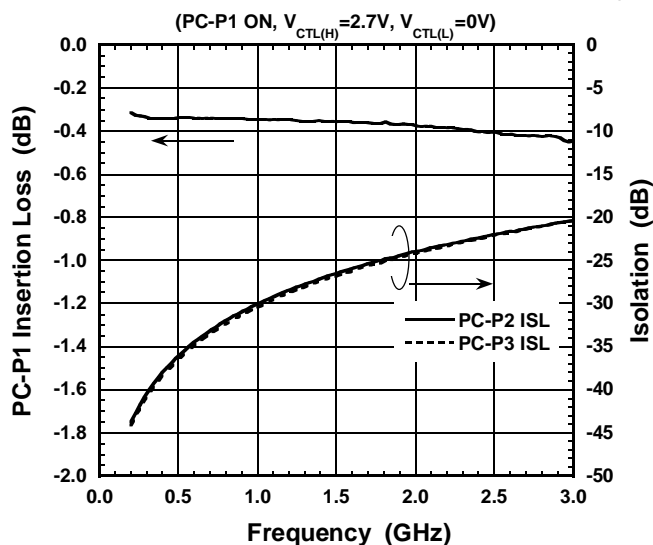
(PC-P1 ON, V$_{CTL(H)}$=2.7V, V$_{CTL(L)}$=0V)

## Insertion Loss, Isolation vs Frequency

(PC-P2 ON, V$_{CTL(H)}$=2.7V, V$_{CTL(L)}$=0V)

## Insertion Loss, Isolation vs Frequency

(PC-P3 ON, V$_{CTL(H)}$=2.7V, V$_{CTL(L)}$=0V)

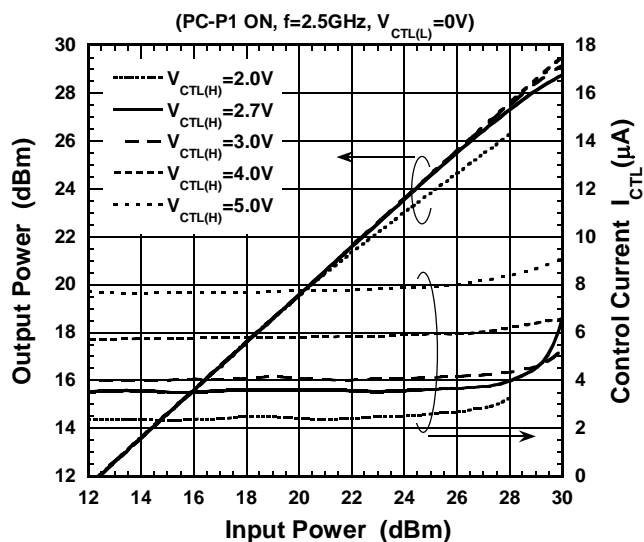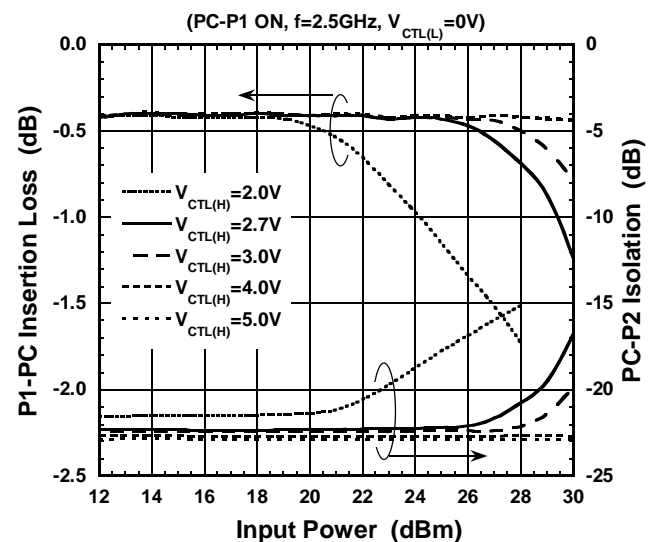## VSWR vs Frequency

(PC Port, V$_{CTL(H)}$=2.7V, V$_{CTL(L)}$=0V)

■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

## Output Power, $I_{CTL}$ vs Input Power

(PC-P1 ON, f=2.5GHz, $V_{CTL(L)}$=0V)

Legend:
- $V_{CTL(H)}$=2.0V
- $V_{CTL(H)}$=2.7V
- $V_{CTL(H)}$=3.0V
- $V_{CTL(H)}$=4.0V
- $V_{CTL(H)}$=5.0V

Y-axis (left): Output Power (dBm)
Y-axis (right): Control Current $I_{CTL}$ (μA)
X-axis: Input Power (dBm)

## Insertion Loss, Isolation vs Input Power
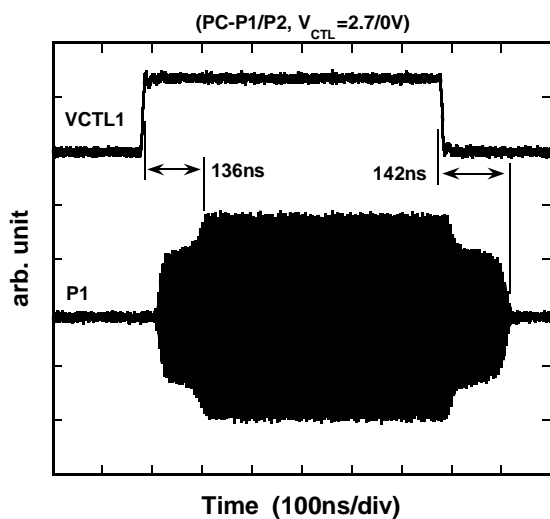
(PC-P1 ON, f=2.5GHz, $V_{CTL(L)}$=0V)

Legend:
- $V_{CTL(H)}$=2.0V
- $V_{CTL(H)}$=2.7V
- $V_{CTL(H)}$=3.0V
- $V_{CTL(H)}$=4.0V
- $V_{CTL(H)}$=5.0V

Y-axis (left): P1-PC Insertion Loss (dB)
Y-axis (right): PC-P2 Isolation (dB)
X-axis: Input Power (dBm)

## Switching Time

(PC-P1/P2, $V_{CTL}$=2.7/0V)

VCTL1

136ns    142ns

P1

Y-axis: arb. unit
X-axis: Time (100ns/div)

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■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

## Insertion Loss vs Ambient Temperature

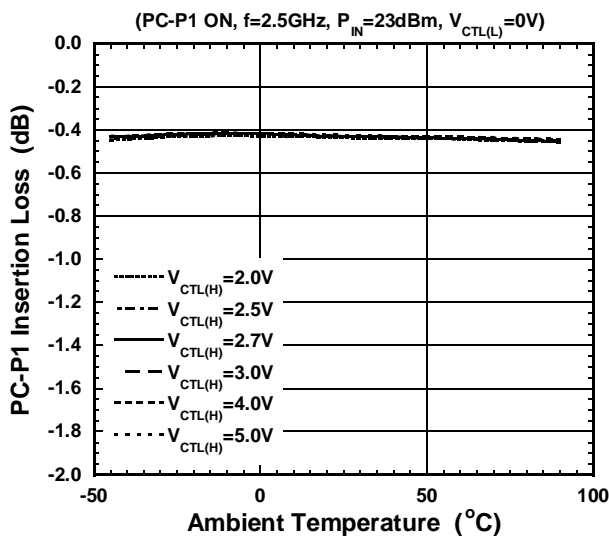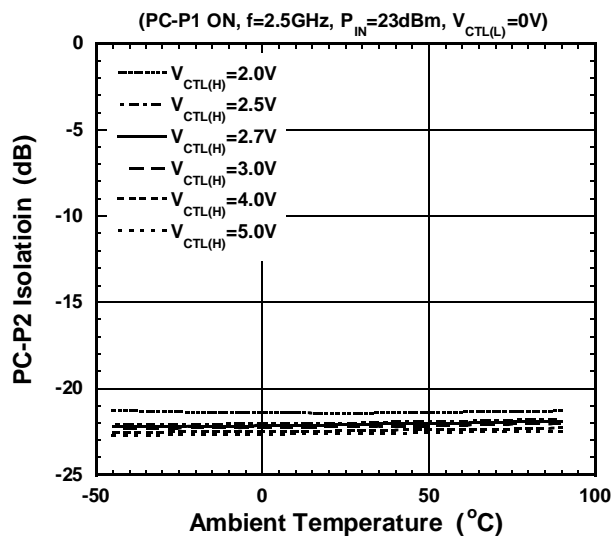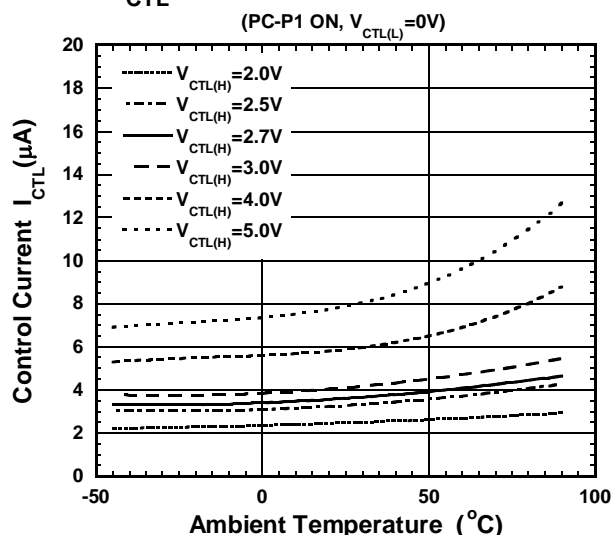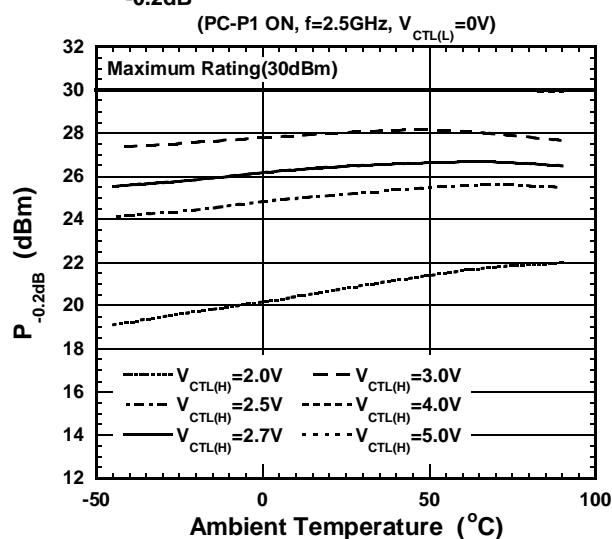(PC-P1 ON, f=2.5GHz, $P_{IN}$=23dBm, $V_{CTL(L)}$=0V)

Y-axis: PC-P1 Insertion Loss (dB)
X-axis: Ambient Temperature ($^{o}$C)

$V_{CTL(H)}$=2.0V
$V_{CTL(H)}$=2.5V
$V_{CTL(H)}$=2.7V
$V_{CTL(H)}$=3.0V
$V_{CTL(H)}$=4.0V
$V_{CTL(H)}$=5.0V

## Isolation vs Ambient Temperature

(PC-P1 ON, f=2.5GHz, $P_{IN}$=23dBm, $V_{CTL(L)}$=0V)

Y-axis: PC-P2 Isolatioin (dB)
X-axis: Ambient Temperature ($^{o}$C)

$V_{CTL(H)}$=2.0V
$V_{CTL(H)}$=2.5V
$V_{CTL(H)}$=2.7V
$V_{CTL(H)}$=3.0V
$V_{CTL(H)}$=4.0V
$V_{CTL(H)}$=5.0V

## VSWR vs Ambient Temperature

(PC-P1 ON, f=2.5GHz, $V_{CTL(L)}$=0V)

Y-axis: VSWR(PC Port)
X-axis: Ambient Temperature ($^{o}$C)

$V_{CTL(H)}$=2.0V
$V_{CTL(H)}$=2.5V
$V_{CTL(H)}$=2.7V
$V_{CTL(H)}$=3.0V
$V_{CTL(H)}$=4.0V
$V_{CTL(H)}$=5.0V

## $I_{CTL}$ vs Ambient Temperature

(PC-P1 ON, $V_{CTL(L)}$=0V)

Y-axis: Control Current $I_{CTL}$ (µA)
X-axis: Ambient Temperature ($^{o}$C)

$V_{CTL(H)}$=2.0V
$V_{CTL(H)}$=2.5V
$V_{CTL(H)}$=2.7V
$V_{CTL(H)}$=3.0V
$V_{CTL(H)}$=4.0V
$V_{CTL(H)}$=5.0V

## $P_{-0.2dB}$ vs Ambient Temperature

(PC-P1 ON, f=2.5GHz, $V_{CTL(L)}$=0V)

Y-axis: $P_{-0.2dB}$ (dBm)
X-axis: Ambient Temperature ($^{o}$C)

Maximum Rating(30dBm)

$V_{CTL(H)}$=2.0V    $V_{CTL(H)}$=3.0V
$V_{CTL(H)}$=2.5V    $V_{CTL(H)}$=4.0V
$V_{CTL(H)}$=2.7V    $V_{CTL(H)}$=5.0V

## Switching Time vs Ambient Temperature

(P1Port(PC-P1/PC-P2), $V_{CTL(L)}$=0V)

Y-axis: Switching Time (ns)
X-axis: Ambient Temperature ($^{o}$C)

$V_{CTL(H)}$=2.0V
$V_{CTL(H)}$=2.5V
$V_{CTL(H)}$=2.7V
$V_{CTL(H)}$=3.0V
$V_{CTL(H)}$=4.0V
$V_{CTL(H)}$=5.0V

■ **APPLICATION CIRCUIT**

(TOP VIEW)
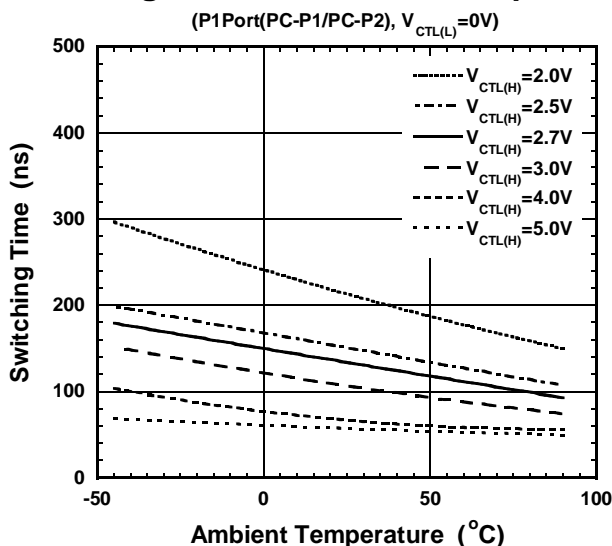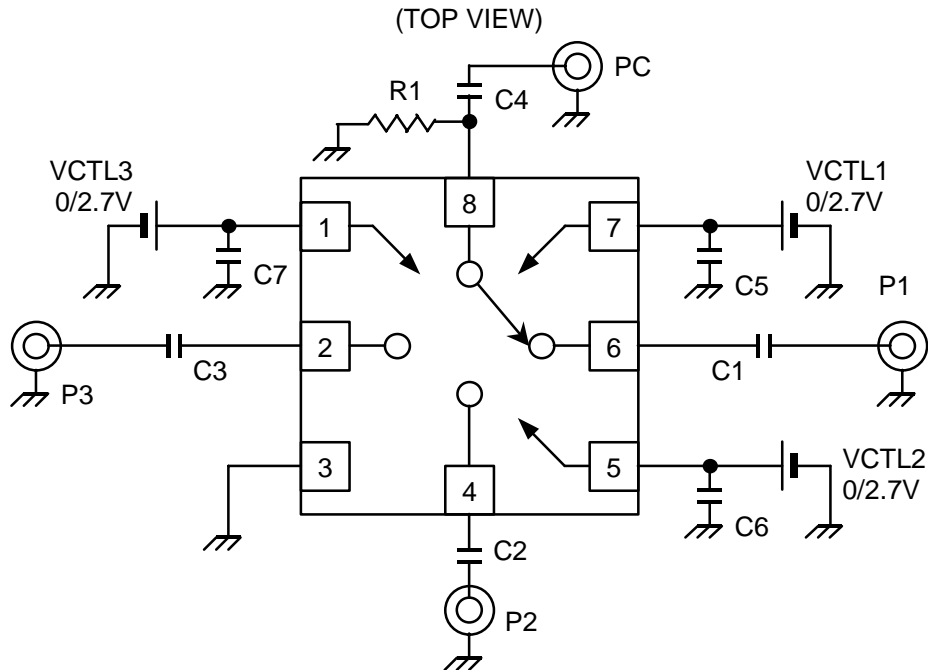


### Parts List

| Parts number | Value | Notes |
|---|---|---|
| C1~C4 | 56pF | GRM15 MURATA |
| C5~C7 | 10pF | |
| R1 | 560k ohm | - |

■ **TEST PCB LAYOUT**

(TOP VIEW)
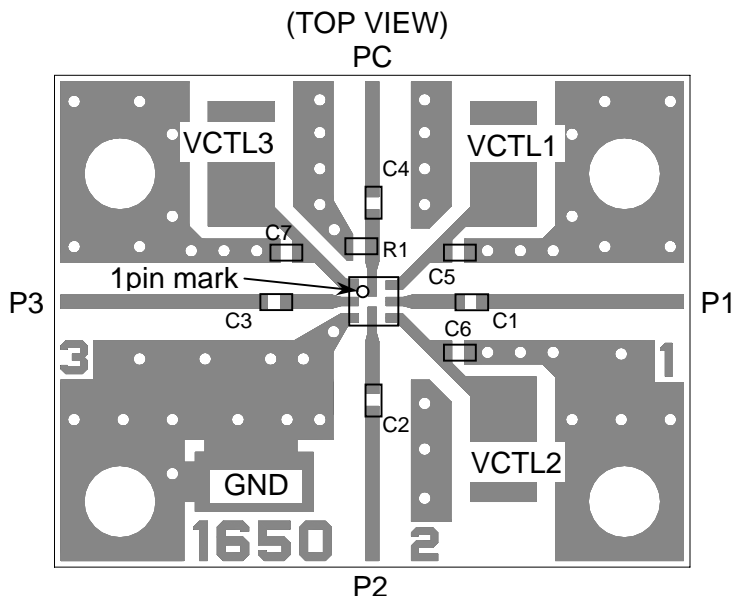


PCB SIZE=19.4x14.0mm

PCB: FR-4, t=0.2mm

CAPACITOR: size 1005

Stlipline =0.4mm

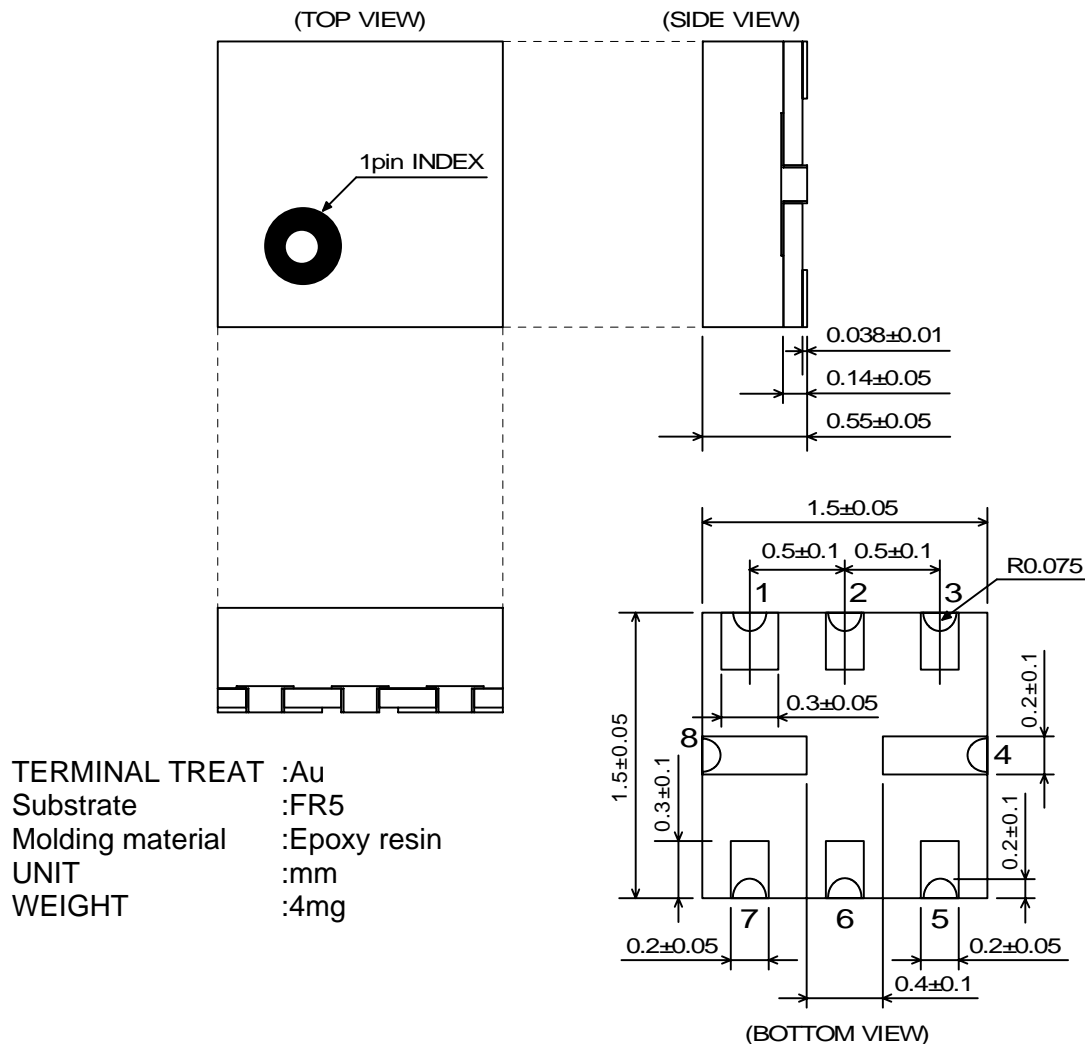### Losses of PCB, Connector and capacitors

| Freq.(GHz) | Loss (dB) |
|---|---|
| 1.0 | 0.21 |
| 2.0 | 0.30 |
| 2.5 | 0.35 |

**PRECAUTIONS**

[1] The DC blocking capacitors have to be placed at RF terminal of P1, P2, P3 and PC.

[2] To reduce stripline influence on RF characteristics, please locate bypass capacitors (C5~C7) close to each terminal.

[3] For good isolation, the GND terminal must be connected with the ground plane of substrate, and through-holes for GND should be placed near by the IC.

# NJG1650HB6

## ■PACKAGE OUTLINE (USB8-B6)

(TOP VIEW)

(SIDE VIEW)

1pin INDEX

0.038±0.01

0.14±0.05

0.55±0.05

1.5±0.05

0.5±0.1   0.5±0.1

R0.075

1   2   3

0.3±0.05

0.2±0.1

8              4

1.5±0.05

0.3±0.1

0.2±0.1

7   6   5

0.2±0.05

0.2±0.05

0.4±0.1

(BOTTOM VIEW)

TERMINAL TREAT :Au
Substrate          :FR5
Molding material  :Epoxy resin
UNIT               :mm
WEIGHT            :4mg