# V29C51001T/V29C51001B
# 1 MEGABIT (131,072 x 8 BIT)
# 5 VOLT CMOS FLASH MEMORY

**PRELIMINARY**

## Features

- 128Kx8-bit Organization
- Address Access Time: 55, 70, 90 ns
- Single 5V ± 10% Power Supply
- Sector Erase Mode Operation
- 8KB Boot Block (lockable)
- 512 bytes per Sector, 256 Sectors
  - Sector-Erase Cycle Time: 10ms (Max)
  - Byte-Program Cycle Time: 20μs (Max)
- Minimum 10,000 Erase-Program Cycles
- Low power dissipation
  - Active Read Current: 20mA (Typ)
  - Active Program Current: 30mA (Typ)
  - Standby Current: 100μA (Max)
- Hardware Data Protection
- Low $V_{CC}$ Program Inhibit Below 3.2V
- Self-timed program/erase operations with end-of-cycle detection
  - $\overline{DATA}$ Polling
  - Toggle Bit
- CMOS and TTL Interface
- Available in two versions
  - V29C51001T (Top Boot Block)
  - V29C51001B (Bottom Boot Block)
- Packages:
  - 32-pin Plastic DIP
  - 32-pin TSOP-I
  - 32-pin PLCC

## Description

The V29C51001T/V29C51001B is a high speed 131,072 x 8 bit CMOS flash memory. Programming or erasing the device is done with a single 5 Volt power supply. The device has separate chip enable CE, program enable $\overline{WE}$, and output enable $\overline{OE}$ controls to eliminate bus contention.

The V29C51001T/V29C51001B offers a combination of features: Boot Block with Sector Erase Mode. The end of program/erase cycle is detected by $\overline{DATA}$ Polling of $I/O_7$ or by the Toggle Bit $I/O_6$.

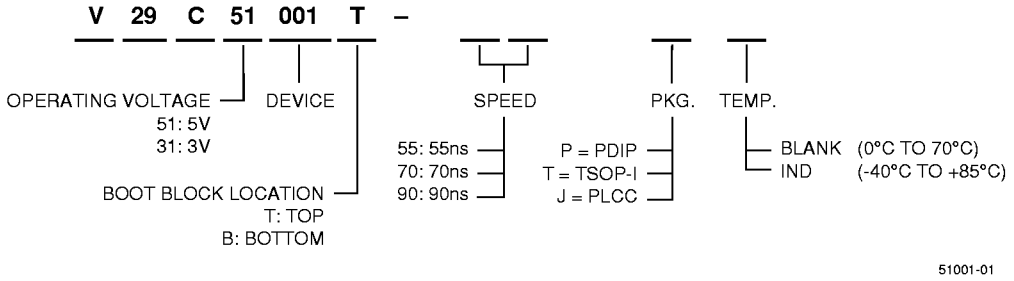
The V29C51001T/V29C51001B features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. The device also supports full chip erase.

Boot block architecture enables the device to boot from either the top (V29C51001T) or bottom (V29C51001B) sector. All inputs and outputs are CMOS and TTL compatible.

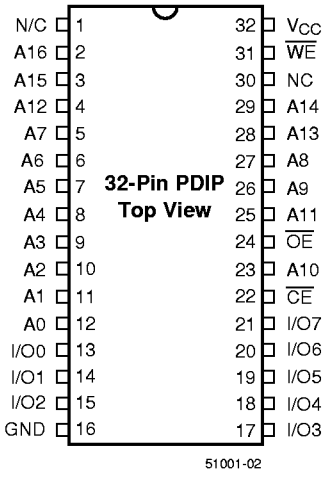
The V29C51001T/V29C51001B is ideal for applications that require updatable code and data storage.

## Device Usage Chart

| Operating Temperature Range | Package Outline | | | Access Time (ns) | | | Power | Temperature Mark |
|---|---|---|---|---|---|---|---|---|
| | P | T | J | 55 | 70 | 90 | Std. | |
| 0°C to 70 °C | • | • | • | • | • | • | • | Blank |
| –40°C to +85°C | • | • | • | • | • | • | • | I |

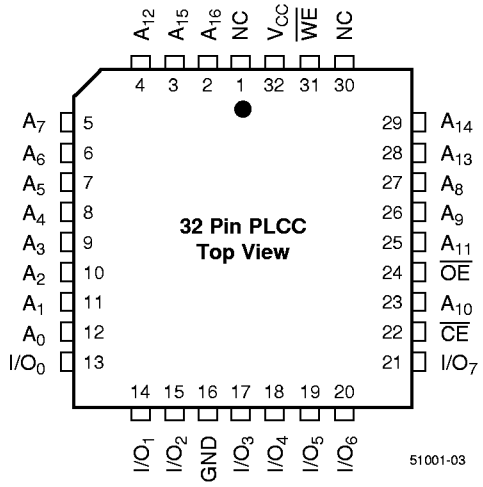


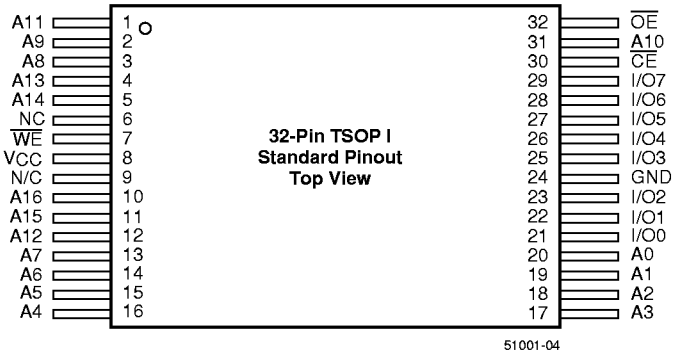

## Pin Configurations



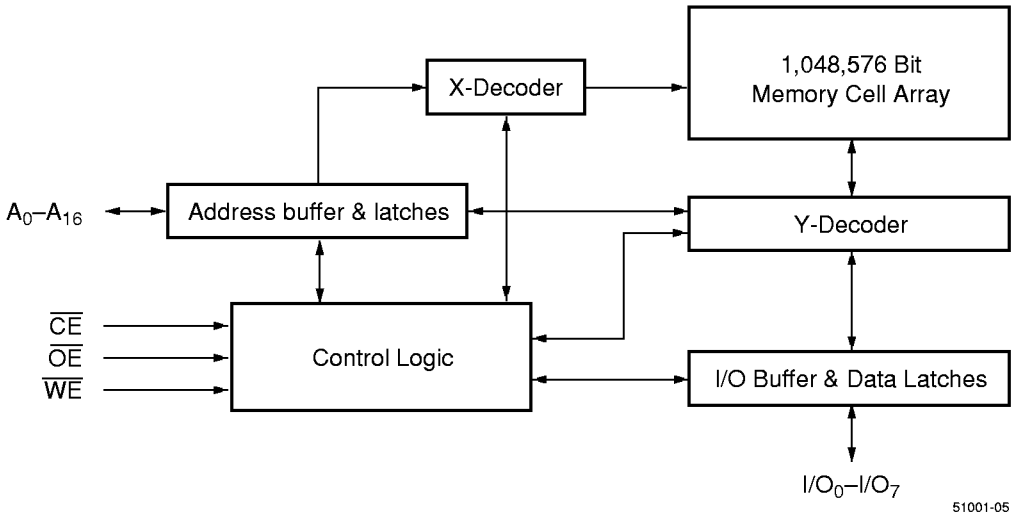

## Pin Names

| | |
|---|---|
| $A_0$–$A_{16}$ | Address Inputs |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Program Enable |
| $V_{CC}$ | 5V ± 10% Power Supply |
| GND | Ground |
| NC | No Connect |



## Functional Block Diagram




## Capacitance (1,2)

| Symbol | Parameter | Test mSetup | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6 | 8 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 8 | 10 | pF |

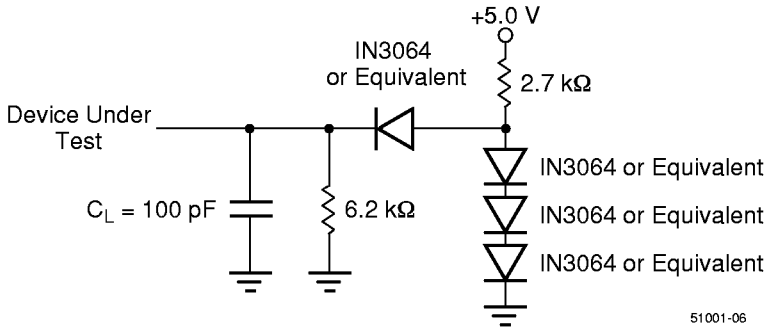
**NOTE:**
1. Capacitance is sampled and not 100% tested.
2. $T_A$ = 25°C, $V_{CC}$ = 5V ± 10%, f = 1 MHz.

## Latch Up Characteristics(1)

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| Input Voltage with Respect to GND on $A_9$, $\overline{OE}$ | -1 | +13 | V |
| Input Voltage with Respect to GND on I/O, address or control pins | -1 | $V_{CC}$ + 1 | V |
| $V_{CC}$ Current | -100 | +100 | mA |

**NOTE:**
1. Includes all pins except $V_{CC}$. Test conditions: $V_{CC}$ = 5V, one pin at a time.

## AC Test Load



## Absolute Maximum Ratings[1]

| Symbol | Parameter | Commercial | Extended | Unit |
|---|---|---|---|---|
| $V_{IN}$ | Input Voltage (input or I/O pins) | -2 to +7 | -2 to +7 | V |
| $V_{IN}$ | Input Voltage ($A_9$ pin, $\overline{OE}$) | -2 to +13 | -2 to +13 | V |
| $V_{CC}$ | Power Supply Voltage | -0.5 to +5.5 | -0.5 to +5.5 | V |
| $T_{STG}$ | Storage Temerpature (Plastic) | -65 to +125 | -65 to +150 | °C |
| $T_{OPR}$ | Operating Temperature | 0 to +70 | -40 to + 125 | °C |
| $I_{OUT}$ | Short Circuit Current[2] | 200 (Max.) | 200 (Max.) | mA |

**NOTE:**
1. Stress greater than those listed unders "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. No more than one output maybe shorted at a time and not exceeding one second long.

## DC Electrical Characteristics

(over the commercial operating range)

| Parameter Name | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | $V_{CC} = V_{CC}$ Min. | — | 0.8 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC} = V_{CC}$ Max. | 2 | — | V |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = GND to $V_{CC}$, $V_{CC} = V_{CC}$ Max. | — | ±1 | µA |
| $I_{OL}$ | Output Leakage Current | $V_{OUT}$ = GND to $V_{CC}$, $V_{CC} = V_{CC}$ Max. | — | ±1 | µA |
| $V_{OL}$ | Output LOW Voltage | $V_{CC} = V_{CC}$ Min., $I_{OL}$ = 2.1mA | — | 0.4 | V |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC} = V_{CC}$ Min, $I_{OH}$ = -400µA | 2.4 | — | V |
| $I_{CC1}$ | Read Current | $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/Os open, Address input = $V_{IL}/V_{IH}$, at f = $1/t_{RC}$ Min., $V_{CC} = V_{CC}$ Max. | — | 40 | mA |
| $I_{CC2}$ | Program Current | $\overline{CE} = \overline{WE}$ = VIL, $\overline{OE} = V_{IH}$, $V_{CC} = V_{CC}$ Max. | — | 50 | mA |
| $I_{SB}$ | TTL Standby Current | $\overline{CE} = \overline{OE} = \overline{WE} = V_{IH}$, $V_{CC} = V_{CC}$ Max. | — | 2 | mA |
| $I_{SB1}$ | CMOS Standby Current | $\overline{CE} = \overline{OE} = \overline{WE} = V_{CC} - 0.3V$, $V_{CC} = V_{CC}$ Max. | — | 100 | µA |
| $V_H$ | Device ID Voltage for $A_9$ | $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ | 11.5 | 12.5 | V |
| $I_H$ | Device ID Current for $A_9$ | $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, A9 = $V_H$ Max. | — | 50 | µA |

## AC Electrical Characteristics

(over all temperature ranges)

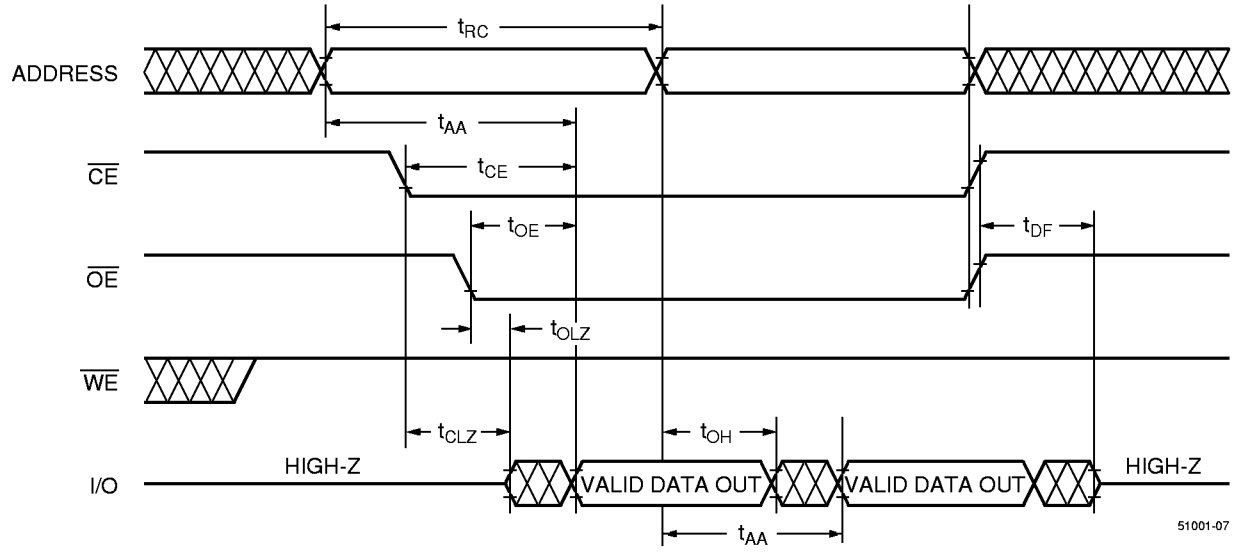
### Read Cycle

| Parameter Name | Parameter | -55 | | -70 | | -90 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 55 | — | 70 | — | 90 | — | ns |
| $t_{AA}$ | Address Access Time | — | 55 | — | 70 | — | 90 | ns |
| $t_{ACS}$ | Chip Enable Access Time | — | 55 | — | 70 | — | 90 | ns |
| $t_{OE}$ | Output Enable Access Time | — | 30 | — | 35 | — | 40 | ns |
| $t_{CLZ}$ | $\overline{CE}$ Low to Output Active | 0 | — | 0 | — | 0 | — | ns |
| $t_{OLZ}$ | $\overline{OE}$ Low to Output Active | 0 | — | 0 | — | 0 | — | ns |
| $t_{DF}$ | Output Enable or Chip Disable to Output in High Z | 0 | 15 | 0 | 20 | 0 | 20 | ns |
| $t_{OH}$ | Output Hold from Address Change | 0 | — | 0 | — | 0 | — | ns |

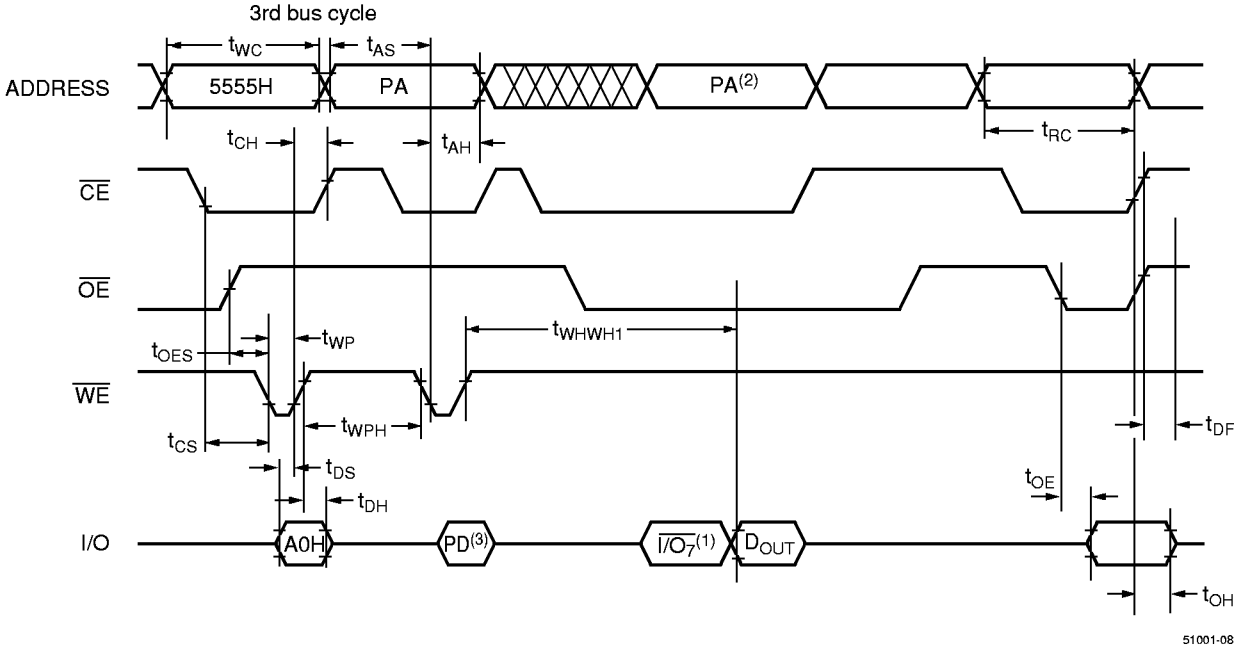
### Program (Erase/Program) Cycle

| Parameter Name | Parameter | -55 | | | -70 | | | -90 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $t_{WC}$ | Program Cycle Time | 55 | — | — | 70 | — | — | 90 | — | — | ns |
| $t_{AS}$ | Address Setup Time | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{AH}$ | Address Hold Time | 40 | — | — | 45 | — | — | 45 | — | — | ns |
| $t_{CS}$ | $\overline{CE}$ Setup Time | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{CH}$ | $\overline{CE}$ Hold Time | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{OES}$ | $\overline{OE}$ Setup Time | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{OEH}$ | $\overline{OE}$ High Hold Time | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{WP}$ | $\overline{WE}$ Pulse Width | 30 | — | — | 35 | — | — | 45 | — | — | ns |
| $t_{WPH}$ | $\overline{WE}$ Pulse Width High | 30 | — | — | 35 | — | — | 35 | — | — | ns |
| $t_{DS}$ | Data Setup Time | 20 | — | — | 25 | — | — | 30 | — | — | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{WHWH1}$ | Programming Cycle | — | — | 20 | — | — | 20 | — | — | 20 | µs |
| $t_{WHWH2}$ | Sector Erase Cycle | — | — | 10 | — | — | 10 | — | — | 10 | ms |
| $t_{WHWH3}$ | Chip Erase Cycle | — | 500 | — | — | 500 | — | — | 500 | — | ms |

## Waveforms of Read Cycle



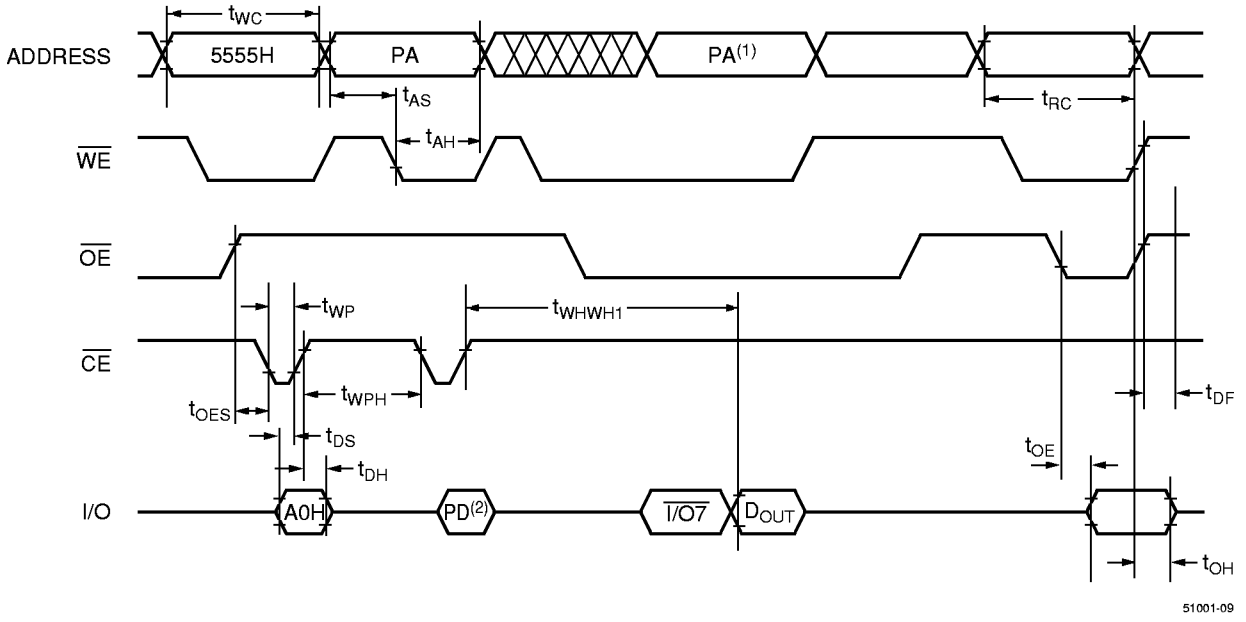

## Waveforms of $\overline{WE}$ Controlled-Program Cycle



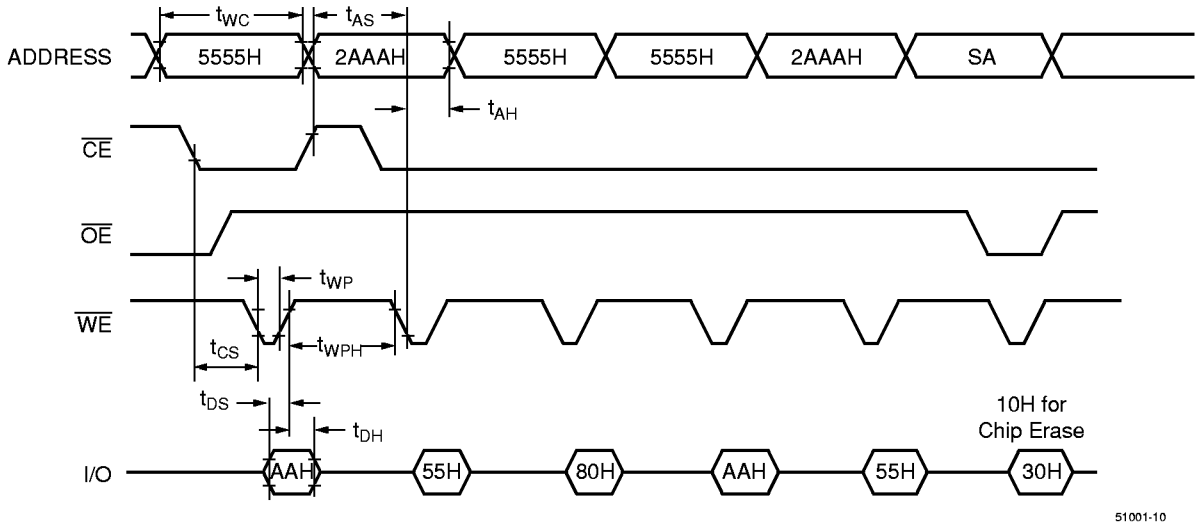

**NOTES:**

1. $I/O_7$: The output is the complement of the data written to the device.
2. PA: The address of the memory location to be programmed.
3. PD: The data at the byte address to be programmed.

## Waveforms of CE Controlled-Program Cycle



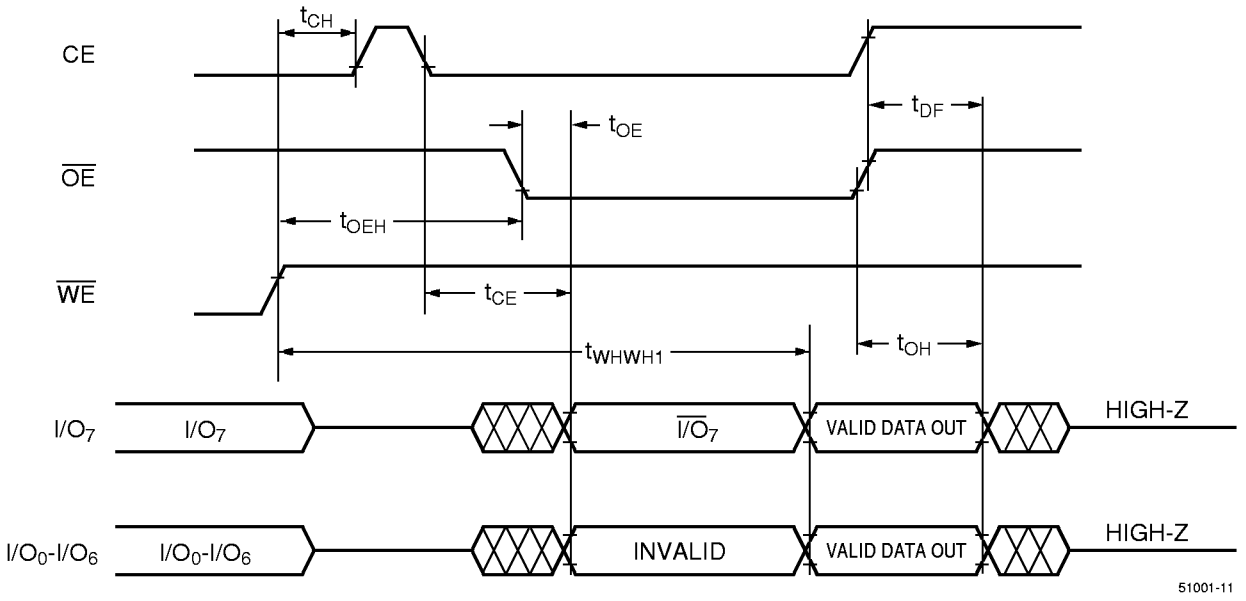

## Waveforms of Erase Cycle(1)



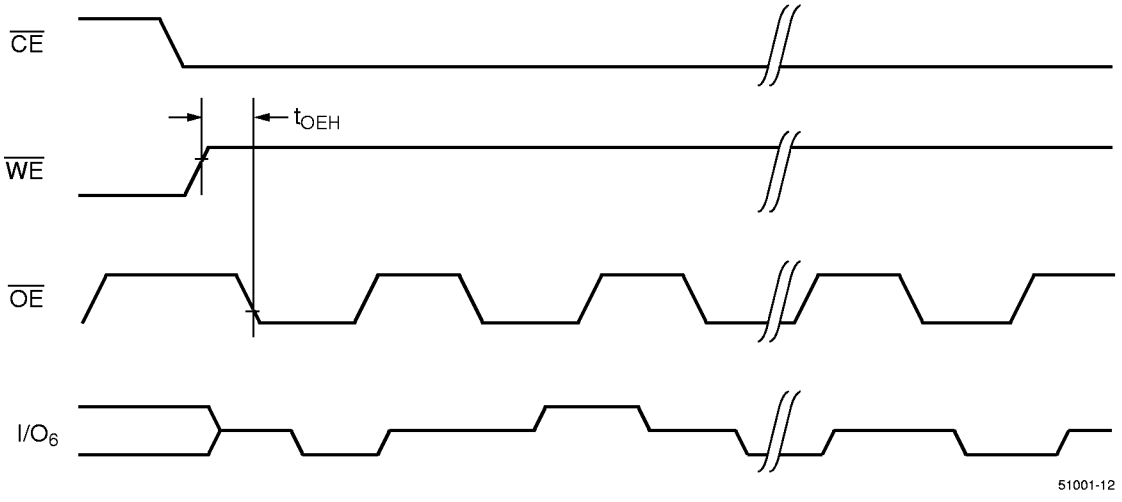

**NOTES:**

1. PA: The address of the memory location to be programmed.
2. PD: The data at the byte address to be programmed.
3. SA: The sector address for Sector Erase. Address = don't care for Chip Erase.

### Waveforms of $\overline{DATA}$ Polling Cycle




### Waveforms of Toggle Bit Cycle



## Functional Description

The V29C51001T/V29C51001B consists of 256 equally-sized sectors of 512 bytes each. The 8 KB lockable Boot Block is intended for storage of the system BIOS boot code. The boot code is the first piece of code executed each time the system is powered on or rebooted.

The V29C51001 is available in two versions: the V29C51001T with the Boot Block address starting from 1E000H to 1FFFFH, and the V29C51001B with the Boot Block address starting from 00000H to 1FFFFH.

## Read Cycle

A read cycle is performed by holding both $\overline{CE}$ and $\overline{OE}$ signals LOW. Data Out becomes valid only when these conditions are met. During a read cycle $\overline{WE}$ must be HIGH prior to $\overline{CE}$ and $\overline{OE}$ going LOW. $\overline{WE}$ must remain HIGH during the read operation for the read to complete (see Table 1).

## Output Disable

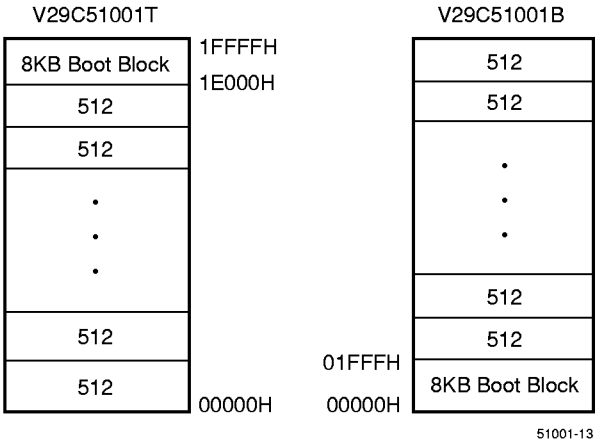
Returning $\overline{OE}$ or $\overline{CE}$ HIGH, whichever occurs first will terminate the read operation and place the I/O pins in the HIGH-Z state.

## Standby

The device will enter standby mode when the $\overline{CE}$ signal is HIGH. The I/O pins are placed in the HIGH-Z, independent of the $\overline{OE}$ signal.

## Byte Program Cycle

The V29C51001T/V29C51001B is programmed on a byte-by-byte basis. The byte program operation is initiated by using a specific four-bus-cycle sequence: two unlock program cycles, a program setup command and program data program cycles (see Table 2).




**8KB Boot Block = 16 Sectors**

During the byte program cycle, addresses are latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever is last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is first. The byte program cycle can be $\overline{CE}$ controlled or $\overline{WE}$ controlled.

## Sector Erase Cycle

The V29C51001T/V29C51001B features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. Sector erase operation is initiated by using a specific six-bus-cycle sequence: Two unlock program cycles, a setup command, two additional unlock program cycles, and the sector erase command (see Table 2). A sector must be first erased before it can be reprogrammed. While in the internal erase mode, the device ignores any program attempt into the device. The internal erase completion can be determined via DATA polling or toggle bit.

The V29C51001T/V29C51001B is shipped with pre-erased sectors (all bits = 1).

## Table 1. Operation Modes Decoding

| Decoding Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $A_0$ | $A_1$ | $A_9$ | I/O |
|---|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $A_0$ | $A_1$ | $A_9$ | READ |
| Program | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $A_0$ | $A_1$ | $A_9$ | PD |
| Standby | $V_{IH}$ | X | X | X | X | X | HIGH-Z |
| Autoselect Device ID | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | $V_H$ | CODE |
| Autoselect Manufacture ID | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_H$ | CODE |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | X | X | HIGH-Z |

**NOTES:**
1. X = Don't Care, $V_{IH}$ = HIGH, $V_{IL}$ = LOW.
2. PD: The data at the byte address to be programmed.

### Table 2. Command Codes

| Command Sequence | First Bus Program Cycle | | Second Bus Program Cycle | | Third Bus Program Cycle | | Fourth Bus Program Cycle | | Fifth Bus Program Cycle | | Six Bus Program Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Address | Data | Address | Data | Address | Data | Address | Data | Address | Data | Address | Data |
| Read | XXXXH | F0H | | | | | | | | | | |
| Read | 5555H | AAH | 2AAAH | 55H | 5555H | F0H | RA | RD | | | | |
| Autoselect | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | 00H | 40H | | | | |
| | | | | | | | 01H | 01H(1)<br>A1H(2) | | | | |
| Byte Program | 5555H | AAH | 2AAAH | 55H | 5555H | A0H | PA | PD(4) | | | | |
| Chip Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 10H |
| Sector Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | PA(3) | 30H |

**NOTES:**
1. Top Boot Sector
2. Bottom Boot Sector
3. PA: The address of the memory location to be programmed.
4. PD: The data at the byte address to be programmed.

### Chip Erase Cycle

The V29C51001T/V29C51001B features a chip-erase operation. The chip erase operation is initiated by using a specific six-bus-cycle sequence: two unlock program cycles, a setup command, two additional unlock program cycles, and the chip erase command (see Table 2).

The chip erase operation is performed sequentially, one sector at a time. When the automated on chip erase algorithm is requested with the chip erase command sequence, the device automatically programs and verifies the entire memory array for an all zero pattern prior to erasure

The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}$ pulse in the command sequence and terminates when the data on DQ7 is "1".

### Program Cycle Status Detection

There are two methods for determining the state of the V29C51001T/V29C51001B during a program (erase/program) cycle: $\overline{DATA}$ Polling ($I/O_7$) and Toggle Bit ($I/O_6$).

### $\overline{DATA}$ Polling ($I/O_7$)

The V29C51001T/V29C51001B features $\overline{DATA}$ polling to indicate the end of a program cycle. When the device is in the program cycle, any attempt to read the device will received the complement of the loaded data on $I/O_7$. Once the program cycle is completed, $I/O_7$ will show true data, and the device is then ready for the next cycle.

### Toggle Bit ($I/O_6$)

The V29C51001T/V29C51001B also features another method for determining the end of a program cycle. When the device is in the program cycle, any attempt to read the device will result in $I/O_6$ toggling between 1 and 0. Once the program is completed, the toggling will stop. The device is then ready for the next operation. Examining the toggle bit may begin at any time during a program cycle.

### Boot Block Protection

The V29C51001T/V29C51001B features hardware Boot Block Protection. This feature will prevent erasing/programming of data in the Boot Block once the feature is enabled (see Table 3). The device is shipped with the Boot Block unprotected.

### Autoselect

The V29C51001T/V29C51001B features an Autoselect mode to identify *the Boot Block (protected/unprotected), the Device (Top/Bottom), and the manufacturer ID.*

To get to the Autoselect mode, a high voltage ($V_H$) must be applied to the $A_9$ pin. Once the $A_9$ signal is returned to LOW or HIGH, the device will return to the previous mode.

### Boot Block Detection

In Autoselect mode, performing a read at address 3CXX2H or address 0CXX2H will indicate if the Top Boot Block sector or the Bottom Boot Block sector is locked out. If the data is 01H, the Top/Bottom Boot Block is protected. If the data is 00H, the Top/Bottom Boot Block is unprotected. (see Table 3.)

### Device ID

In Autoselect mode, performing a read at address XXXXH will determine whether the device is a Top Boot Block device or a Bottom Boot Block device. If the data is 01H, the device is a Top Boot Block. If the data is A1H, the device is a Bottom Boot Block device (see Table 3).

In addition, the device ID can also be read via the command register when the device is erased or programmed in a system without applying high voltage to the $A_9$ pin. When $A_0$ is HIGH, the device ID is presented at the outputs.

### Manufacturer ID

In Autoselect mode, performing a read at address. XXXX0H will determine the manufacturer ID. 40H is the manufacturer code for Mosel Vitelic Flash.

In addition the manufacturer ID can also be read via the command register when the device is erased or programmed in a system without applying high voltage to the $A_9$ pin. when $A_0$ is LOW, the manufacturer ID is presented at the outputs.

### Hardware Data Protection

*$V_{CC}$ Sense Protection:* the program operation is inhibited when VCC is less than 2.5V.

*Noise Protection:* a CE or WE pulse of less than 5ns will not initiate a program cycle.

*Program Inhibit Protection:* holding any one of OE LOW, CE HIGH or WE HIGH inhibits a program cycle.

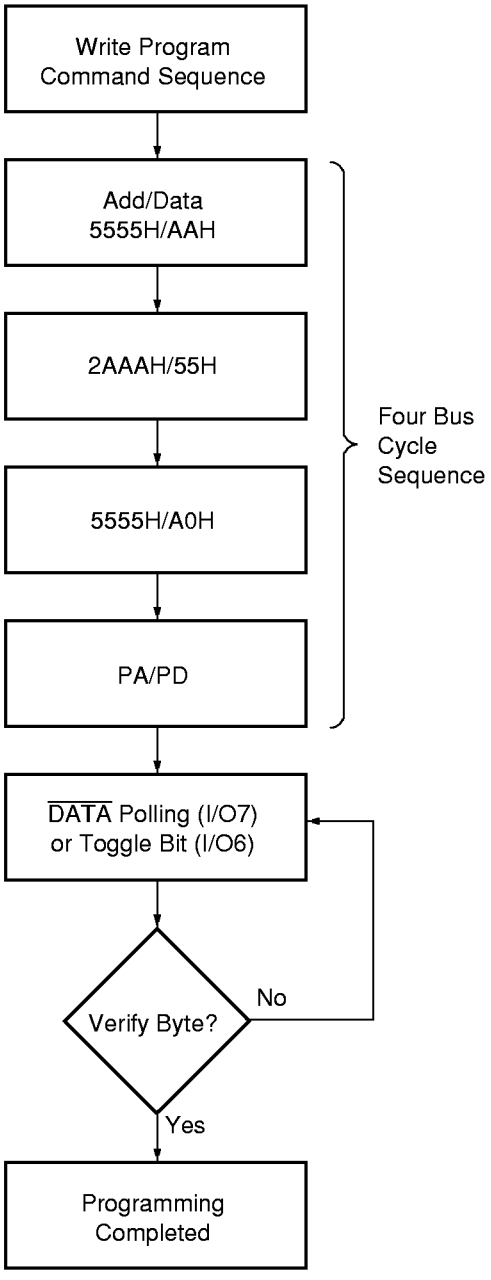
### Table 3. Autoselect Decoding

| Decoding Mode | Boot Block | Address | | | | Data $I/O_0$–$I/O_7$ |
|---|---|---|---|---|---|---|
| | | $A_0$ | $A_1$ | $A_2$–$A_{13}$ | $A_{14}$–$A_{16}$ | |
| Boot Block Protection | Top | $V_{IL}$ | $V_{IH}$ | X | $V_{IH}$ | 01H: protected |
| | Bottom | $V_{IL}$ | $V_{IH}$ | X | $V_{IL}$ | 00H: unprotected |
| Device ID | Top | $V_{IH}$ | $V_{IL}$ | X | X | 01H |
| | Bottom | | | | | A1H |
| Manufacture ID | | $V_{IL}$ | $V_{IL}$ | X | X | 40H |

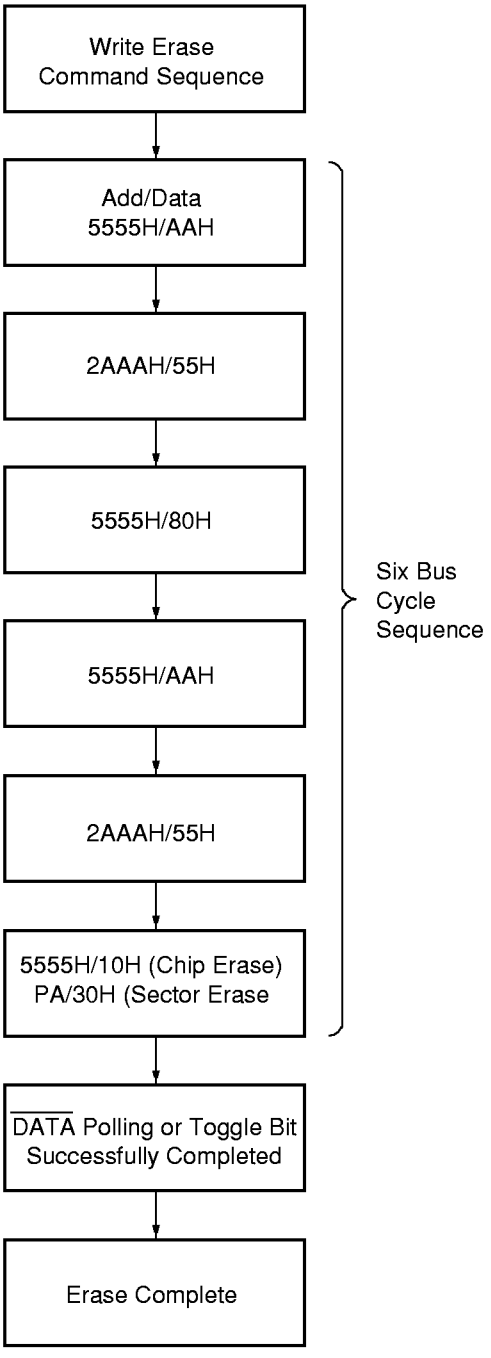
**NOTE:**

1. X = Don't Care, $V_{IH}$ = HIGH, $V_{IL}$ = LOW.

### Byte Program Algorithm

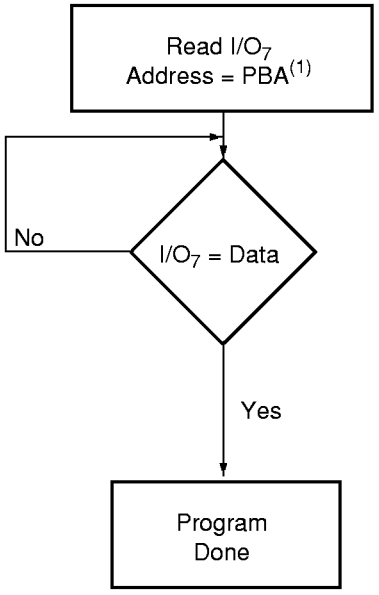



### Chip/Sector Erase Algorithm

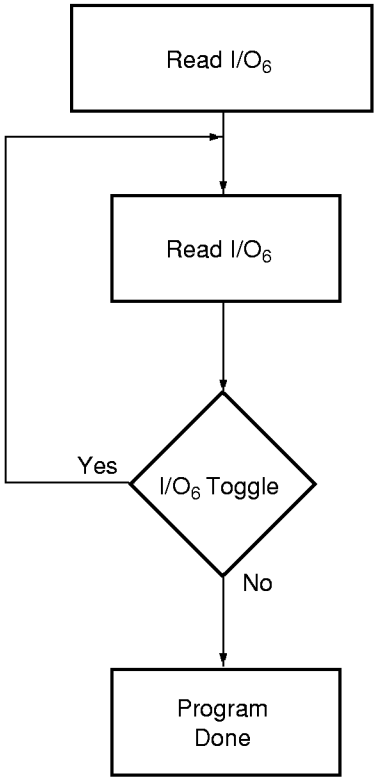



51001-14

### DATA Polling Algorithm




### Toggle Bit Algorithm

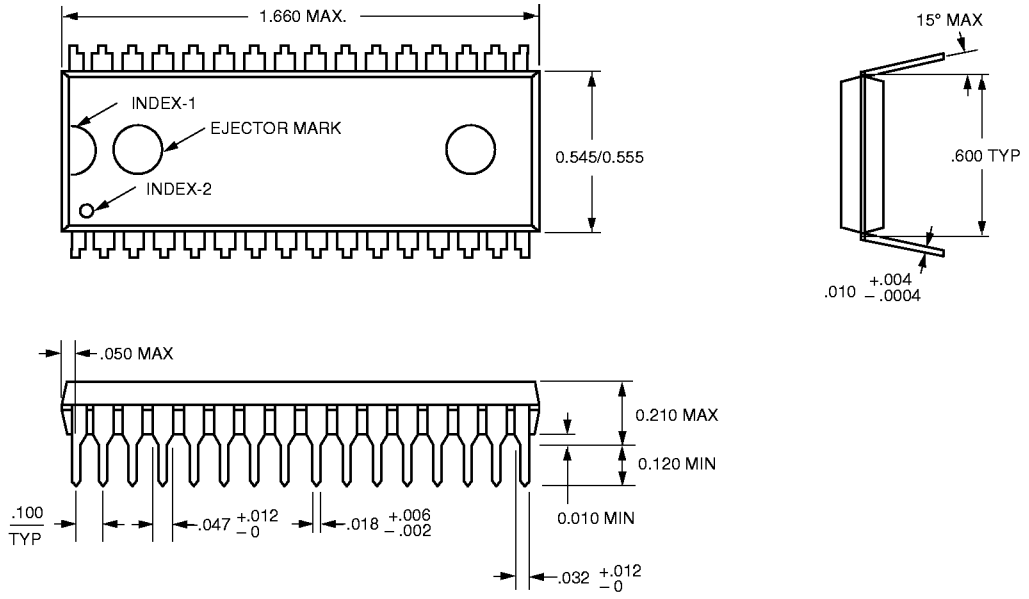



51002-17

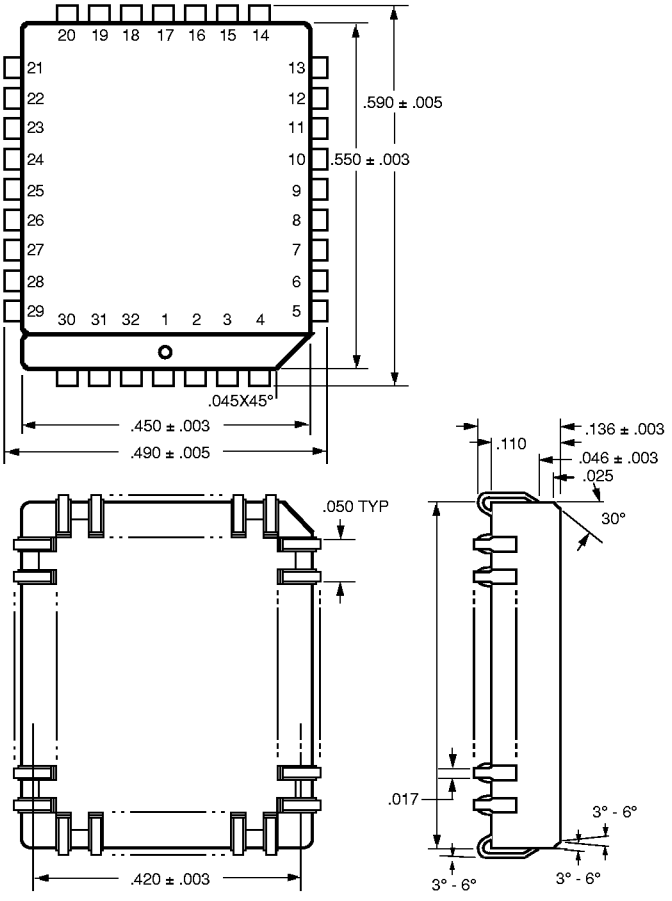
**NOTE:**
1. PBA: The byte address to be programmed.

## Package Diagrams

### 32-pin Plastic DIP

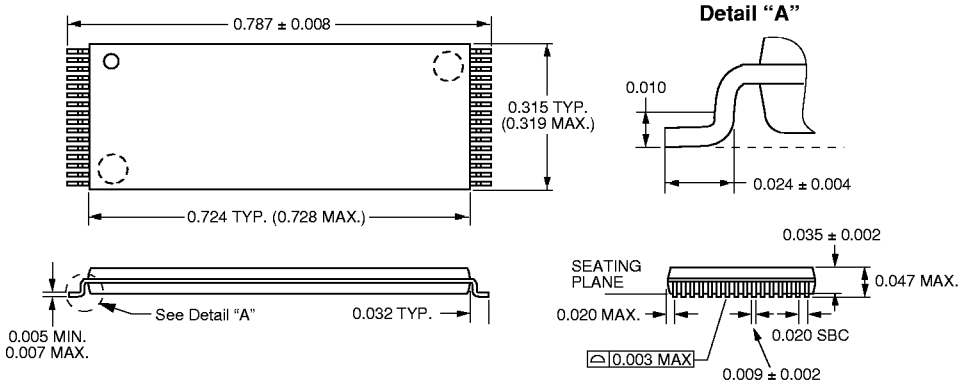



### 32-pin PLCC



## 32-pin TSOP-I

**Units in inches**



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