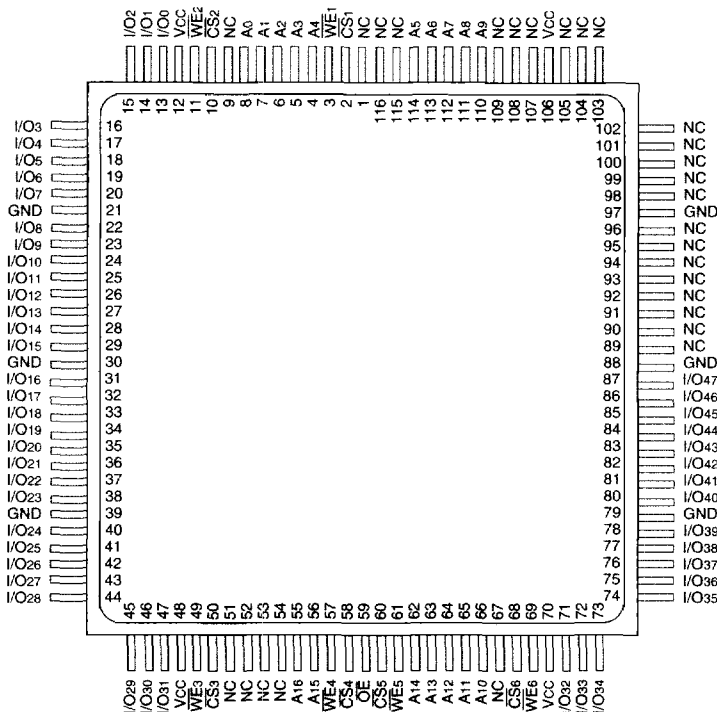
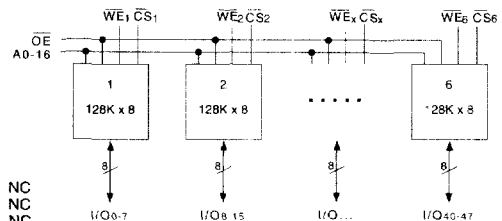


**128Kx48 3.3V SRAM MODULE** *ADVANCED****FEATURES**

- Access Times 15, 17, 20, 25ns
- Packaging
 - 116 Lead, 40.0mm Hermetic CQFP (Package 504)
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt Power Supply
- Low Power CMOS
- Organized as 128K x 48, Data Width is user configurable.

- 2V Data Retention Devices Available (Low Power Version)
- TTL Compatible Inputs and Outputs
- Weight
WS128K48V-XG4WX - 20 grams typical

* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

PIN CONFIGURATION FOR WS128K48V-XG4WX**TOP VIEW****BLOCK DIAGRAM****PIN DESCRIPTION**

I/O0-47	Data Inputs/Outputs
A0-16	Address Inputs
WE1-6	Write Enables
CS1-6	Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-65	+150	$^{\circ}\text{C}$
Signal Voltage Relative to GND	V_S	-0.5	4.6	V
Junction Temperature	T_J		150	$^{\circ}\text{C}$
Supply Voltage	V_{CC}	-0.5	4.6	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	$^{\circ}\text{C}$

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(TA = +25 $^{\circ}\text{C}$)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$	100	pF
$\overline{WE}$ capacitance	C_{WE}	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$	20	pF
$\overline{CS}$ capacitance	C_{CS}	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$, $f = 1.0\text{ MHz}$	20	pF
Address input capacitance	C_{AD}	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$	100	pF

This parameter is guaranteed by design but not tested.

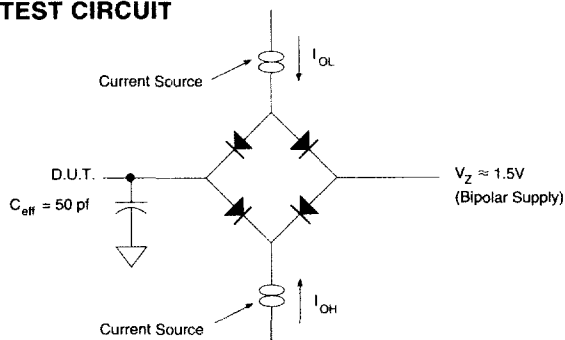
DC CHARACTERISTICS

(VCC = 3.3V $\pm$ 0.3V, TA = -55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	$V_{IN} = \text{GND to } V_{CC}$		10	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, $V_{OUT} = \text{GND to } V_{CC}$		10	μA
Operating Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, $f = 5\text{ MHz}$, $V_{CC} = 3.6$		750	mA
Standby Current	I_{SB}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, $f = 5\text{ MHz}$, $V_{CC} = 3.6$		48	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8\text{ mA}$		0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4.0\text{ mA}$	2.4		V

NOTE: DC test conditions: $V_{IH} = V_{CC} - 0.3\text{V}$, $V_{IL} = 0.3\text{V}$

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0$, $V_{IH} = 2.5$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75\ \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.

**AC CHARACTERISTICS**

(VCC = 3.3V ± 0.3V, TA = -55°C To +125°C)

Parameter Read Cycle	Symbol	-15		-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	15		17		20		25		ns
Address Access Time	t _{AA}		15		17		20		25	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		ns
Chip Select Access Time	t _{ACS}		15		17		20		25	ns
Output Enable to Output Valid	t _{OE}		10		10		12		15	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	3		3		3		3		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		10		10		12		12	ns
Output Disable to Output in High Z	t _{OHZ} ¹		10		10		12		12	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

(VCC = 3.3V ± 0.3V, TA = -55°C To +125°C)

Parameter Write Cycle	Symbol	-15		-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	15		17		20		25		ns
Chip Select to End of Write	t _{CW}	14		14		15		20		ns
Address Valid to End of Write	t _{AW}	14		15		15		20		ns
Data Valid to End of Write	t _{DW}	10		10		12		15		ns
Write Pulse Width	t _{WP}	14		14		15		20		ns
Address Setup Time	t _{AS}	0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		ns
Output Active from End of Write	t _{OW} ¹	3		3		3		3		ns
Write Enable to Output in High Z	t _{WHZ} ¹		10		10		12		15	ns
Data Hold Time	t _{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

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SRAM MODULES



ORDERING INFORMATION

W S 128K48 V - XXX G4W X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

G4W = 116 Lead 40mm Ceramic Quad Flat Pack, CQFP (Package 504)

ACCESS TIME (ns)

Low Voltage Supply 3.3V $\pm$ 10%

ORGANIZATION, 128K x 48

SRAM

WHITE MICROELECTRONICS