PRELIMINARY INFORMATION MK0220

## Description

The MK0220 provides clocks for video CD systems. It is designed to work specifically with the C-Cube CL480, and supports audio DAC's like the Crystal CS4333, and NTSC/PAL encoders such as Brooktree's Bt851.

The chip uses MicroClock's proprietary analog Phase-Locked Loop technology, and locks to the CD output reference clock of 2.1168 MHz to produce four output clocks.

MicroClock can customize this device for any different frequencies for a small NRE.

#### Features

- Packaged in 16 pin narrow (150 mil) SOIC
- Fully compatible with C-Cube CL480
- Supports Crystal Semiconductor's CS4333
- Supports timing for Bt851 NTSC/PAL encoder
- CD clock input eliminates crystals and oscillators
- All clocks are frequency-locked to the CD clock
- 2.7V to 5.5V operation
- Zero ppm error 16.9344, 13.5, 27.0 MHz clocks
- Power down mode reduces IDD to 10µA (typ)



Signal names in parentheses under the outputs indicate the corresponding input pins of the CL480 needing this clock.

## **Block Diagram**

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## **Pin Assignment**



Note on reference input - the MK0220 is designed to be used with a clock input into pin 3. This clock will come from the CD kit. While the chip can also be used with a 2.1168 MHz crystal, this is not a commonly stocked value. If a 2.1168 MHz clock is not available, contact MicroClock for other devices.

## **Pin Descriptions**

Number	Name	Туре	Description
1	GND	Р	Connect to ground.
2	X2	0	Crystal connection. Leave unconnected for clock input, or connect to 2.1168 MHz crystal.
3	X1/ICLK	Ι	Crystal connection. Connect to 2.1168 MHz input clock from CD (or crystal). See note above.
4	VDD	Р	Connect to +3.3V.
5	GND	Р	Connect to ground.
6	VDD	Р	Connect to +3.3V.
7	40M	0	40 MHz clock output. Use for GCK on CL480.
8	GND	Р	Connect to ground.
9	16.9M	0	16.9344 MHz clock output. Use for DA-XCK on CL480, MCLK on CS4333.
10	27M	0	27.00 MHz clock output. Leads 13.5M by 5ns. Use for VCK on CL480, NTSC/PAL encoder.
11	GND	Р	Connect to ground.
12	GND	Р	Connect to ground.
13	VDD	Р	Connect to +3.3V.
14	13.5M	0	13.5 MHz clock output. Lags 27M by 5ns.
15	NC	-	No Connect.
16	PD	Ι	Power down. Stops all clocks low when this pin is taken low.

Type: I = Input, O = output, P = power supply connection

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## MK0220 Video CD Clock Source

## **External Components**

The MK0220 requires a minimum number of external components for proper operation. Decoupling capacitors of  $0.1\mu$ F should be connected between VDD and GND on pins 4/5 and pins 13/12, as close to the MK0220 as possible. A series termination resistor of 33 may be used for each clock output. The device does not require (nor do we recommend) capacitors connected to the crystal pins. If a 2.1168 MHz crystal is used, it must be connected as close to the chip as possible. Recommended load capacitance for the crystal is 12pF.

## **Electrical Specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Units			
ABSOLUTE MAXIMUM RATINGS (Note 1)								
Supply Voltage, VDD	Referenced to GND			7	V			
Inputs and Clock Outputs		-0.5		VDD+0.5	V			
Ambient Operating Temperature		0		70	°C			
Soldering Temperature	Max of 20 seconds			260	°C			
Storage Temperature		-65		150	°C			
DC CHARACTERISTICS								
Operating Voltage, VDD		2.7		5.5	V			
Input High Voltage, VIH		2			V			
Input Low Voltage, VIL				0.8	V			
Output High Voltage	IOH=-4mA	VDD-0.4			V			
Output High Voltage	IOH=-25mA	2.4			V			
Output Low Voltage	IOL=25mA			0.4	V			
Operating Supply Current, IDD	No Load, VDD=3.6V		16	20	mA			
Operating Supply Current, IDD	No Load, VDD=3.0V		12	16	mA			
Standby Supply Current, IDD, at 3.6V	No Load, PD=0V		10		μA			
Short Circuit Current	Each output		±100		mA			
Input Capacitance, X1 and X2 pins			15		pF			
Input Capacitance			7		pF			
Actual mean frequency error versus target	40.0MHz output only			±100	ppm			
Actual mean frequency error versus target	Note 2			0	ppm			
AC CHARACTERISTICS				_				
Input Frequency			2.1168		MHz			
Output Clock Rise Time	0.8 to 2.0V			1.5	ns			
Output Clock Fall Time	2.0 to 0.8V			1.5	ns			
Output Clock Duty Cycle, High Time	At VDD/2	45	49 to 51	55	%			
Power down Time, $\overline{PD}$ taken low to clocks off				1	μs			
Power up Time, PD taken high to clocks stable			2.5	5	ms			

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

2. For the 13.5MHz, 16.9MHz, and 27MHz outputs

#### Package Outline and Package Dimensions



#### 16 pin SOIC narrow

	Inch	es	Millimeters		
Symbol	Min	Max	Min	Max	
Α	0.055	0.070	1.397	1.778	
b	0.013	0.019	0.330	0.483	
с	0.007	0.010	0.190	0.254	
D	0.385	0.400	9.779	10.160	
Е	0.150	0.160	3.810	4.064	
Н	0.225	0.245	5.715	6.223	
е	.050 BSC		1.27 BSC		
h		0.016		0.406	
Q	0.004	0.01	0.102	0.254	

## **Ordering Information**

Part/Order Number	Marking	Package	Temperature
MK0220-01S	MK0220-01S	16 pin narrow SOIC	0-70°C
MK0220-01STR	MK0220-01S	Add Tape & Reel	0-70°C

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CHANGE HISTORY <u>Version</u> <u>Date first published</u> A 6/1/95 B 6/22./95 C 9/18/95

<u>Comments</u> Original Changed operating voltage from 3.0-4.0V to 2.7V-3.6V. Corrected pin 14. Added 40MHz accuracy. Changed operating volyage to 2.7V-5.5V. Added specific pins for decoupling caps.