STK12C88

32K x 8 *AutoStore*™ nvSRAM High Performance CMOS Nonvolatile Static RAM

SIMTEK

PRELIMINARY

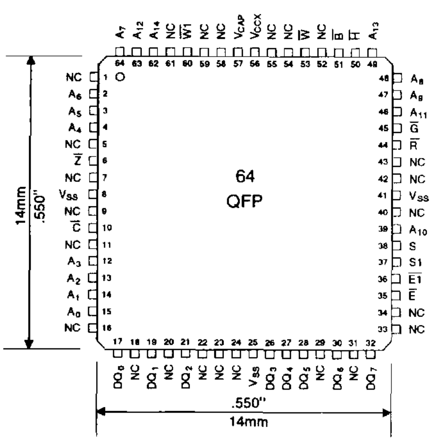
FEATURES

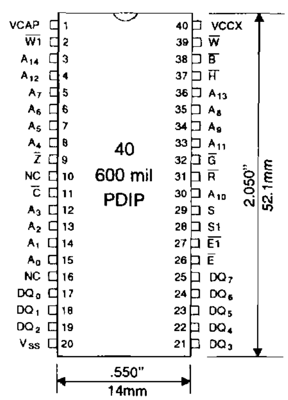
- **25ns, 35ns and 45ns Access Times**
- **Store to EEPROM Initiated by Hardware, Software or *AutoStore*™ on Power Down**
- **Recall to SRAM Initiated by Hardware Reset, Software or Power Restore**
- **"Hands-off" Store with 100μF Capacitor**
- **Low Power Sleep Mode: I_{CC} < 10μA**
- **25mA I_{CC} at 200ns Cycle Time**
- **Multiple Select and Enable Pins for Flexible Interface to Processors**
- **Separate Strobe Input for Software Control**
- **Unlimited Recalls from EEPROM to SRAM**
- **100,000 Store Cycles to EEPROM**
- **10 Year Data Retention in EEPROM**
- **Commercial and Industrial Temp. Ranges**
- **64 Pin PQFP and 40 Pin 600 mil PDIP Packages**

DESCRIPTION

The Simtek STK12C88 is a fast static RAM with a nonvolatile, electrically-erasable PROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent, nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) can take place automatically on power down using charge stored in an external capacitor. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of STORE and RECALL cycles can also be controlled by separate input pins or by entering control sequences on the SRAM inputs. Hardware reset and low power SLEEP mode functions are included.

PACKAGE DIAGRAMS

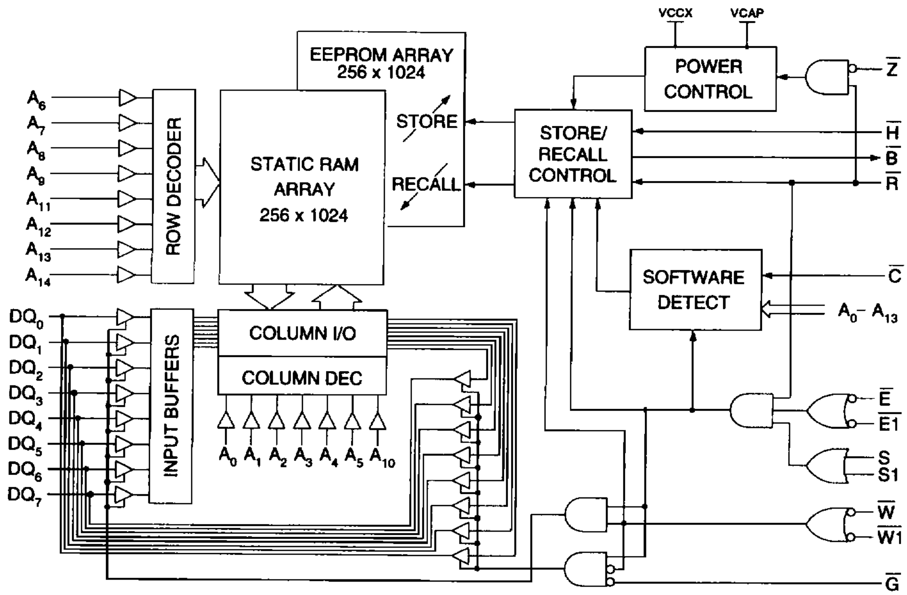




PIN NAMES

A_0 - A_{14}	Address Inputs
DQ_0 - DQ_7	Data In/Out
$\overline{E}$, $\overline{E1}$	Chip Enables (Low)
S, S1	Chip Selects (High)
$\overline{W}$, $\overline{W1}$	Write Enables
$\overline{G}$	Output Enable
$\overline{H}$	Hardware Store
$\overline{R}$	Hardware Reset
$\overline{B}$	Store Busy
$\overline{C}$	Software Clock
$\overline{Z}$	Sleep Mode Enable
V_{CCX}	Power (+5V)
V_{CAP}	Capacitor
V_{SS}	Ground

BLOCK DIAGRAM



POWER SUPPLY CONNECTION OPTIONS

The STK12C88 can be powered in three modes. In the normal mode, 5V is supplied to V_{CCX} and a 100µF capacitor is connected to the V_{CAP} terminal, as shown in Figure 1. This datasheet is written assuming that this configuration is used so power supply specifications will refer to V_{CCX}. An optional pull up resistor is shown connected to $\overline{B}$. This is used to signal that the *AutoStore*™ cycle is in progress.

Optionally, V_{CCX} can be tied to ground and +5V applied to V_{CAP} (Figure 2). This is the data protect mode in which the *AutoStore*™ function is disabled. If the STK12C88 is operated in this configuration, references to V_{CCX} should be changed to V_{CAP} throughout this data sheet.

In system power mode (Figure 3) both V_{CCX} and V_{CAP} are connected to the +5V power supply without the 100µF capacitor. In this mode the *AutoStore*™ function of the STK12C88 will operate. However, the user must guarantee that V_{CCX} does not drop below 3.6V during the 10ms store cycle.

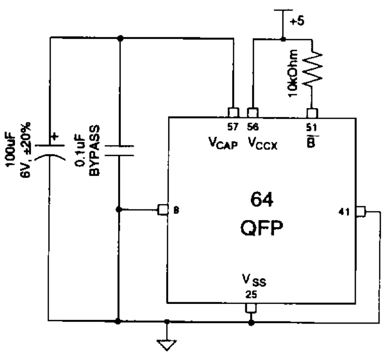


Figure 1: AutoStore™ Mode

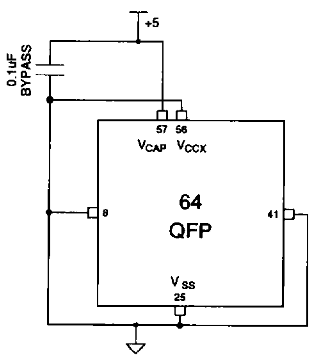


Figure 2: Data Protect Mode

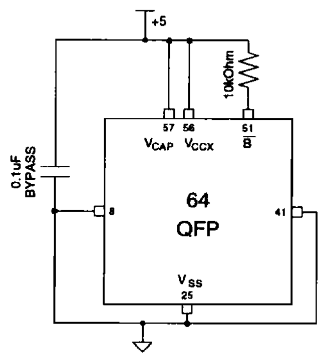


Figure 3: System Power Mode

MULTIPLE CONTROL INPUTS

The STK12C88 provides dual control pins for each of the primary SRAM control functions, chip enable ($\overline{E}$), chip select (S) and write enable ($\overline{W}$). The secondary input carries the suffix "1", e.g. $\overline{E1}$. These multiple inputs are provided for ease of interface to various processors and control chips. They allow such functions as data and program access to the same STK12C88 chip and independent control of the nonvolatile software sequences.

Either control pin from each pair may be used interchangeably. For the sake of brevity, this datasheet references only the non-suffix input per pair but all AC and DC specifications apply to both.

Logical AND and OR chip selection is possible using the chip select and chip enable input pairs. To select the chip, S or S1 must be active HIGH and $\overline{E}$ or $\overline{E1}$ must be active LOW. The Boolean definition is $(\overline{\overline{E} \bullet \overline{E1}}) \bullet (S + S1)$. The SRAM write function is enabled when $\overline{W}$ or $\overline{W1}$ is active low.

An additional input, $\overline{C}$, is provided for more flexible control of the software modes (see software mode selection table). The software sequence can be clocked with $\overline{E}$ or S controlled reads assuming $\overline{C}$ is low, or clocked by $\overline{C}$ if the STK12C88 is already enabled. The Boolean definition of the software clock function is $\overline{\overline{C}} \bullet (\overline{\overline{E} \bullet \overline{E1}}) \bullet (S + S1)$. If the additional control is not needed the $\overline{C}$ pin can be tied to 0V. The software clock, $\overline{C}$, has no effect on SRAM cycles.

HARDWARE MODE SELECTION

$\overline{E}$	S	$\overline{W}$	$\overline{G}$	$\overline{H}$	$\overline{Z}$	$\overline{R}$	MODE	POWER	NOTES
H	X	X	X	H	H	H	Not selected	Standby	a
X	L	X	X	H	H	H	Not selected	Standby	a
L	H	H	L	H	H	H	Read RAM	Active	
L	H	L	X	H	H	H	Write RAM	Active	b
X	X	X	X	L	X	X	Nonvolatile *STORE*	I_{CC2}	c, d
X	X	X	X	X	L	H	*SLEEP* mode	I_{ZZ}	
X	X	X	X	X	X	L	Hardware *RESET / RECALL*	Standby	

SOFTWARE MODE SELECTION

$\overline{E}$	S	$\overline{C}$	$\overline{W}$	$\overline{R}$	$\overline{H}$	$\overline{Z}$	A_{13} - A_0 (hex)	MODE	I/O	NOTES
L	H	H	H	H	H	H	X	Read SRAM Software Disabled	Output data	
L	H	L	H	H	H	H	0E38 31C7 03E0 3C1F 303F 0FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile *STORE*	Output data Output data Output data Output data Output data Output high Z	e, f
L	H	L	H	H	H	H	0E38 31C7 03E0 3C1F 303F 0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile *RECALL*	Output data Output data Output data Output data Output data Output high Z	e, f

Note a: The Boolean expression of chip selection is $(\overline{\overline{E} \bullet \overline{E1}}) \bullet (S + S1)$.
Note b: Assuming the chip is selected, the Boolean expression for write selection is $(\overline{\overline{W} \bullet \overline{W1}})$.
Note c: $\overline{H}$ store operation occurs only if an SRAM write has been done since the last nonvolatile cycle. After the store (if any) completes the part will go into standby mode inhibiting all operations until $\overline{H}$ rises.
Note d: $\overline{R}$ must be held high for t_{HLRL} after $\overline{H}$ otherwise the store cycle may be aborted by the reset request.
Note e: The six consecutive addresses must be in order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.
Note f: While there are 15 addresses on the STK12C88, only the lower 14 are used to control software modes.

ABSOLUTE MAXIMUM RATINGS[g]

Voltage on input relative to V_{SS} . . . . –0.5V to (V_{CCX} + 0.5V)
Voltage on DQ_{0-7} or $\overline{B}$ . . . . –0.5V to (V_{CCX} + 0.5V)
Temperature under bias . . . . –55°C to 125°C
Storage temperature . . . . –65°C to 150°C
Power dissipation 1W
DC output current (1 output at a time, 1s duration) 15mA

Note g: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CCX} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL MAX	INDUSTRIAL MIN	INDUSTRIAL MAX	UNITS	NOTES
I_{CC_1}[h]	Average V_{CCX} Current		155 135 115		170 150 130	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC_2}[i]	Average V_{CCX} Current During STORE		6		7	mA	All inputs Don't Care
I_{CC_3}[h]	Average V_{CCX} Current at t_{AVAV} = 200ns		25		25	mA	$\overline{W} \geq (V_{CCX} - 0.2V)$ All others cycling, CMOS levels
I_{CC_4}[i]	Average V_{CAP} Current During *AutoStore*™ Cycle		4		4	mA	All inputs Don't Care
I_{SB_1}[j]	Average V_{CCX} Current (Standby, Cycling TTL Input Levels)		40 36 33		42 38 35	mA mA mA	t_{AVAV} = 25ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 35ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 45ns, $\overline{E} \geq V_{IH}$
I_{SB_2}[j]	V_{CCX} Standby Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\overline{E} \geq (V_{CCX} - 0.2V)$ or $S \leq 0.2V$ All others $V_{IN} \leq 0.2V$ or $\geq (V_{CCX} - 0.2V)$
I_{ZZ}	V_{CCX} Current During Sleep Mode		10		10	µA	$\overline{Z} \leq 0.2V$; $\overline{R} \geq (V_{CCX} - 0.2V)$; all others Don't Care. Typical current = 2µA
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CCX} = max $V_{IN} = V_{SS}$ to V_{CCX}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CCX} = max $V_{IN} = V_{SS}$ to V_{CCX}, $\overline{E}$ or $\overline{G} \geq V_{IH}$ or $S \leq V_{IL}$
V_{IH}	Input Logic "1" Voltage	2.2	V_{CCX} + .5	2.2	V_{CCX} + .5	V	All inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA
V_{BL}	Logic "0" Voltage on $\overline{B}$ Output		0.4		0.4	V	I_{OUT} = 3mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note h: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note i: I_{CC_2} and I_{CC_4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note j: $\overline{E} \geq V_{IH}$ or $S \leq V_{IL}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input pulse levels . . . . 0V to 3V
Input rise and fall times . . . . ≤ 5ns
Input and output timing reference levels 1.5V
Output load . . . . See Figure 4

CAPACITANCE[k] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output capacitance	7	pF	ΔV = 0 to 3V

Note k: These parameters are guaranteed but not tested.

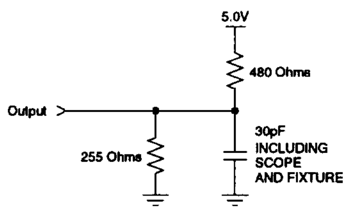


Figure 4: AC Output Loading

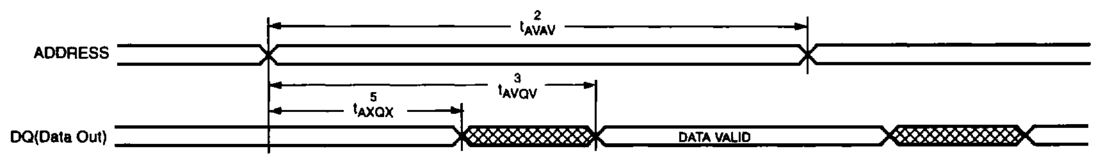
SRAM READ CYCLES #1 & #2

(V_{CCX} = 5.0V ± 10%)

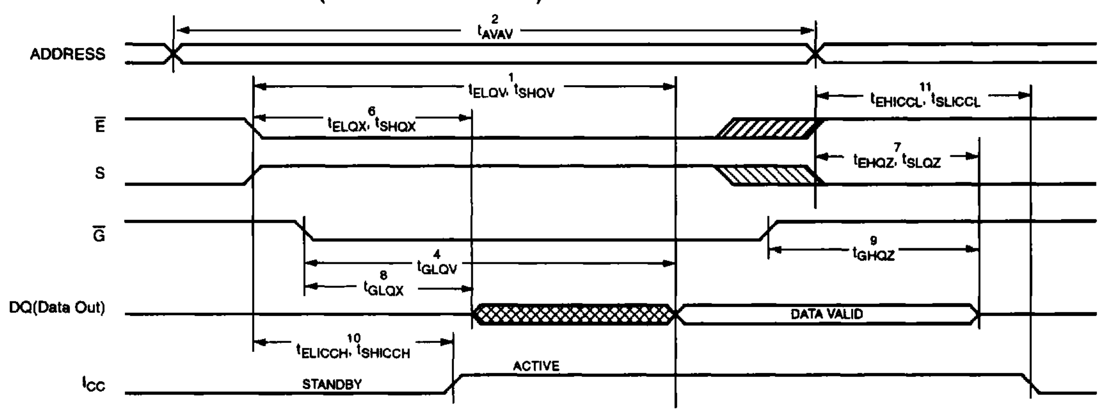
NO.	SYMBOLS #1, #2	SYMBOLS Alt.	PARAMETER	STK12C88-25 MIN	STK12C88-25 MAX	STK12C88-35 MIN	STK12C88-35 MAX	STK12C88-45 MIN	STK12C88-45 MAX	UNITS
1	t_{ELQV}, t_{SHQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}^{l}	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}^{m}	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}^{m}	t_{OH}	Output Hold After Address Change	3		3		3		ns
6	t_{ELQX}, t_{SHQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}, t_{SLQZ}^{n}	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}^{n}	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}, t_{SHICCH}^{k}	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}, $t_{SLICCL}^{j,k}$	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note l: $\overline{W}$, $\overline{H}$, $\overline{R}$ and $\overline{Z}$ must be high during SRAM read and write cycles.
Note m: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low and S high.
Note n: Measured ± 200mV from steady state output voltage

SRAM READ CYCLE #1 (Address Controlled)$^{l,\ m}$



SRAM READ CYCLE #2 ($\overline{E}$ or S controlled)^{l}



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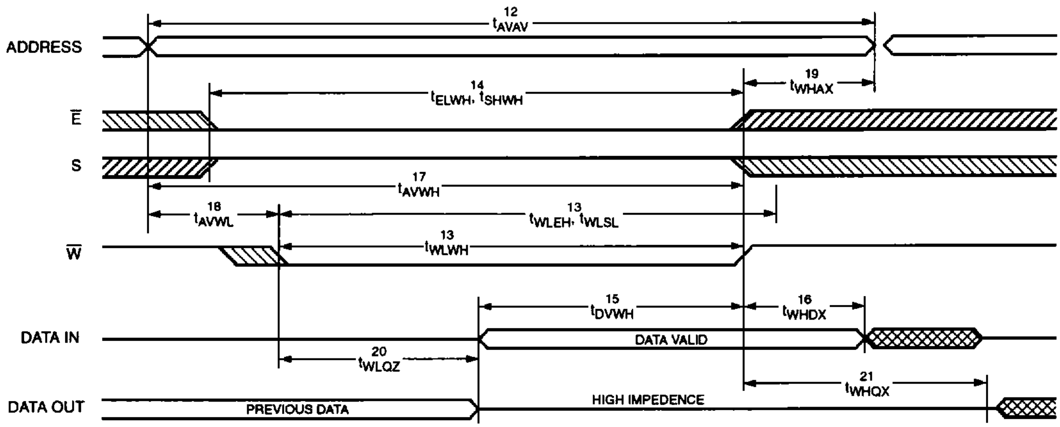
SRAM WRITE CYCLES #1 & #2

(V_{CCX} = 5.0V ± 10%)

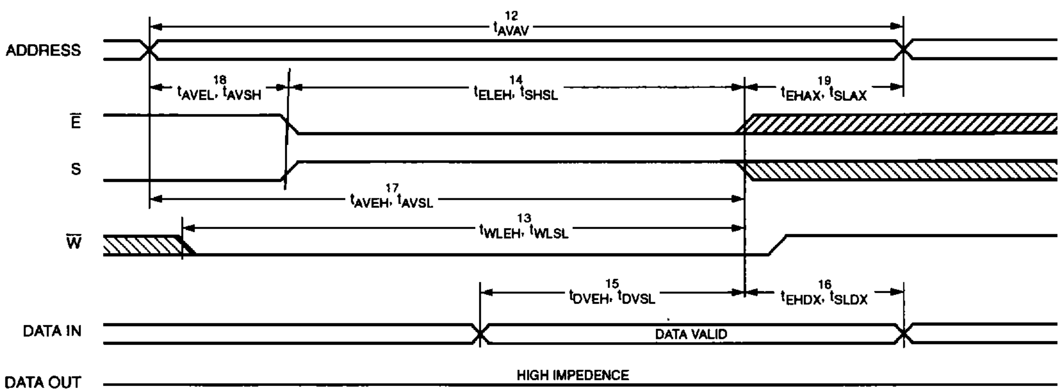
NO.	SYMBOLS			PARAMETER	STK12C88-25		STK12C88-35		STK12C88-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}, t_{WLSL}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}, t_{SHEH}	t_{ELEH}, t_{SHSL}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}, t_{DVSL}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}, t_{SLDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}, t_{AVSL}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}, t_{AVSH}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}, t_{SLAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	t_{WLQZ}[n, o]		t_{WZ}	Write Dnable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		ns

Note o: If $\overline{W}$ is low when either $\overline{E}$ goes low or S goes high, the outputs remain in the high impedance state.
Note p: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} or S must be ≤ V_{IL} during address transitions.

SRAM WRITE CYCLE #1: $\overline{W}$ CONTROLLED[p, l]



SRAM WRITE CYCLE #2: $\overline{E}$, S CONTROLLED[p, l]



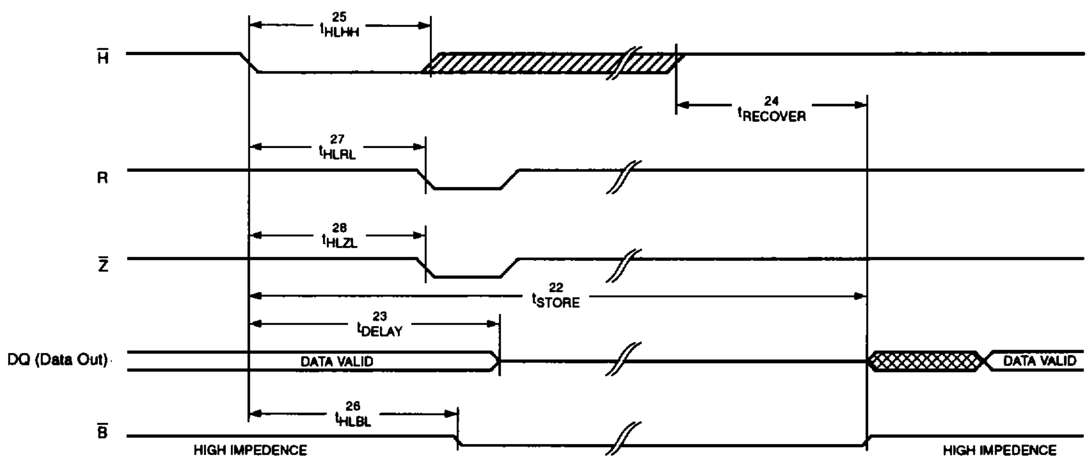
HARDWARE STORE CYCLE

(V_{CCX} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK12C88		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	t_{STORE}	t_{HLBZ}	STORE Cycle Duration		10	ms	n, q
23	t_{DELAY}	t_{HLQZ}	Time allowed to Complete SRAM Cycle	1		µs	n, r
24	$t_{RECOVER}$	t_{HHQX}	Hardware Store High to Inhibit Off		200	ns	q, s
25	t_{HLHH}		Hardware Store Pulse Width	20		ns	
26	t_{HLBL}		Hardware Store Low to Store Busy		300	ns	
27	t_{HLRL}		Hardware Store Set-up to Reset	300		ns	
28	t_{HLZL}		Hardware Store Set-up to Sleep	10		ns	

Note q: $\overline{E}$ and $\overline{G}$ low and S, $\overline{R}$, $\overline{Z}$ and $\overline{H}$ high for output behavior.
Note r: $\overline{E}$ and $\overline{G}$ low and S, $\overline{R}$, and $\overline{Z}$ high for output behavior.
Note s: $t_{RECOVER}$ is only applicable after t_{STORE} is complete.

HARDWARE STORE CYCLE



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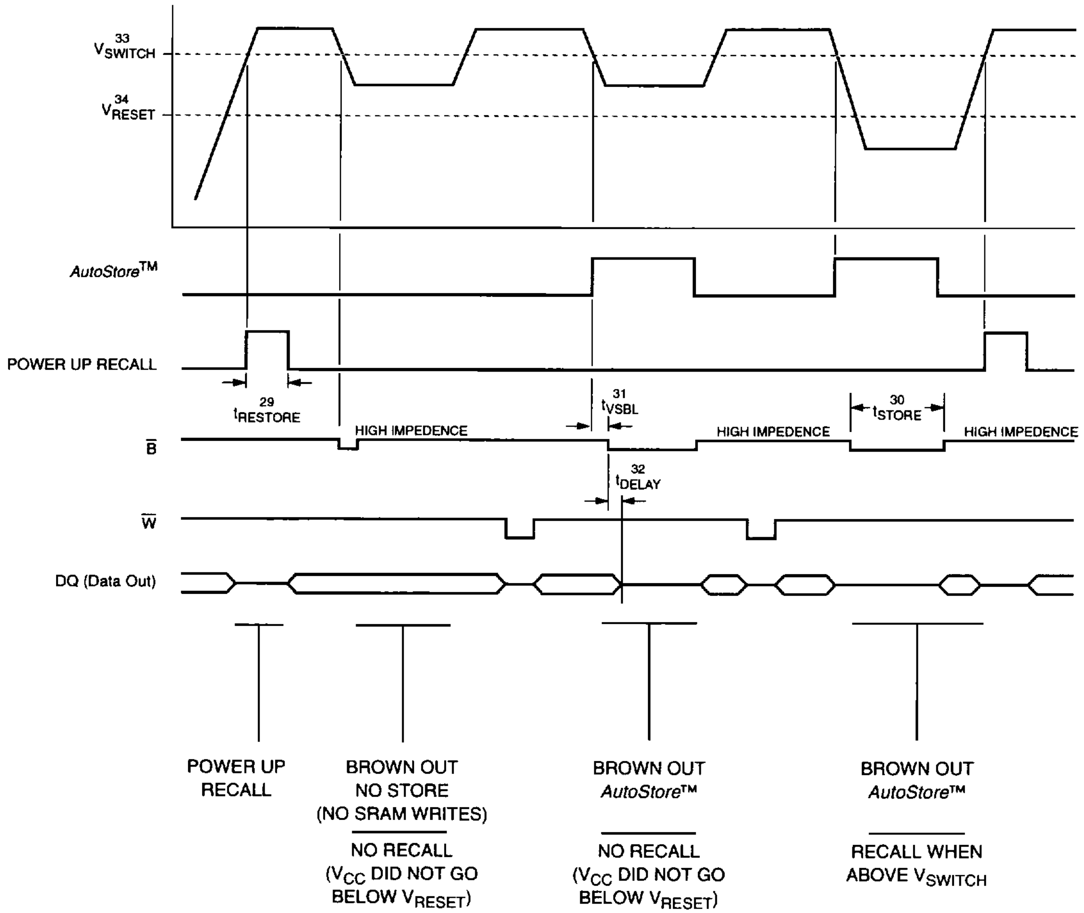
AutoStore™ / POWER UP RECALL

(V_{CCX} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK12C88		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
29	$t_{RESTORE}$		Power Up RECALL Duration		550	μs	t
30	t_{STORE}	t_{BLBZ}	STORE Cycle Duration		10	ms	n, q, u
31	t_{VSBL}		Low Voltage Trigger (V_{SWITCH}) to Busy Low		300	ns	k
32	t_{DELAY}	t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		μs	n, q
33	V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V	
34	V_{RESET}		Low Voltage Reset Level		3.6	V	

Note t: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.
Note u: $\overline{B}$ is asserted low for 1μs when discharging through V_{SWITCH}. If an SRAM Write has not taken place since the last nonvolatile cycle, $\overline{B}$ will be released and no STORE will take place.

AutoStore™ / POWER UP RECALL



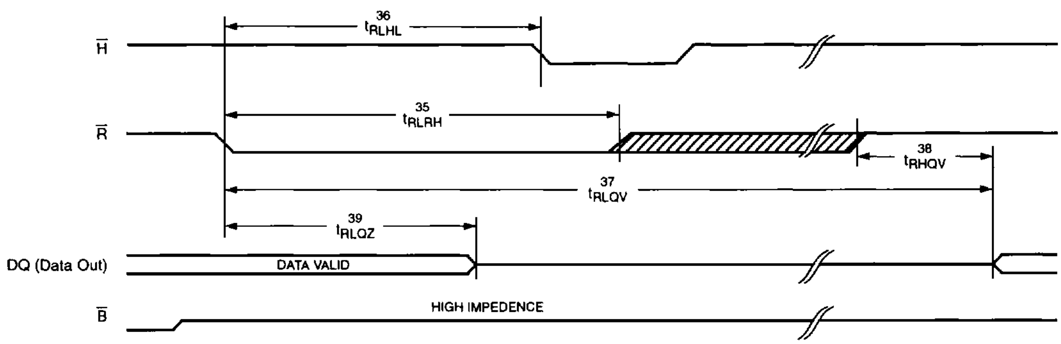
HARDWARE RESET/RECALL & SLEEP CYCLES

(V_{CCX} = 5.0V ± 10%)

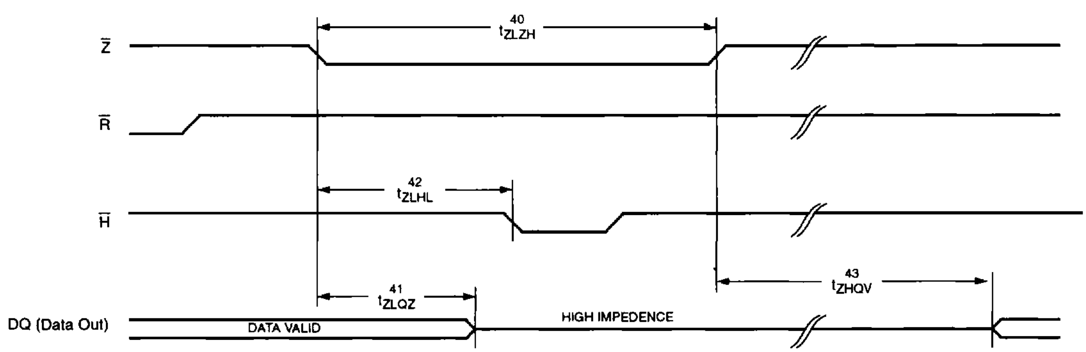
NO.	SYMBOLS	PARAMETER	STK12C88 MIN	STK12C88 MAX	UNITS	NOTES
35	t_{RLRH}	Reset Enable Pulse Width	20		ns	
36	t_{RLHL}	Reset Enable Set-up Time	0		ns	
37	t_{RLQV}	Reset Cycle Duration		550	µs	q
38	t_{RHQV}	Reset Disable to Data Valid		50	ns	q, y
39	t_{RLQZ}	Reset Enable to Output Inactive		100	ns	n, w
40	t_{ZLZH}	Sleep Enable Pulse Width	20		ns	v
41	t_{ZLQZ}	Sleep Enable to Output Inactive		300	ns	n, x
42	t_{ZLHL}	Sleep Enable Set-up Time	10		ns	
43	t_{ZHQV}	Sleep Disable High to Output Valid		550	µs	q

Note v: Sleep current, I_{zz}, only occurs while $\overline{Z} \leq 0.2V$ and $\overline{R} \geq (V_{CCX} - 0.2V)$ after t_{ZLQZ}.
Note w: $\overline{E}$ and $\overline{G}$ low and S, $\overline{Z}$ and $\overline{H}$ high for output behavior.
Note x: $\overline{E}$ and $\overline{G}$ low and S, $\overline{R}$ and $\overline{H}$ high for output behavior.
Note y: t_{RHQV} is only applicable once t_{RLQV} has been satisfied.

HARDWARE RESET/RECALL CYCLE



SLEEP CYCLE



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SOFTWARE CYCLES #1 & #2[aa]

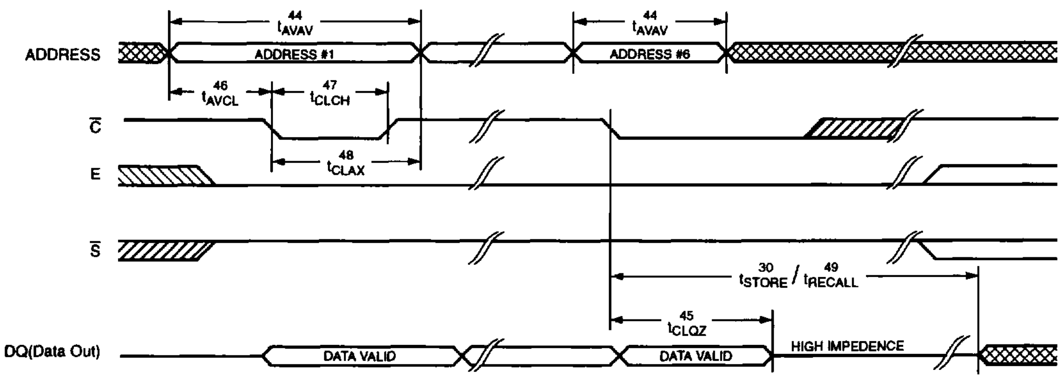
(V_{CCX} = 5.0V ± 10%)

NO.	SYMBOLS #1	SYMBOLS #2	PARAMETER	STK12C88-25 MIN	STK12C88-25 MAX	STK12C88-35 MIN	STK12C88-35 MAX	STK12C88-45 MIN	STK12C88-45 MAX	UNITS	NOTES
44	t_{AVAV}		*STORE/RECALL* Initiation Cycle Time	25		35		45		ns	x
45	t_{CLQZ}	t_{ELQZ}, t_{SHQZ}	End of Sequence to Outputs Inactive		600		600		600	ns	q, z
46	t_{AVCL}	t_{AVEL}, t_{AVSH}	Address Set-up Time	0		0		0		ns	z
47	t_{CLCH}	t_{ELEH}, t_{SHSL}	Clock Pulse Width	20		25		30		ns	z
48	t_{CLAX}	t_{ELAX}, t_{SHAX}	Address Hold Time	15		15		15		ns	z
49	t_{RECALL}		Recall Duration		20		20		20	µs	

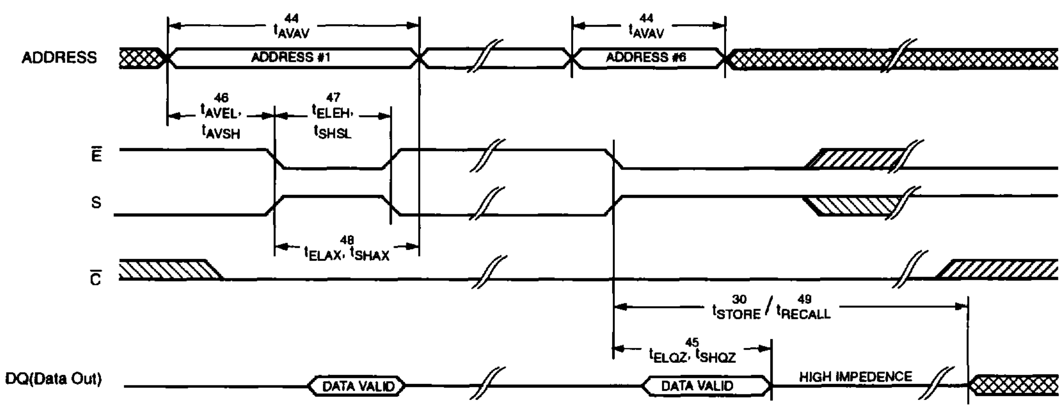
Note z: The software sequence is clocked with $\overline{E}$ or S controlled reads assuming $\overline{C}$ is low, or clocked by $\overline{C}$ if the STK12C88 is already in SRAM read mode. The Boolean definition of the software clock function is $\overline{C} \cdot (\overline{E} \cdot \overline{E1}) \cdot (S + S1)$.

Note aa: The six consecutive addresses must be in the order listed in the SOFTWARE MODE SELECTION Table - (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a STORE cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a RECALL cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE CYCLE #1: $\overline{C}$ CONTROLLED[q,aa]



SOFTWARE CYCLE #2: $\overline{E}$ OR S CONTROLLED[q,aa]



DEVICE OPERATION

The STK12C88 is a versatile memory chip that provides several modes of operation. The STK12C88 can operate as a standard 32K x 8 SRAM. It has a 32K x 8 EEPROM shadow to which the SRAM information can be copied or from which the SRAM cells can be updated. It also offers systems features such as RESET, SLEEP and multiple chip control options. The mode is determined by either the state of the control pins or by execution of software sequences.

NOISE CONSIDERATIONS

The STK12C88 is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1µF connected between DUT V_{CAP} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK12C88 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$, S, $\overline{R}$, $\overline{Z}$ and $\overline{H}$ are high. The address specified on pins $A_{0\text{-}14}$ determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$, S or $\overline{G}$, the outputs will be valid at t_{ELQV}, t_{SHQV} or at t_{GLQV}, whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high or S is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and S, $\overline{R}$, $\overline{Z}$ and $\overline{H}$ are high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high or S goes low at the end of the cycle. The data on the common I/O pins $DQ_{0\text{-}7}$ will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} or t_{DVSL} before the end of an $\overline{E}$ or S, respectively, controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

SOFTWARE NONVOLATILE STORE

The STK12C88 software STORE cycle is initiated by executing sequential READ cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1.	Read address	0E38 (hex)	Valid READ
2.	Read address	31C7 (hex)	Valid READ
3.	Read address	03E0 (hex)	Valid READ
4.	Read address	3C1F (hex)	Valid READ
5.	Read address	303F (hex)	Valid READ
6.	Read address	0FC0 (hex)	Initiate STORE cycle

The software sequence can be clocked with $\overline{E}$ or S controlled reads assuming $\overline{C}$ is low, or clocked by $\overline{C}$ if the STK12C88 is already enabled. The Boolean definition of the software clock function is $\overline{C} \bullet (\overline{\overline{E} \bullet \overline{E1}}) \bullet (S + S1)$.

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE RECALL

A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of READ operations must be performed with the software clock, $\overline{C}$, low:

1.	Read address	0E38 (hex)	Valid READ
2.	Read address	31C7 (hex)	Valid READ
3.	Read address	03E0 (hex)	Valid READ
4.	Read address	3C1F (hex)	Valid READ
5.	Read address	303F (hex)	Valid READ
6.	Read address	0C63 (hex)	Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AutoStore™ OPERATION

During normal operation, the STK12C88 will draw current from V_{CCX} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a STORE operation.

Figure 1 (page 4-2) shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of at least 100µf (± 20%) rated at 6V should be provided for the STK12C88.

If an automatic STORE on power loss is not required then V_{CAP} should be tied directly to the power supply and V_{CCX} should be tied to ground as shown in figure 2 (page 4-2). In this mode, STORE operations may be triggered through software control or the $\overline{H}$ pin. In either event, V_{CAP} must always have a proper bypass capacitor connected to it.

In order to prevent unneeded STORE operations, automatic STOREs as well as those initiated by externally driving $\overline{H}$ low will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place.

POWER UP RECALL

During power up, or after any low power condition ($V_{CAP} < V_{RESET}$) an internal recall request will be latched. When V_{CAP} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

$\overline{H}$ AND $\overline{B}$ OPERATION

The STK12C88 provides the $\overline{H}$ and $\overline{B}$ pins for controlling and acknowledging the STORE operations. The $\overline{H}$ pin is used to request a hardware STORE cycle. When the $\overline{H}$ pin is driven low, the STK12C88 will conditionally initiate a STORE operation after t_{DELAY}; an actual STORE cycle will only begin if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{B}$ pin is an open drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when $\overline{H}$ is driven low or after an *AutoStore™* cycle is requested and $\overline{B}$ is pulled low, are given time to complete before the STORE operation is initiated. After $\overline{H}$ goes low, the STK12C88 will continue SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{B}$ is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{B}$ transitions low will be inhibited.

The $\overline{H}$ and $\overline{B}$ pins can be used to synchronize multiple STK12C88s while using a single larger capacitor. To operate in this mode the $\overline{H}$ and $\overline{B}$ pins should be connected together and to the $\overline{H}$ and $\overline{B}$ pins from the other STK12C88s. An external pull up resistor to +5V is needed since $\overline{B}$ is an open drain pull down. Do not connect this or any other pull-up to the V_{CAP} pin. The V_{CAP} pins from the other STK12C88 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK12C88s detects a power loss and asserts $\overline{B}$, the common $\overline{H}$ pin will cause all parts to request a STORE cycle (a STORE will take place in those STK12C88s that have been written since the last nonvolatile cycle).

During any STORE operation, regardless of how it was initiated, the STK12C88 will continue to drive the $\overline{B}$ pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the STK12C88 will remain disabled until the $\overline{H}$ pin is brought high.

HARDWARE RESET

A hardware RESET cycle is performed when $\overline{R}$ is brought low, interrupting any cycle in progress with the exception of STORE cycles (assuming t_{HLRL} has been satisfied). $\overline{R}$ interfaces directly to the system reset. RESET, which includes an internally-generated RECALL cycle, takes t_{RLQV} to complete as long as $V_{CAP} > V_{SWITCH}$. If $\overline{R}$ is kept low after the RESET is completed all other pins will remain disabled and the current consumption will be I_{SB_2}. Bringing $\overline{R}$ high after the RESET has finished (i.e. $t > t_{RLQV}$) enables the SRAM quickly, within only t_{RHQV}.

Control clock priority is, from highest to lowest: $\overline{R}$; $\overline{Z}$; $\overline{H}$; SRAM control pins. For example, if the $\overline{Z}$ and $\overline{H}$ pins are asserted in unison the part will go to SLEEP rather than STORE.

HARDWARE PROTECT

The STK12C88 offers hardware protection against inadvertent STORE operation during low voltage conditions. When $V_{CAP} < V_{SWITCH}$ all externally initiated STORE operations will be inhibited.

AutoStore™ can be completely disabled by tying V_{CCX} to ground and applying +5V to V_{CAP}, as illustrated in Figure 2. This is the data protect mode; STOREs are only initiated by explicit request using either the software sequence or the $\overline{H}$ pin.

SLEEP MODE

SLEEP mode is initiated by asserting $\overline{Z}$ low. Internally all current loads, including the SRAM array are turned off, reducing current consumption to near zero. This will, of course, cause all SRAM data to be lost. A STORE must be explicitly requested by the user t_{HLZL} before asserting $\overline{Z}$ if the SRAM data is to be preserved. Note that *AutoStore*™ and all other operations with the exception of RESET are disabled when $\overline{Z}$ is low. On the rising edge of $\overline{Z}$ a POWER UP RECALL cycle is initiated lasting t_{ZHQV} so long as $V_{CAP} > V_{SWITCH}$.

LOW AVERAGE ACTIVE POWER

The STK12C88 will draw significantly less current when it is cycled at times longer than 30ns. Figure 5, below, shows the relationship between I_{CC} and READ cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). Figure 6 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled.

The overall average current drawn by the STK12C88 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READ's to WRITE's; 5) the operating temperature; 6) the V_{CCX} level and; 7) I/O loading.

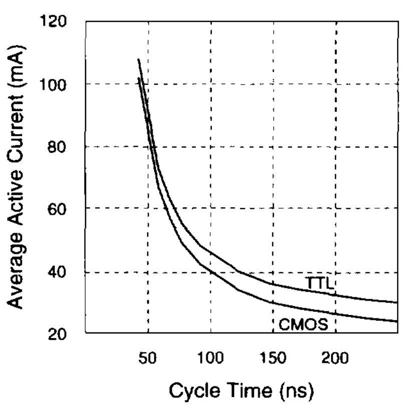


Fig 5: Icc (max) Reads

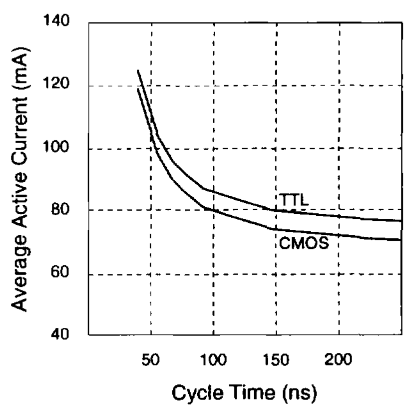


Fig 6: Icc (Max) Writes

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ORDERING INFORMATION

STK12C88 - Q 35 I

Temperature Range
- blank = Commercial (0 to 70 degrees C)
- I = Industrial (–40 to 85 degrees C)

Access Time
- 25 = 25ns
- 35 = 35ns
- 45 = 45ns

Package
- Q = Plastic Quad Flat Pack
- W = Plastic 40-pin 600 mil PDIP