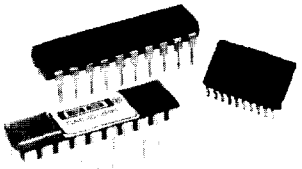
BURR-BROWN®



DAC8012

CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTER With Memory

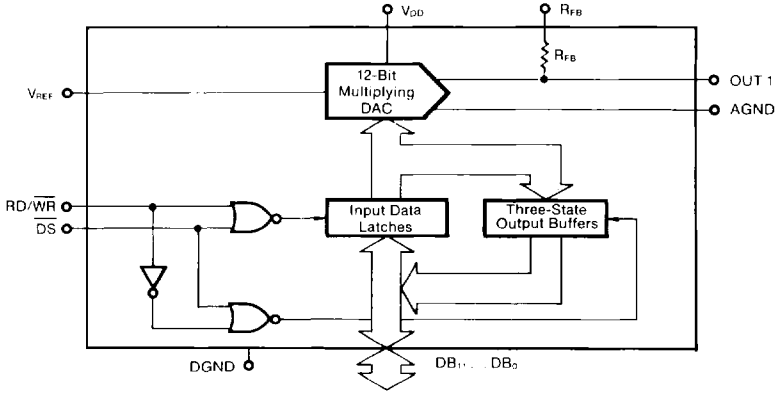
FEATURES

- DATA READBACK CAPABILITY
- FOUR-QUADRANT MULTIPLICATION
- LOW GAIN TC: 2PPM/°C typ
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- SINGLE 5V TO 15V SUPPLY
- LOW OUTPUT LEAKAGE (10nA max)
- LOW OUTPUT CAPACITANCE (70pF max)
- DIRECT REPLACEMENT FOR PMI DAC8012

DESCRIPTION

The DAC8012 is a CMOS, 12-bit, four-quadrant multiplying, digital-to-analog converter with input data latches and 3-state readback capabilities. The input data is loaded into the DAC as a 12-bit data word. The data is loaded into the DAC from the bus when both the data strobe ($\overline{DS}$) and the read/write (RD/$\overline{WR}$) pins are held low. Data may be read back from the DAC by holding $\overline{DS}$ low and (RD/$\overline{WR}$) high. This readback feature enables the user to monitor the state of multiple DACs on a single bi-directional bus.

Laser-trimmed thin-film resistors and excellent CMOS voltage switches provide true 12-bit integral and differential linearity. The device operates on a single +5V to +15V supply and is available in 20-pin side-brazed DIP, 20-pin plastic DIP or a 20-lead plastic SOIC package. Devices are specified over the commercial, industrial, and military temperature ranges and are available with additional reliability screening.



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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{REF} = +10V, $V_{OUT\,1}$ = 0V, AGND = DGND = 0V unless otherwise noted.

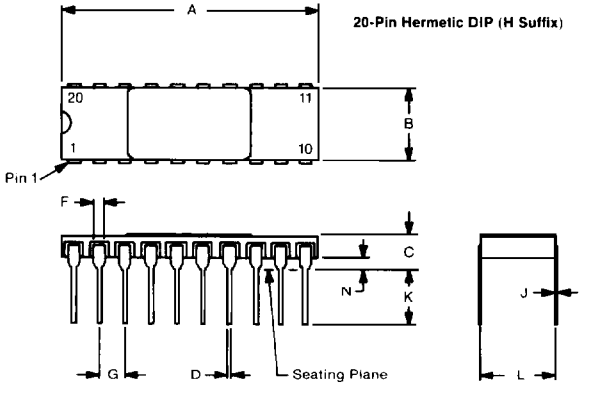
PARAMETER	CONDITIONS	DAC8012B, K, T[1]			DAC8012A, J, S[1]			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{DD} = +5V or +15V								
STATIC ACCURACY								
Resolution		12			12			Bits
Relative Accuracy	T_A = Full temperature range			±1/2			±1	LSB
Differential Nonlinearity[2]	T_A = Full temperature range			+1			±1	LSB
Gain Error[3][4]	T_A = +25°C			±1			±3	LSB
	T_A = Full temperature Range			+2			±4	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature[5][6]				±5			±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD}[5]	T_A = +25°C (ΔV_{DD} = ±5%)			0.002			0.002	%/%
	T_A = Full temperature range (ΔV_{DD} = ±5%)			0.004			0.004	%/%
Output Leakage Current at OUT 1	T_A = +25°C, RD/WR = DS = 0V, all digital inputs = 0V			10			10	nA
	T_A = Full temperature range, S, T versions			200			200	nA
	J, K, A, B versions			25			25	nA
DYNAMIC PERFORMANCE								
Propagation Delay[5][7][8]	T_A = +25°C (OUT 1 Load = 100Ω, C_{EXT} = 13pF)			300			300	ns
Current Settling Time[5][8]	T_A = Full temperature range (to 1/2 LSB) $I_{OUT\,1}$ Load = 100Ω			1			1	µs
Glitch Energy[5], V_{REF} = AGND	T_A = +25°C			400			400	nVs
	T_A = Full temperature range			500			500	nVs
AC Feedthrough at $I_{OUT\,1}$[5][11]	T_A = Full temperature range, V_{REF} = ±10V, f = 10kHz			5			5	mVp-p
REFERENCE INPUT								
Input Resistance (Pin 19 to GND)[12]	T_A = Full temperature range	7	11	15	7	11	15	kΩ
V_{DD} = +5V								
ANALOG OUTPUTS	T_A = Full temperature range							
Output Capacitance[5]	V_{DD} = +5V or +15V							
$C_{OUT\,2}$	DB_0-DB_{11} = 0V, RD/WR = DS = 0V			70			70	pF
$C_{OUT\,1}$	DB_0-DB_{11} = V_{DD}, RD/WR = DS = 0V			150			150	pF
DIGITAL INPUTS								
Input High Voltage	T_A = Full temperature range	2.4			2.4			V
Input Low Voltage	T_A = Full temperature range			0.8			0.8	V
Input Current[9]	T_A = +25°C			1			1	µA
	T_A = Full temperature range			10			10	µA
Input Capacitance[5] DB_0-DB_{11}	T_A = Full temperature range			12			12	pF
RD/WR, DS	T_A = Full temperature range			6			6	pF
DIGITAL OUTPUTS								
Output High Voltage	I_O = 400µA	4.0			4.0			V
Output Low Voltage	I_O = −1.6mA			0.4			0.4	V
Three-State Output Leakage Current				10			10	µA
SWITCHING CHARACTERISTICS[10]	See timing diagram							
Write to Data Stobe Setup Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Write Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Read to Data Strobe Setup Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Read Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Write Mode Data Strobe Width	T_A = −25°C	180			180			ns
	T_A = Full temperature range	250			250			ns
Read Mode Data Strobe Width	T_A = −25°C	220			220			ns
	T_A = Full temperature range	290			290			ns
Data Setup Time	T_A = +25°C	210			210			ns
	T_A = Full temperature range	250			250			ns
Data Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Output Valid Time[5]	T_A = +25°C			300			300	ns
	T_A = Full temperature range			400			400	ns
Output Active Time from Deselection[5]	T_A = +25°C			215			215	ns
	T_A = Full temperature range			375			375	ns
POWER SUPPLY	T_A = Full temperature range							
	(all digital inputs V_{INL} or V_{INH})			2			2	mA
Supply Current	T_A = Full temperature range (all digital inputs 0V or V_{DD})		10	100		10	100	µA

ELECTRICAL CHARACTERISTICS (CONT)

PARAMETER	CONDITIONS	DAC8012B, K, T[1] MIN	DAC8012B, K, T[1] TYP	DAC8012B, K, T[1] MAX	DAC8012A, J, S[1] MIN	DAC8012A, J, S[1] TYP	DAC8012A, J, S[1] MAX	UNITS
	V_{DD} = +15V							
DIGITAL INPUTS								
Input High Voltage	T_A = Full temperature range	13.5			13.5			V
Input Low Voltage	T_A = Full temperature range			1.5			1.5	V
Input Current[9]	T_A = +25°C			1			1	µA
	T_A = Full temperature range			10			10	µA
Input Capacitance[5]: DB_0-DB_{11}	T_A = Full temperature range			12			12	pF
RD/WR, DS	T_A = Full temperature range			10			10	pF
DIGITAL OUTPUTS								
Output High Voltage	I_O = 3mA	13.5			13.5			V
Output Low Voltage	I_O = 3mA			1.5			1.5	V
Three-State Output Leakage Current				10			10	µA
SWITCHING CHARACTERISTICS[10]	See Timing Diagram							
Write to Data Strobe Setup Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Write Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Read to Data Strobe Setup Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Read Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Write Mode Data Strobe Width	T_A = +25°C	100			100			ns
	T_A = Full temperature range	120			120			ns
Read Mode Data Strobe Width	T_A = +25°C	110			110			ns
	T_A = Full temperature range	150			150			ns
Data Setup Time	T_A = +25°C	90			90			ns
	T_A = Full temperature range	120			120			ns
Data Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Output Valid Time	T_A = +25°C			180			180	ns
	T_A = Full temperature range			220			220	ns
Output Active Time for Deselection	T_A = +25°C			180			180	ns
	T_A = Full temperature range			250			250	ns
POWER SUPPLY								
Supply Current	T_A = Full temperature range (all digital inputs V_{INL} or V_{INH})			2			2	mA
	T_A = Full temperature range (all digital inputs 0V or V_{DD})		10	100		10	100	µA

NOTES: (1) T_A = −55°C to +125°C for S, T grades. T_A = −25°C to +85°C for A, B grades. T_A = 0°C to +70°C for J, K grades. (2) 12-bit monotonic over full temperature range. (3) Includes the effects of 5ppm max gain TC. (4) Using internal R_{FB}. DAC register loaded with 1111 1111 1111. (5) **Guaranteed** but **not tested**. (6) Typical value is 2ppm/°C for V_{DD} = +5V. (7) From digital input change to 90% of final analog output. (8) All digital inputs = 0V to V_{DD}; or V_{DD} to 0V. (9) Logic inputs are MOS gates, typical input current (at +25°C) is less than 1nA. (10) Sample tested at +25°C to ensure compliance. (11) Feedthrough can further be reduced by connecting the metal lid on the sidebraze package (Suffix H) to DGND. (12) Resistor T.C. = +100ppm/°C max.

MECHANICAL



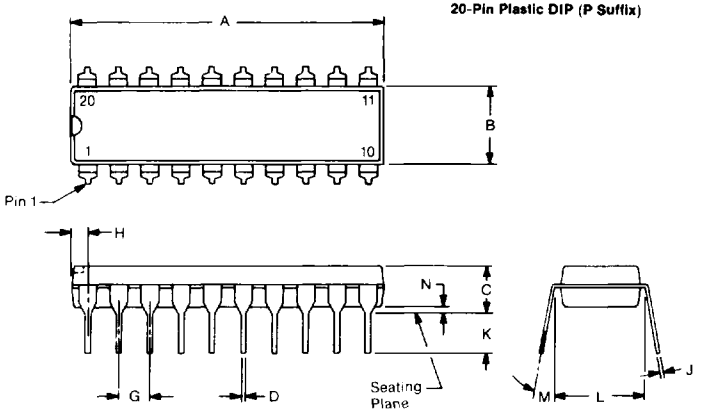
20-Pin Hermetic DIP (H Suffix)

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.990	1.010	25.15	25.65
B	.285	.305	7.24	7.75
C	.100	.140	2.54	3.56
D	.016	.020	0.41	0.51
F	.054 TYP		1.37 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.31
K	.170 BASIC		4.32 BASIC	
L	.300	.320	7.62	8.13
N	.025	.045	0.64	1.14

20-Pin Plastic DIP (P Suffix)

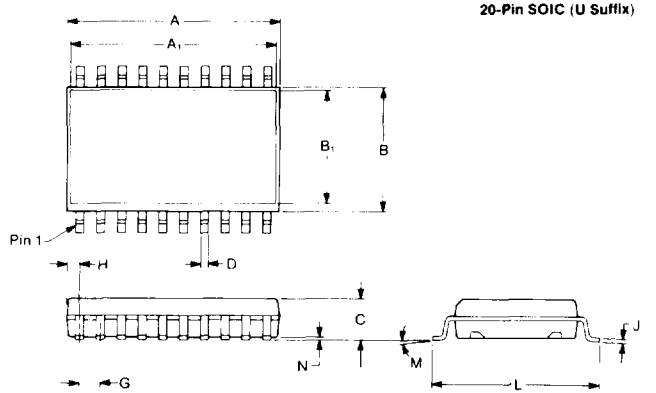


NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.980	1.020	24.89	25.91
B	.240	.280	6.10	7.11
C	—	.210	—	5.33
D	.014	.022	0.36	0.56
G	.100 BASIC		2.54 BASIC	
H	.040	.060	1.02	1.52
J	.008	.015	0.20	0.38
K	.115	.150	2.92	3.81
L	.280	.300	7.11	7.62
M	0°	10°	0°	10°
N	.000	.020	0.00	0.51

20-Pin SOIC (U Suffix)

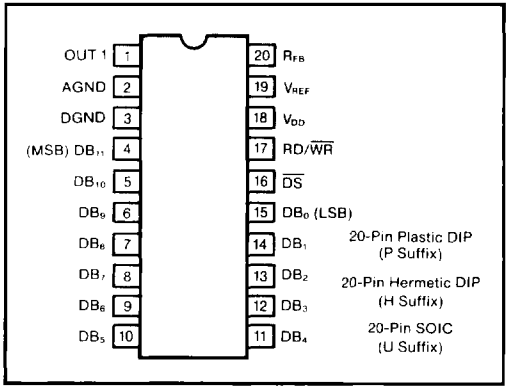


NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.502	.518	12.75	13.16
A_1	.495	.518	12.57	13.16
B	.286	.302	7.26	7.67
B_1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

PIN DESIGNATIONS



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to DGND ..... −0.3V, +17V
Digital Input Voltage to DGND ..... −0.3V, V_{DD}
AGND to DGND ..... −0.3V, V_{DD}
V_{RFB}, V_{REF} to DGND ..... ±25V
$V_{PIN\ 1}$ to DGND ..... −0.3V, V_{DD}
Power Dissipation (any package) to +75°C 450mW
Derates Above +75°C by ..... 6mW/°C
Operating Temperature Range
Military Grades: S, T ..... −55°C to +125°C
Industrial Grades: A, B ..... −25°C to +85°C
Commercial Grades: J, K ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

CAUTION

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
3. The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper antistatic handling procedures.
4. Remove power before inserting or removing units from their sockets.

ORDERING INFORMATION

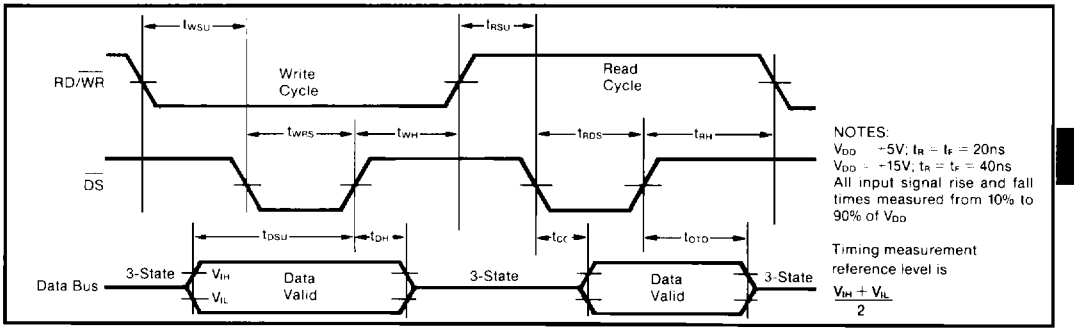
Model	Package	Temperature Range	Relative Accuracy (LSB)	Gain Error (LSB)
DAC8012JP	Plastic DIP	0°C to +70°C	±1	±3
DAC8012KP	Plastic DIP	0°C to +70°C	±1/2	±1
DAC8012JU	Plastic SOIC	0°C to +70°C	±1	±3
DAC8012KU	Plastic SOIC	0°C to +70°C	±1/2	±1
DAC8012AH	Side-brazed ceramic DIP	-25°C to +85°C	±1	±3
DAC8012BH	Side-brazed ceramic DIP	-25°C to +85°C	±1/2	±1
DAC8012SH	Side-brazed ceramic DIP	-55°C to +125°C	±1	±3
DAC8012TH	Side-brazed ceramic DIP	-55°C to +125°C	±1/2	±1

BURN-IN SCREENING OPTION
See text for details.

Model	Package	Temperature Range	Relative Accuracy (LSB)	Burn-In Temp. (160 Hours)[1]
DAC8012JP-BI	Plastic DIP	0°C to +70°C	±1	+85°C
DAC8012KP-BI	Plastic DIP	0°C to +70°C	±1/2	+85°C
DAC8012JU-BI	Plastic SOIC	0°C to +70°C	±1	+85°C
DAC8012KU-BI	Plastic SOIC	0°C to +70°C	±1/2	+85°C
DAC8012AH-BI	Side-brazed ceramic DIP	-25°C to +85°C	±1	+125°C
DAC8012BH-BI	Side-brazed ceramic DIP	-25°C to +85°C	±1/2	+125°C
DAC8012SH-BI	Side-brazed ceramic DIP	-55°C to +125°C	±1	+125°C
DAC8012TH-BI	Side-brazed ceramic DIP	-55°C to +125°C	±1/2	+125°C

NOTE: (1) Or equivalent combination of time and temperature.

TIMING DIAGRAM



BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ESD PROTECTION

The design of the DAC8012 includes ESD protection circuitry for the digital inputs. High voltage static charges are shunted to the supply and ground rails. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket before devices are removed.

DISCUSSION OF SPECIFICATIONS

Relative Accuracy

This term (also known as end point linearity) describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line after zero and full scale have been adjusted.

Differential Nonlinearity

Differential nonlinearity is the deviation from an ideal 1LSB change in the output, for adjacent input code changes. A differential nonlinearity specification of 1LSB guarantees monotonicity.

Gain Error

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC8012 is $-(4095/4096)$ (V_{REF}). Gain error may be adjusted to zero using external trims as shown in the applications section.

Output Leakage Current

The current which appears at OUT_1 with the DAC loaded with all zeros.

Multiplying Feedthrough Error

The AC output error due to capacitive feedthrough from V_{REF} to OUT_1 with the DAC loaded with all zeros. This test is performed using a 10kHz sine wave.

Output Current Settling Time

The time required for the output to settle within ±1/2LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

Propagation Delay

The delay of the internal circuitry is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

Digital-To-Analog Glitch Impulse

The area of the glitch energy measured in nanovolt-seconds. Key contributions to glitch energy are internal circuitry timing differences and charge injected from digital logic. The measurement is performed with V_{REF} = GND.

Monotonicity

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC8012 is guaranteed monotonic to 12 bits.

Power Supply Rejection

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

DIGITAL-TO-ANALOG SECTION

Figure 1 shows a simplified schematic of the digital-to-analog portion of the DAC8012. The current from the V_{REF} pin is switched from $I_{OUT\,1}$ to AGND by the FET switch for that bit. This circuit architecture keeps the resistance at the reference pin constant and equal to R_{LDR}, so the reference could be provided by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V even with V_{DD} = 5V. The R_{LDR} is equal to "R" and is typically 11kΩ.

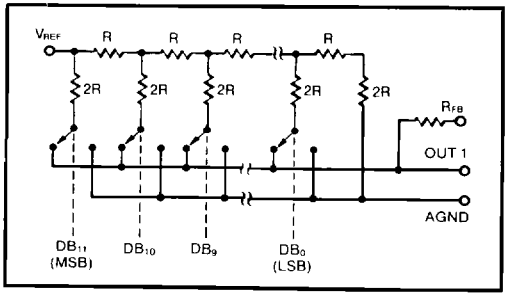


FIGURE 1. Simplified Circuit of the DAC8012.

The output capacitance of the DAC8012 is code dependent and varies from a minimum value (70pF) at code 000_H to a maximum (200pF) at code FFF_H.

DIGITAL SECTION

Figure 2 shows the basic current switch. Figure 3 shows the schematic of the input/output buffers. When the $\overline{DS}$ and the RD/$\overline{WR}$ are held low, the latches are transparent and pass data from the data bus to the DAC. When the $\overline{DS}$ is held low and the RD/$\overline{WR}$ line is held high, the three-state buffer becomes active and the data at the DAC is presented to the digital input/output lines for data readback.

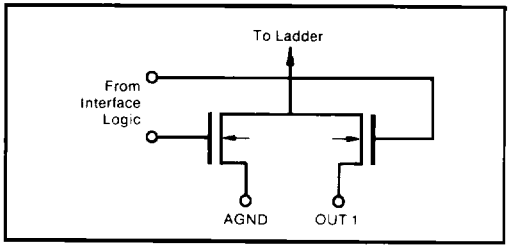


FIGURE 2. N-Channel Current Steering Switch.

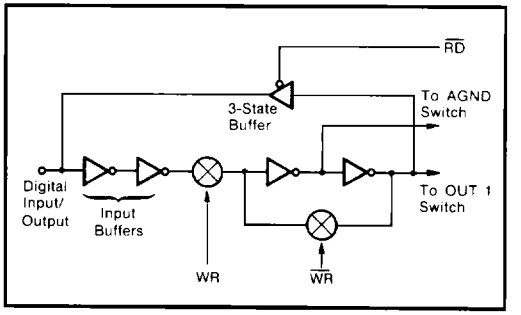


FIGURE 3. Digital Input/Output Structure.

The input buffers are CMOS inverters, designed so that when the DAC8012 is operated from a 5V supply (V_{DD}), the logic threshold is TTL compatible. Being simple CMOS inverters, there is a range of operations where the inverters operate in the linear region and thus draw more supply current than normal. Minimizing the transition time through the linear region and insuring that the digital inputs are operated as close to the rails as possible will minimize the supply drain current.

APPLICATIONS

UNIPOLAR OPERATION

Figure 4 shows the DAC8012 connected for unipolar operation. The high-grade DAC8012 is specified for a 1LSB gain error, so gain adjust is typically not needed.

However, the resistors shown are for adjusting full-scale errors. The value of R_1 should be minimized to reduce the effects of mismatching temperature coefficients between the internal and external resistors. A range of adjustment of 1.5 times the desired range will be adequate. For example, for a DAC8012JP, the gain error is specified to be ±3LSB. A range of adjustment of ±4.5LSB will be adequate. The equation shows a minimum value of 33Ω for the potentiometer.

$$R_1 = (R_{LADDER} / 4096) \times (3 \times \text{Gain Error})$$

The addition of R_1 will cause a negative gain error. To compensate for this error, R_2 must be added. The value of R_2 should be one-third the value of R_1.

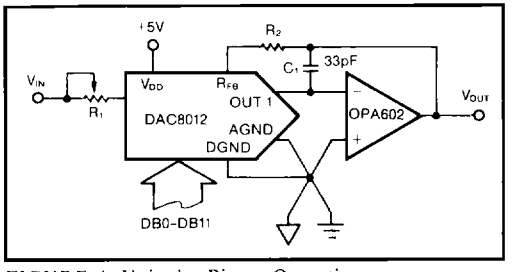


FIGURE 4. Unipolar Binary Operation.

The capacitor across the feedback resistor is used to compensate for the phase shift due to stray capacitances of the circuit board, the DAC output capacitance, and op amp input capacitance. Eliminating this capacitor will result in excessive ringing and an increase in glitch energy in higher speed applications. This capacitor should be as small as possible to minimize settling time.

The circuit of Figure 4 may be used with input voltages up to ±20V as long as the output amplifier is biased to handle the excursions. Table I represents the analog output for four codes into the DAC for Figure 4.

TABLE I. Unipolar Output Code for Figure 4.

Binary Code	Analog Output
MSB ↓ ↓ LSB	
1111 1111 1111	$-V_{IN}$ (4095/4096)
1000 0000 0000	$-V_{IN}$ (2048/4096) = $-1/2V_{IN}$
0000 0000 0001	$-V_{IN}$ (1/4096)
0000 0000 0000	0 Volts

BIPOLAR FOUR-QUADRANT OPERATION

Figure 5 and Table II illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter U_1 on the MSB line converts twos complement input code to offset binary code. The inverter U_1 may be omitted if the inversion is done in software.

R_3, R_4, and R_5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R_3 value to R_4 causes both offset and full-scale error. Mismatch of R_5 to R_4 and R_3 causes full-scale error.

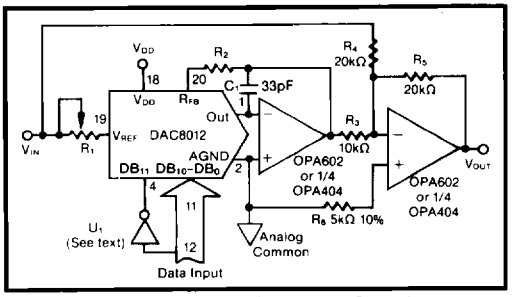


FIGURE 5. Bipolar Operation (Twos Complement Code).

TABLE II. Twos Complement Code Table for Circuit of Figure 5.

Data Input	Analog Output
MSB ↓ ↓ LSB	
0111 1111 1111	$+V_{IN}$ (2047/2048)
0000 0000 0001	$+V_{IN}$ (1/2048)
0000 0000 0000	0 Volts
1111 1111 1111	$-V_{IN}$ (1/2048)
1000 0000 0000	$-V_{IN}$ (2048/2048)

DIGITALLY CONTROLLED GAIN BLOCK

Figure 6 shows a circuit for a digitally controlled gain block. The feedback for the op amp is made up of the FET switch and the R-2R ladder. The input resistor to the gain block is the R_{FB} of the DAC8012. Since the FET switch is in the feedback loop, a "zero code" into the DAC will result in the op amp having no feedback and a saturated op amp output. The DAC8012 readback feature makes the DAC8012 especially good for this configuration when an automatic gain or automatic calibration routine is used. If the logic were set up to calibrate a value via logic external to the processor (successive approximation register), then when the calibration is done, the processor could read the DAC8012 to store away the calibration code.

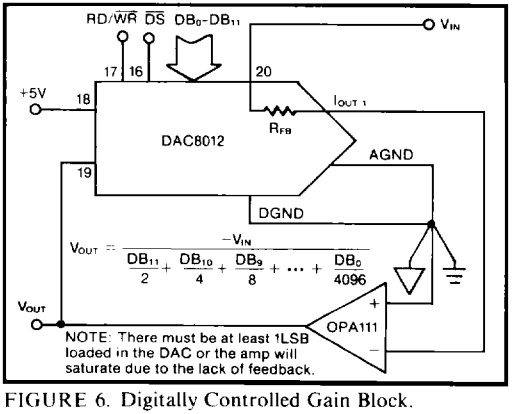


FIGURE 6. Digitally Controlled Gain Block.

APPLICATIONS HINTS

CMOS DACs such as the DAC8012 exhibit a code-dependent output resistance. The effect of this is a code-dependent differential nonlinearity at the amplifier output which depends on the offset voltage V_{OS} of the amplifier. Thus linearity depends upon the potential of I_{OUT} and AGND being exactly equal to each other. Usually the DAC is connected to an external op amp with its noninverting input connected to AGND. The op amp selected should have a low input bias current and low V_{OS} and V_{OS} drift over temperature. The op amp offset voltage should be less than $(25 \times 10^{-6})(V_{REF})$ over operating conditions. Suitable op amps are the Burr-Brown OPA37 and the OPA111 for fixed reference applications and low bandwidth requirements. The OPA37 has low V_{OS} and will not require an offset trim. For wide bandwidth, high slew rate, or fast settling applications, the Burr-Brown OPA602, 1/4 OPA404, or OPA606 are recommended.

Unused digital inputs should be connected to V_{DD} or to DGND. This prevents noise from triggering the high impedance digital input. It is suggested that the unused digital inputs also be given a path to ground or V_{DD} through a 1MΩ resistor to prevent the accumulation of static charge if the PC card is unplugged from the system. In addition, in systems where the AGND to DGND connection is on a backplane, it is recommended that two diodes be connected in inverse parallel between AGND and DGND.

INTERFACING TO MICROPROCESSORS

Figure 7 shows the DAC8012 interfaced to a 16-bit microprocessor. The interface requires only address decoding to select the DAC to be written to or read from.

Figure 8 shows an interface scheme for using the DAC8012 with an 8-bit microprocessor. The data for the first 4 bits are written and latched into the external write latch and the next 8 bits are presented on the bus. The DAC8012 is then instructed to pass the data through the internal DAC latch ($\overline{WR}$ + $\overline{DS}$) and all 8 bits are transferred into the DAC. Reading data back is done in the same manner.

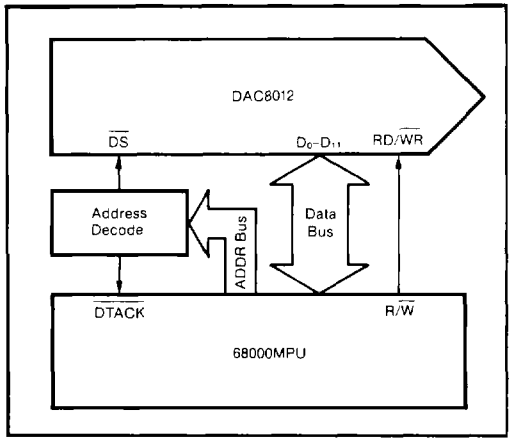


FIGURE 7. 16-Bit Microprocessor to DAC8012 Interface.

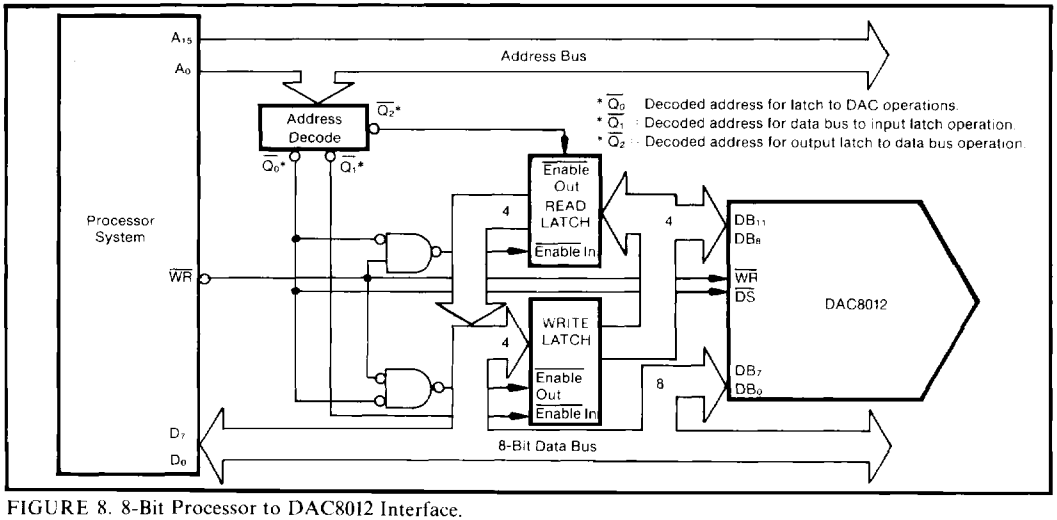


FIGURE 8. 8-Bit Processor to DAC8012 Interface.