DPS832V

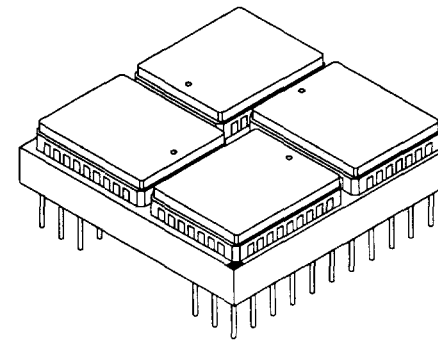
CMOS SRAM VERSAPAC MODULE

DESCRIPTION:

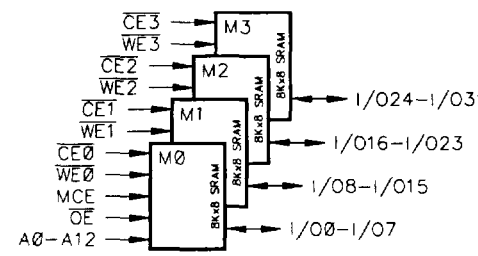
The DPS832V is a 66-pin Pin Grid Array (PGA) consisting of four 8K X 8 SRAM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matching thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

The pins have been arranged around a central 0.6" gap which can accomodate a heat rail. In this central gap is a cavity containing four 0.1µf decoupling capacitors.

Provisions have been made in the pinout for use of 256K and 1MB SRAMs, providing an upgrade path to 128KX32 and to 256KX32 increasing the module density from four to thirty-two times.



FUNCTIONAL BLOCK DIAGRAM



FEATURES:

- Organizations Available:
  32K X 8, 16K X 16 or 8K X 32
- Access Times:
  25, 35, 45, 55, 70, 85, 100, 120, 150ns
- Low Data Retention: 2.0V min.
- Fully Static Operation - No clock or refresh required
- TTL-compatible
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions (EEPROM, EPROM AND MIXED)
- Module Weight is 15 grams
- Module can be built with devices compliant to MIL-STD 883C

PIN NAMES	
A0 - A12	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{CE0}$ - $\overline{CE3}$	Chip Enables
MCE	Master Chip Enable
$\overline{WE0}$ - $\overline{WE3}$	Write Enables
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

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PIN-OUT DIAGRAM

	1	I/08	12	$\overline{WE1}$	23	I/015		34	I/024	45	VDD	56	I/031
	2	I/09	13	$\overline{CE1}$	24	I/014		35	I/025	46	$\overline{CE3}$	57	I/030
	3	I/010	14	VSS	25	I/013		36	I/026	47	$\overline{WE3}$	58	I/029
† *	4	MCE	15	I/011	26	I/012		37	A6	48	I/027	59	I/028
*	5	N.C.	16	A10	27	$\overline{OE}$		38	A7	49	A3	60	A0
*	6	N.C.	17	A11	28	N.C.	(TOP VIEW)	39	N.C.	50	A4	61	A1
*	7	N.C.	18	A12	29	$\overline{WE0}$		40	A8	51	A5	62	A2
	8	N.C.	19	VDD	30	I/07		41	A9	52	$\overline{WE2}$	63	I/023
	9	I/00	20	$\overline{CE0}$	31	I/06		42	I/016	53	$\overline{CE2}$	64	I/022
	10	I/01	21	N.C.	32	I/05		43	I/017	54	VSS	65	I/021
	11	I/02	22	I/03	33	I/04		44	I/018	55	I/019	66	I/020

* Designers should connect these pins to A13, 14, A15 and A16 for future upgrades.
† To enable 8KX8 SRAM pin 4 (MCE) must be held in logic "1" condition.

DPS832V-25, -35, -45, -55, -70, -85 DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-10	+10	-10	+10	-10	+10	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-10	+10	-10	+10	-10	+10	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, MCE = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		400		400		400	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		640		640		640	mA
I_{SB1}	Full Standby Supply Current (CMOS)	V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ V_{SS} + 0.2V		60		80		80	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, MCE = V_{IL}		120		120		120	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

DPS832V-25, -35, -45, -55, -70, -85 DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	TYP.	Max.	Unit
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V, MCE ≤ 0.2V $\overline{CE}$ ≥ V_{DD} -0.2V		0.4	1.2	mA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V, MCE ≤ 0.2V $\overline{CE}$ ≥ V_{DD} -0.2V		1.5	2.4	mA
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	5			ms

DPS832V-100, -120, -150 DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions	Typ.	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-	-10	+10	-10	+10	-10	+10	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-	-10	+10	-10	+10	-10	+10	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, MCE = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	140		180		180		200	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA	200		240		260		280	mA
I_{SB1}	Full Standby Supply Current (CMOS)	V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ V_{SS} +0.2V	4		480		600		1100	µA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, MCE = V_{IL}	2		8		8		8	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA	-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	-	2.4		2.4		2.4		V

DPS832V-100, -120, -150 DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	TYP.	Max.	Unit
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V, MCE ≤ 0.2V $\overline{CE}$ ≥ V_{DD} -0.2V		6	400	µA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V, MCE ≤ 0.2V $\overline{CE}$ ≥ V_{DD} -0.2V		8	440	µA
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	5			ms

RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V
T_A	Operating Temp.	0	+25	+70	°C

ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{CC}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

TRUTH TABLE						
Mode	MCE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	X	H	X	X	HIGH-Z	Standby
Not Selected	L	X	X	X	HIGH-Z	Standby
D_{OUT} Disable	H	L	H	H	HIGH-Z	Active
Read	H	L	H	L	D_{OUT}	Active
Write	H	L	L	H*	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

* If $\overline{OE}$ is LOW during Write, t_{WHZ} must be observed before data is presented to the device.

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	50	pF	V_{IN} = 0V
C_{CE}	Chip Enable	20		
C_{WE}	Write Enable	20		
C_{OE}	Output Enable	50		
$C_{I/O}$	Data Input/Output	20		

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AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns**
Input and Output Timing Reference Levels	1.5V

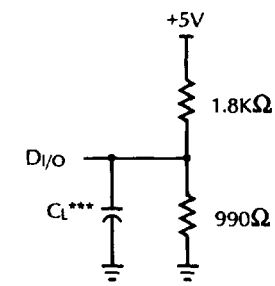
** Transition between 0.8V and 2.2V.

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 2.1mA	-	0.4	V

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OLZ}, t_{OHZ}, t_{OW}, and t_{WHZ}
2	5 pF	t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OLZ}, t_{OHZ}, t_{OW}, and t_{WHZ}

Figure 1. Output Load

*** Including Probe and Jig Capacitance.



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

No.	Symbol	Parameter	-25		-35		-45-		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	25		35		45		55		70		ns
2	t_{AA}	Address Access Time		25		35		45		55		70	ns
3	t_{CO1}	Chip Enable ($\overline{CE}$) to Output Valid		25		35		45		55		70	ns
4	t_{CO2}	Chip Enable (MCE) to Output Valid		25		35		45		55		70	ns
5	t_{OE}	Output Enable to Output Valid		15		25		25		35		40	ns
6	t_{OH}	Output Hold from Address Change	3		3		3		3		3		ns
7	t_{LZ1}	Chip Enable ($\overline{CE}$) to Output in LOW-Z [4, 6]	5		5		5		5		5		ns
8	t_{LZ2}	Chip Enable (MCE) to Output in LOW-Z [4, 6]	5		5		5		5		5		ns
9	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	0		0		5		5		5		ns
10	t_{HZ1}	Chip Enable ($\overline{CE}$) to Output in HIGH-Z [4, 6]		15		15		20		25		30	ns
11	t_{HZ2}	Chip Enable (MCE) to Output in HIGH-Z [4, 6]		15		15		20		25		30	ns
12	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		15		15		20		25		30	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]

No.	Symbol	Parameter	-25		-35		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t_{WC}	Write Cycle Time	25		35		45		55		70		ns
14	t_{AW}	Address Valid to End of Write	20		30		40		50		65		ns
15	t_{CW1}	Chip Enable ($\overline{CE}$) to End of Write	20		30		40		50		65		ns
16	t_{CW2}	Chip Enable (MCE) to End of Write	20		30		40		50		65		ns
17	t_{DW}	Data Valid to End of Write	15		20		25		25		30		ns
18	t_{DH}	Data Hold Time	3		3		3		3		3		ns
19	t_{WP}	Write Pulse Width	20		30		40		50		60		ns
20	t_{AS}	Address Set-up Time*	0		0		0		0		0		ns
21	t_{WR}	Write Recovery Time	0		0		0		0		0		ns
22	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		15		15		20		25		30	ns
23	t_{OW}	Output Active from End of Write	5		5		5		5		5		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

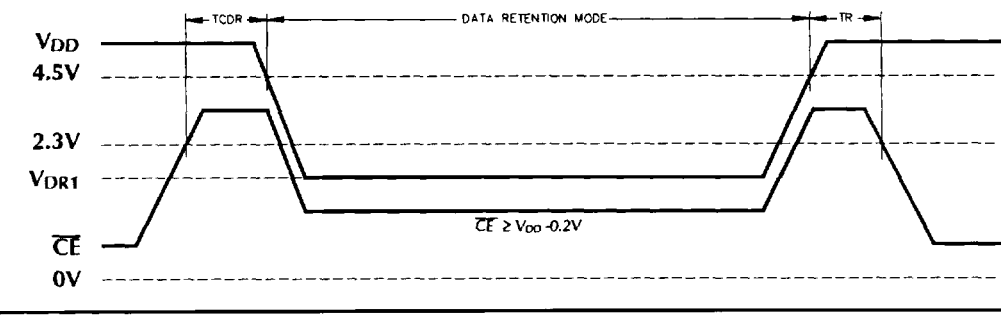
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	85		100		120		150		ns
2	t_{AA}	Address Access Time		85		100		120		150	ns
3	t_{CO1}	Chip Enable ($\overline{CE}$) to Output Valid		85		100		120		150	ns
4	t_{CO2}	Chip Enable (MCE) to Output Valid		85		100		120		150	ns
5	t_{OE}	Output Enable to Output Valid		60		60		60		70	ns
6	t_{OH}	Output Hold from Address Change	5		10		10		10		ns
7	t_{LZ1}	Chip Enable ($\overline{CE}$) to Output in LOW-Z [4, 6]	10		10		10		10		ns
8	t_{LZ2}	Chip Enable (MCE) to Output in LOW-Z [4, 6]	10		10		10		10		ns
9	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns
10	t_{HZ1}	Chip Enable ($\overline{CE}$) to Output in HIGH-Z [4, 6]		30		35		40		50	ns
11	t_{HZ2}	Chip Enable (MCE) to Output in HIGH-Z [4, 6]		30		35		40		50	ns
12	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		30		35		40		50	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]

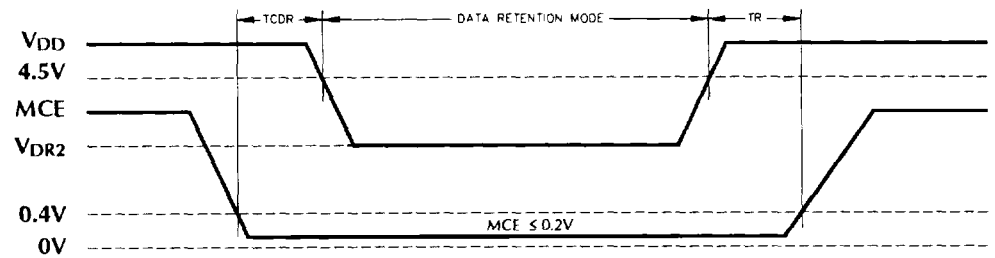
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t_{WC}	Write Cycle Time	85		100		120		150		ns
14	t_{AW}	Address Valid to End of Write	75		90		100		120		ns
15	t_{CW1}	Chip Enable to End of Write	75		90		100		120		ns
16	t_{CW1}	Chip Enable to End of Write	75		90		100		120		ns
17	t_{DW}	Data Valid to End of Write	35		40		50		60		ns
18	t_{DH}	Data Hold Time	0		0		0		0		ns
19	t_{WP}	Write Pulse Width	75		80		90		100		ns
20	t_{AS}	Address Set-up Time*	0		0		0		0		ns
21	t_{WR}	Write Recovery Time	0		0		0		0		ns
22	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		35		35		40		50	ns
23	t_{OW}	Output Active from End of Write	5		5		5		5		ns

* Valid for both Read and Write Cycles.

DATA RETENTION WAVEFORM: $\overline{CE}$ Controlled.



DATA RETENTION WAVEFORM: MCE Controlled.



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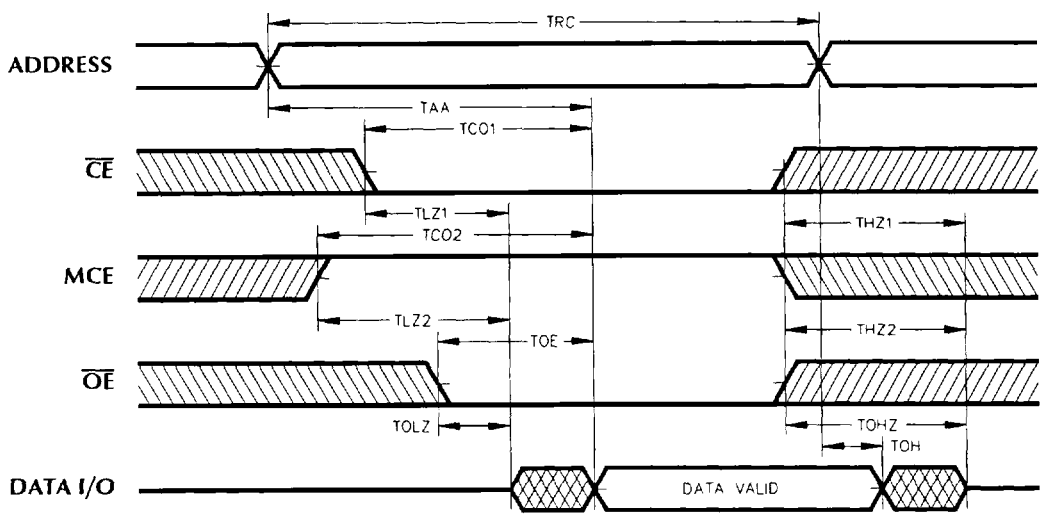
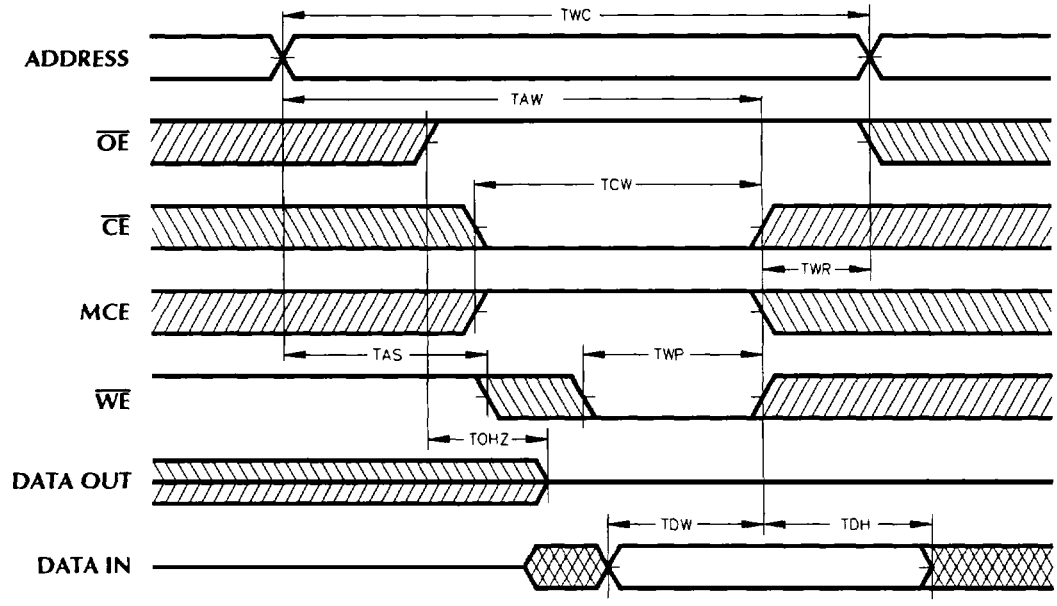
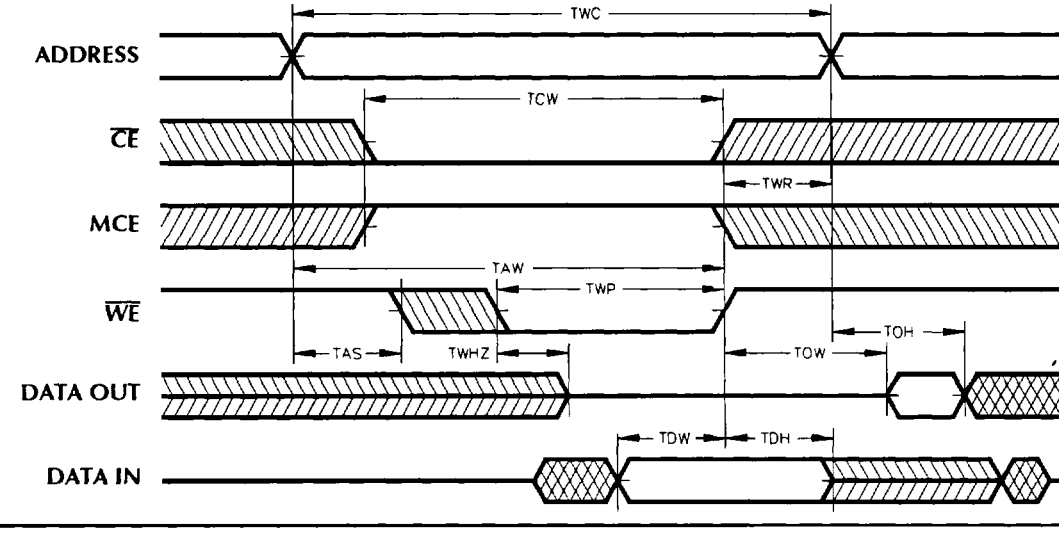
READ CYCLE



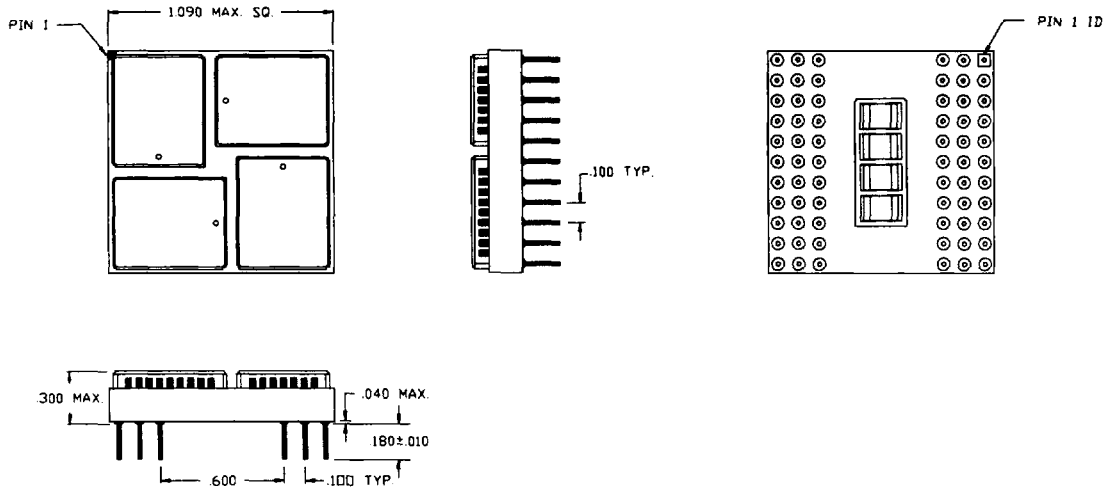
WRITE CYCLE 1: $\overline{WE}$ Controlled, $\overline{OE}$ Clocked.



WRITE CYCLE 2: $\overline{CE}$ Controlled, $\overline{OE}$ is LOW.



MECHANICAL DRAWING



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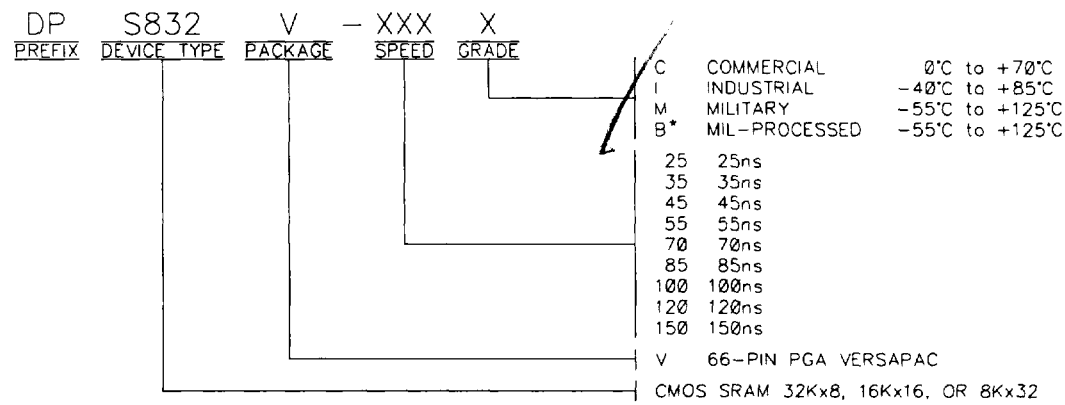
NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min.= -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

ORDERING INFORMATION



* B grade modules can be constructed with 883 devices.

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