

Features

- Specified for +3V, +5V, or ±5V Applications
- Large Input Common Mode Range $0V < V_{CM} < V_S - 1.2V$
- Output Swings to Ground Without Saturating
- -3 dB Bandwidth = 125 MHz
- ±0.1 dB Bandwidth = 30 MHz
- Low Supply Current = 5 mA (per amplifier)
- Slew Rate = 275 V/μsec
- Low Offset Voltage = 2 mV max
- Output Current = ±100 mA
- High Open Loop Gain = 80 dB
- Differential Gain = 0.05%
- Differential Phase = 0.05°

Applications

- Video Amplifier
- PCMCIA Applications
- A/D Driver
- Line Driver
- Portable Computers
- High Speed Communications
- RGB Printer, FAX, Scanner
- Broadcast Equipment
- Active Filtering

Ordering Information

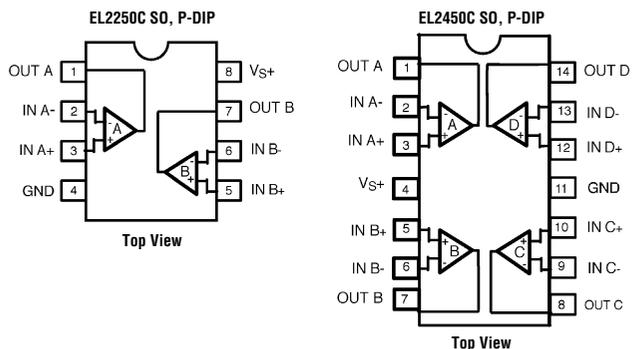
Part No.	Temp. Range	Package	Outline #
EL2250CN	-40°C to +85°C	8 Pin PDIP	MDP0031
EL2250CS	-40°C to +85°C	8 Pin SOIC	MDP0027
EL2450CN	-40°C to +85°C	14 Pin PDIP	MDP0031
EL2450CS	-40°C to +85°C	14 Pin SOIC	MDP0027

General Description

The EL2250C/EL2450C are part of a family of the electronics industries fastest single supply op amps available. Prior single supply op amps have generally been limited to bandwidths and slew rates 1/4 that of the EL2250C/EL2450C. The 125 MHz bandwidth, 275 V/μsec slew rate, and 0.05%/0.05° differential gain/differential phase makes this part ideal for single or dual supply video speed applications. With its voltage feedback architecture, this amplifier can accept reactive feedback networks, allowing them to be used in analog filtering applications. The inputs can sense signals below the bottom supply rail and as high as 1.2V below the top rail. Connecting the load resistor to ground and operating from a single supply, the outputs swing completely to ground without saturating. The outputs can also drive to within 1.2V of the top rail. The EL2250C/EL2450C will output ±100 mA and will operate with single supply voltages as low as 2.7V, making them ideal for portable, low power applications.

The EL2250C/EL2450C are available in plastic DIP and SOIC packages in industry standard pin outs. Both parts operate over the industrial temperature range of -40°C to +85°C, and are part of a family of single supply op amps. For single amplifier applications, see the EL2150C/EL2157C. For dual and triple amplifiers with power down and output voltage clamps, see the EL2257C/EL2357C.

Connection Diagrams



EL2250C/EL2450C

125 MHz Single Supply Dual/Quad Op Amps

Absolute Maximum Ratings (T_A = 25 °C)

Supply Voltage between V _S and GND	+12.6V	Power Dissipation	See Curves
Input Voltage (IN+, IN-)	GND-0.3V, V _S +0.3V	Storage Temperature Range	-65°C to +150°C
Differential Input Voltage	±6V	Ambient Operating Temperature Range	-40°C to +85°C
Maximum Output Current	90 mA	Operating Junction Temperature	150°C
Output Short Circuit Duration	(Note 1)		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore T_J = T_C = T_A.

Test Level	Test Procedure
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I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T _A = 25°C and QA sample tested at T _A = 25°C, T _{MAX} and T _{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T _A = 25°C for information purposes only.

DC Electrical Characteristics

V_S=+5V, GND=0V, T_A=25°C, V_{CM}=1.5V, V_{OUT}=1.5V, unless otherwise specified.

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
V _{OS}	Offset Voltage		-4		4	I	mV
TCV _{OS}	Offset Voltage Temperature Coefficient	Measured from T _{min} to T _{max}		10		V	μV/°C
I _B	Input Bias Current	V _{IN} =0V		-5.5	-10	I	μA
I _{OS}	Input Offset Current	V _{IN} =0V	-750	150	750	I	nA
TCI _{OS}	Input Bias Current Temperature Coefficient	Measured from T _{min} to T _{max}		50		V	nA/°C
PSRR	Power Supply Rejection Ratio	V _S =+2.7V to +12V	55	70		I	dB
CMRR	Common Mode Rejection Ratio	V _{CM} =0V to +3.8V V _{CM} =0V to +3.0V	55	65 70		I	dB
CMIR	Common Mode Input Range		0		V _S -1.2	I	V
R _{IN}	Input Resistance	Common Mode	1	2		I	MΩ
C _{IN}	Input Capacitance	SOIC Package PDIP Package		1 1.5		V	pF
R _{OUT}	Output Resistance	A _V =+1		40		V	mΩ
I _S	Supply Current (per amplifier)	V _S =+12V		5	6.5	I	mA
PSOR	Power Supply Operating Range		2.7		12.0	I	V

EL2250C/EL2450C

125 MHz Single Supply Dual/Quad Op Amps

EL2250C/EL2450C

DC Electrical Characteristics

$V_S=+5V$, $GND=0V$, $T_A=25^\circ C$, $V_{CM}=+1.5V$, $V_{OUT}=+1.5V$, unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
AVOL	Open Loop Gain	$V_S=+12V$, $V_{OUT}=+2V$ to $+9V$, $R_L=1\text{ k}\Omega$ to GND	65	80		I	dB
		$V_{OUT}=+1.5V$ to $+3.5V$, $R_L=1\text{ k}\Omega$ to GND		70		V	dB
		$V_{OUT}=+1.5V$ to $+3.5V$, $R_L=150\Omega$ to GND		60		V	dB
V _{OP}	Positive Output Voltage Swing	$V_S=+12V$, $A_V=+1$, $R_L=1\text{ k}\Omega$ to 0V		10.8		V	V
		$V_S=+12V$, $A_V=+1$, $R_L=150\Omega$ to 0V	9.6	10.0		I	V
		$V_S=\pm 5V$, $A_V=+1$, $R_L=1\text{ k}\Omega$ to 0V		4.0		V	V
		$V_S=\pm 5V$, $A_V=+1$, $R_L=150\Omega$ to 0V	3.4	3.8		I	V
		$V_S=+3V$, $A_V=+1$, $R_L=150\Omega$ to 0V	1.8	1.95		I	V
V _{ON}	Negative Output Voltage Swing	$V_S=+12V$, $A_V=+1$, $R_L=150\Omega$ to 0V		5.5	8	I	mV
		$V_S=\pm 5V$, $A_V=+1$, $R_L=1\text{ k}\Omega$ to 0V		-4.0		V	V
		$V_S=\pm 5V$, $A_V=+1$, $R_L=150\Omega$ to 0V		-3.7	-3.4	I	V
I _{OUT}	Output Current ^[1]	$V_S=\pm 5V$, $A_V=+1$, $R_L=10\Omega$ to 0V	± 75	± 100		I	mA
		$V_S=\pm 5V$, $A_V=+1$, $R_L=50\Omega$ to 0V $\pm 60VmA$					

1. Internal short circuit protection circuitry has been built into the EL2250C/EL2450C. See the Applications section.

Closed Loop AC Electrical Characteristics

$V_S=+5V$, $GND=0V$, $T_A=25^\circ C$, $V_{CM}=+1.5V$, $V_{OUT}=+1.5V$, $A_V=+1$, $R_F=0\Omega$, $R_L=150\Omega$ to GND pin, unless otherwise specified^[1]

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
BW	-3dB Bandwidth ($V_{OUT}=400\text{ mVp-p}$)	$V_S=+5V$, $A_V=+1$, $R_F=0\Omega$		125		V	MHz
		$V_S=+5V$, $A_V=-1$, $R_F=500\Omega$		60		V	MHz
		$V_S=+5V$, $A_V=+2$, $R_F=500\Omega$		60		V	MHz
		$V_S=+5V$, $A_V=+10$, $R_F=500\Omega$		6		V	MHz
		$V_S=+12V$, $A_V=+1$, $R_F=0\Omega$		150		V	MHz
		$V_S=+3V$, $A_V=+1$, $R_F=0\Omega$		100		V	MHz
BW	$\pm 0.1\text{ dB}$ Bandwidth ($V_{OUT}=400\text{ mVp-p}$)	$V_S=+12V$, $A_V=+1$, $R_F=0\Omega$		25		V	MHz
		$V_S=+5V$, $A_V=+1$, $R_F=0\Omega$		30		V	MHz
		$V_S=+3V$, $A_V=+1$, $R_F=0\Omega$		20		V	MHz
GBWP	Gain Bandwidth Product	$V_S=+12V$, @ $A_V=+10$		60		V	MHz
PM	Phase Margin	$R_L=1\text{ k}\Omega$, $C_L=6\text{ pF}$		55		V	°
SR	Slew Rate	$V_S=+10V$, $R_L=150\Omega$, $V_{OUT}=0V$ to $+6V$	200	275		I	V/ μs
		$V_S=+5V$, $R_L=150\Omega$, $V_{OUT}=0V$ to $+3V$		300		V	V/ μs
t _r , t _f	Rise Time, Fall Time	$\pm 0.1V$ Step		2.8		V	ns
OS	Overshoot	$\pm 0.1V$ Step		10		V	%
t _{PD}	Propagation Delay	$\pm 0.1V$ Step		3.2		V	ns
t _S	0.1% Settling Time	$V_S=\pm 5V$, $R_L=500\Omega$, $A_V=+1$, $V_{OUT}=\pm 3V$		40		V	ns
	0.01% Settling Time	$V_S=\pm 5V$, $R_L=500\Omega$, $A_V=+1$, $V_{OUT}=\pm 3V$		75		V	ns
dG	Differential Gain ^[2]	$A_V=+2$, $R_F=1\text{ k}\Omega$		0.05		V	%

EL2250C/EL2450C

125 MHz Single Supply Dual/Quad Op Amps

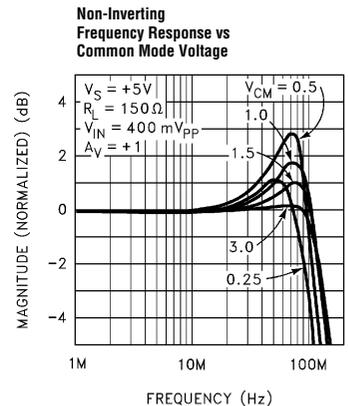
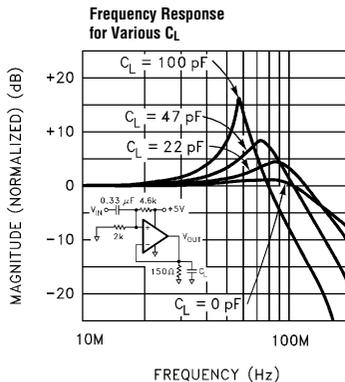
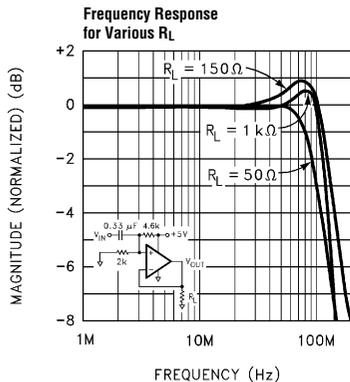
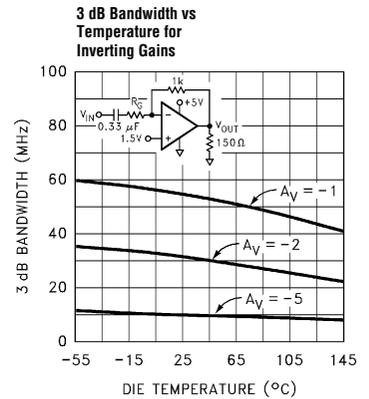
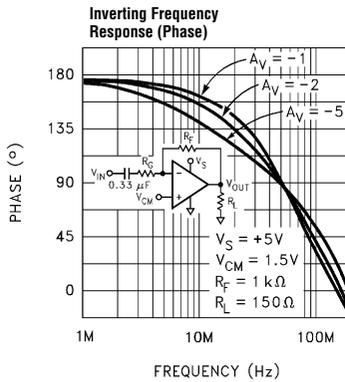
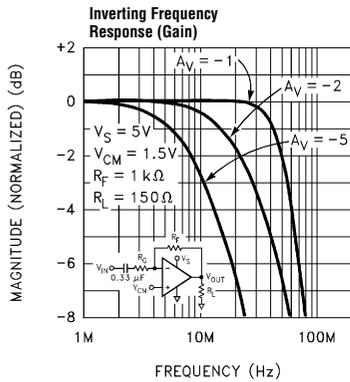
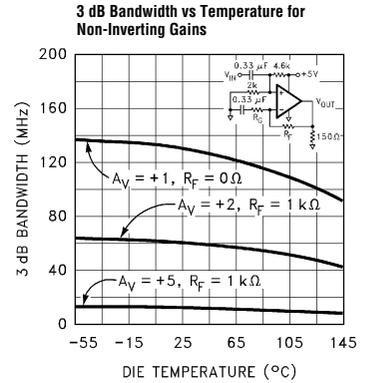
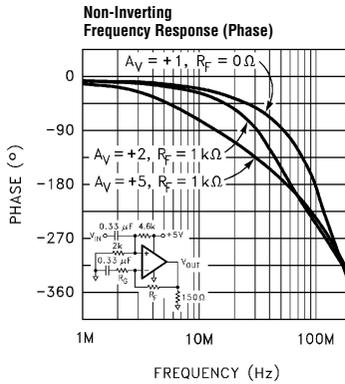
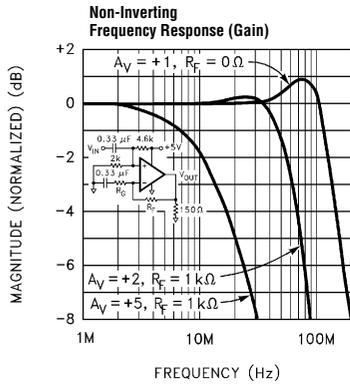
Closed Loop AC Electrical Characteristics

$V_S=+5V$, $GND=0V$, $T_A=25^\circ C$, $V_{CM}=+1.5V$, $V_{OUT}=+1.5V$, $A_V=+1$, $R_F=0\Omega$, $R_L=150\Omega$ to GND pin, unless otherwise specified^[1]

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
dP	Differential Phase ^[2]	$A_V=+2$, $R_F=1\text{ k}\Omega$		0.05		V	°
e _N	Input Noise Voltage	f=10 kHz		48		V	nV/ $\sqrt{\text{Hz}}$
i _N	Input Noise Current	f=10 kHz		1.25		V	pA/ $\sqrt{\text{Hz}}$

1. All AC tests are performed on a “warmed up” part, except slew rate, which is pulse tested.
2. Standard NTSC signal = 286 mVp-p, f=3.58 MHz, as V_{IN} is swept from 0.6V to 1.314V. R_L is DC coupled.

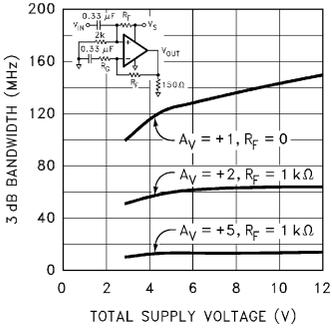
Typical Performance Curves



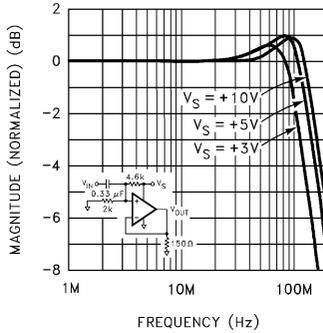
EL2250C/EL2450C

125 MHz Single Supply Dual/Quad Op Amps

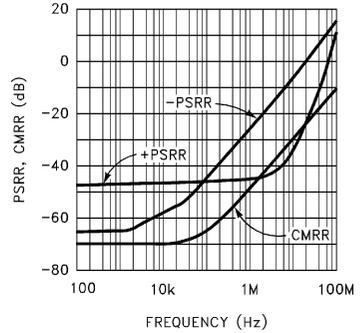
3 dB Bandwidth vs Supply Voltage for Non-Inverting Gains



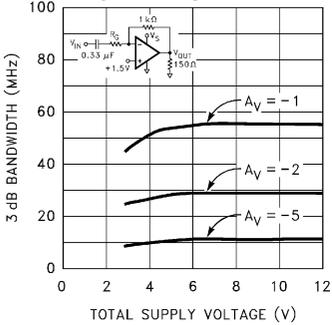
Frequency Response for Various Supply Voltages, Av = +1



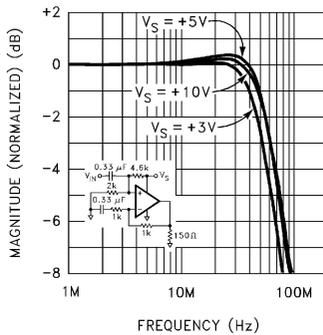
PSRR and CMRR vs Frequency



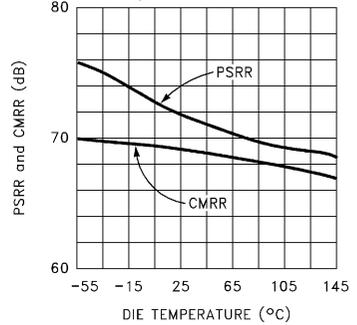
3 dB Bandwidth vs Supply Voltage for Inverting Gains



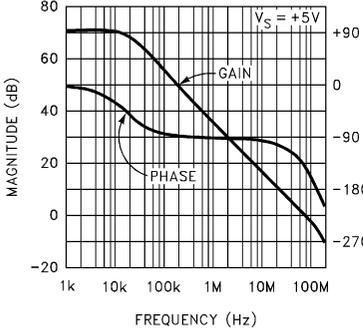
Frequency Response for Various Supply Voltages, Av = +2



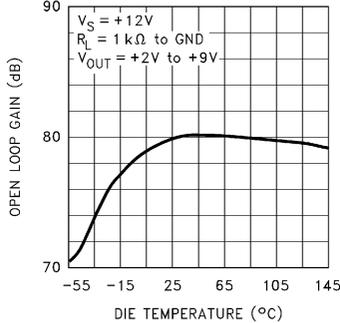
PSRR and CMRR vs Die Temperature



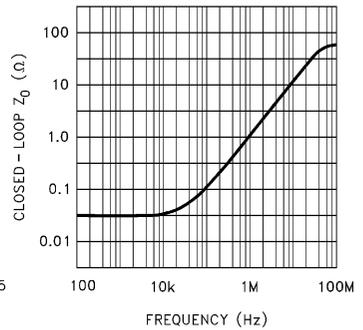
Open Loop Gain and Phase vs Frequency



Open Loop Voltage Gain vs Die Temperature

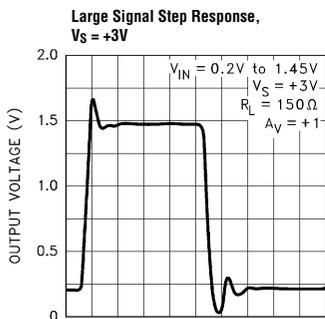


Closed Loop Output Impedance vs Frequency

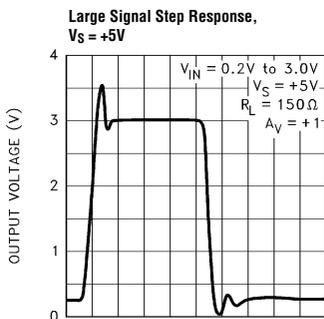


EL2250C/EL2450C

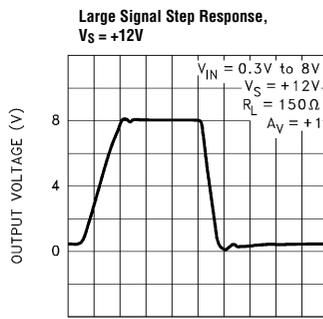
125 MHz Single Supply Dual/Quad Op Amps



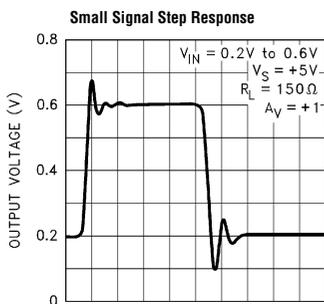
TIME 20 ns/div



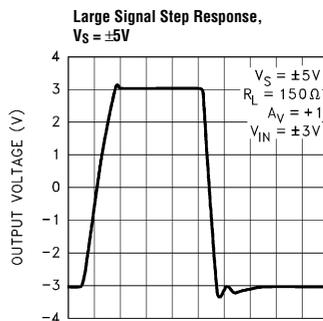
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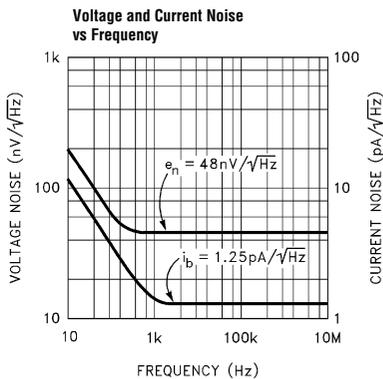
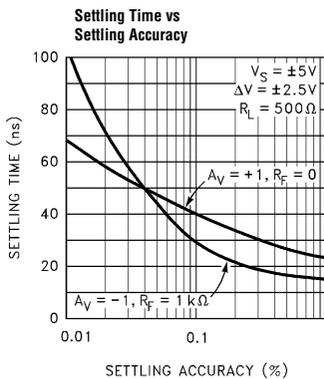
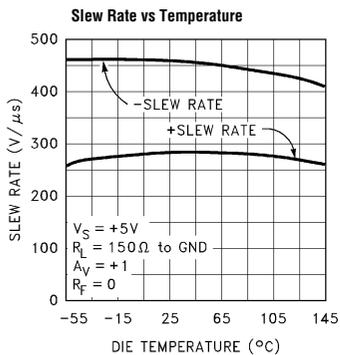
TIME 20 ns/div



TIME 20 ns/div



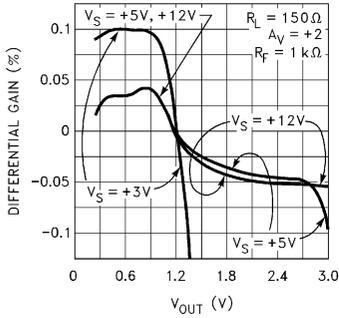
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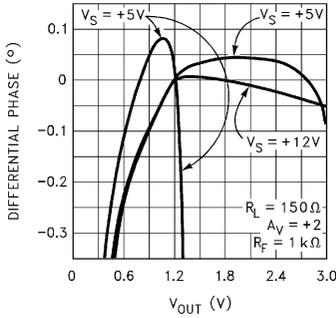
EL2250C/EL2450C

125 MHz Single Supply Dual/Quad Op Amps

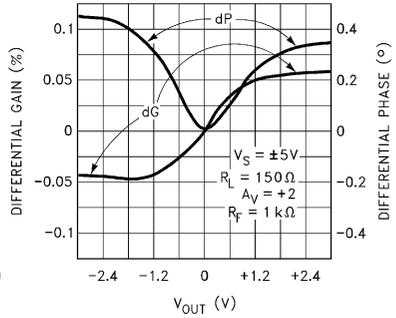
Differential Gain for Single Supply Operation



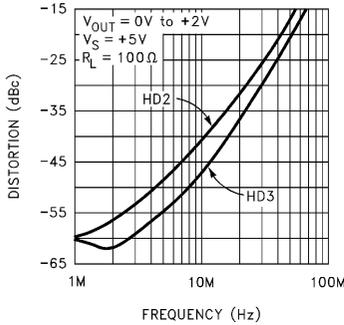
Differential Phase for Single Supply Operation



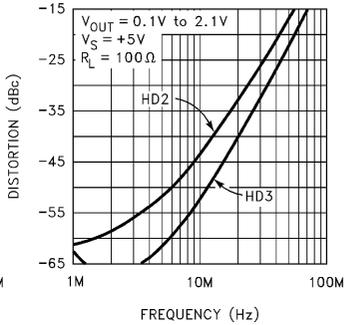
Differential Gain and Phase for Dual Supply Operation



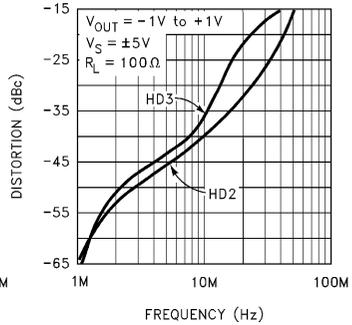
2nd and 3rd Harmonic Distortion vs Frequency



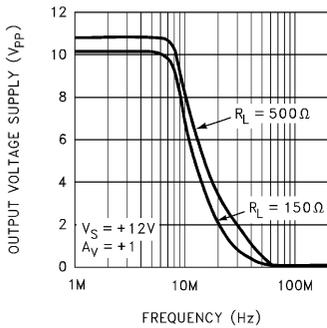
2nd and 3rd Harmonic Distortion vs Frequency



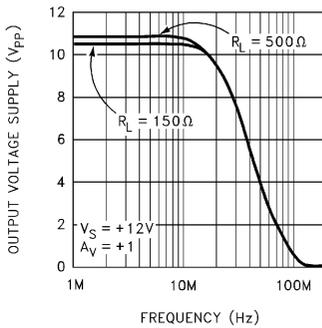
2nd and 3rd Harmonic Distortion vs Frequency



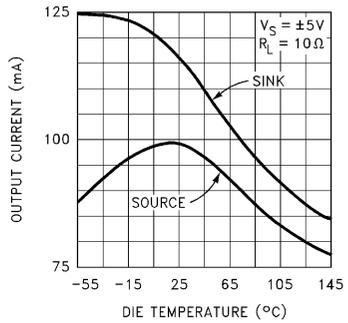
Output Voltage Swing vs Frequency for THD < 0.1%



Output Voltage Swing vs Frequency for Unlimited Distortion

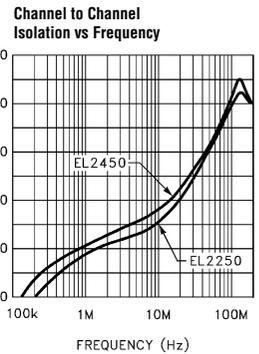
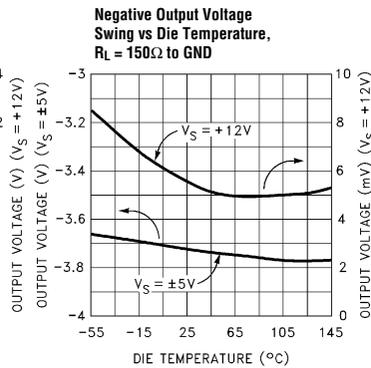
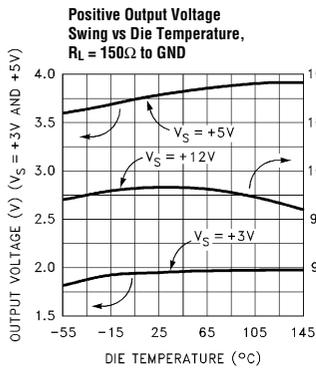
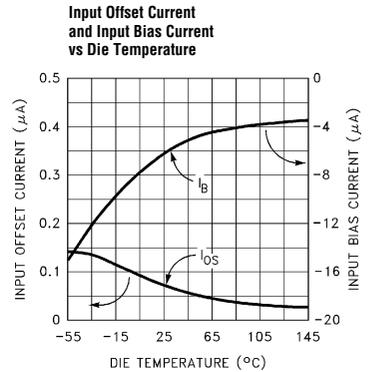
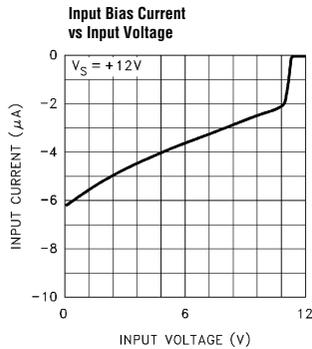
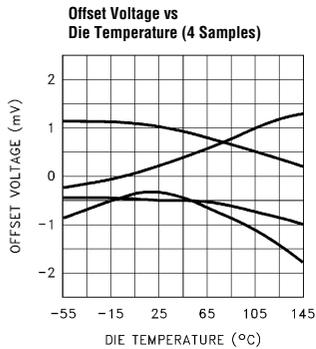
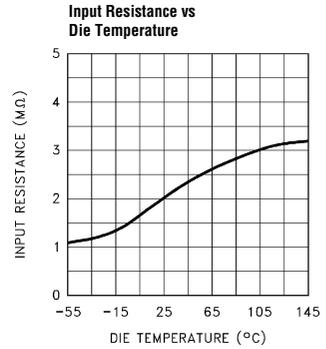
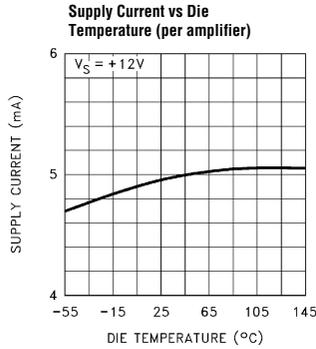
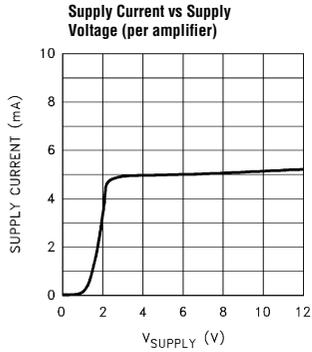


Output Current vs Die Temperature



EL2250C/EL2450C

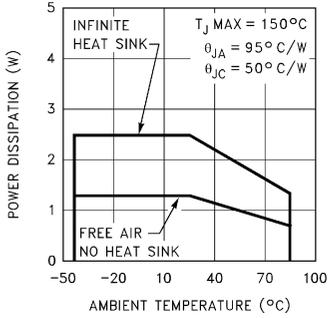
125 MHz Single Supply Dual/Quad Op Amps



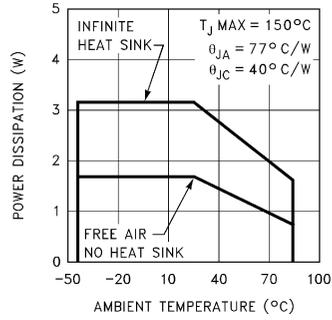
EL2250C/EL2450C

125 MHz Single Supply Dual/Quad Op Amps

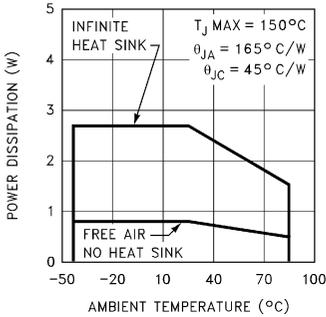
8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



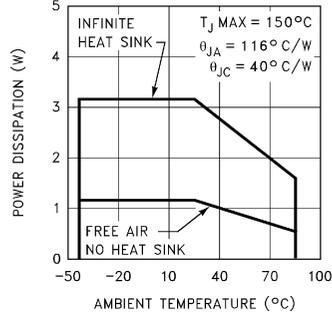
14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



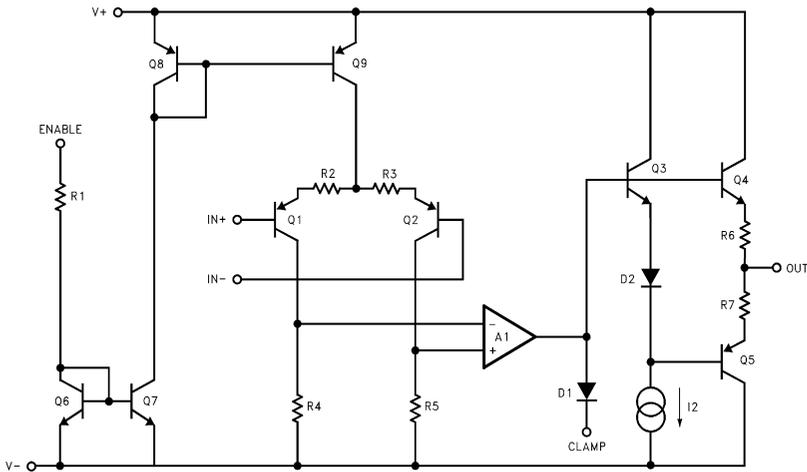
8-Lead Plastic SOIC
Maximum Power Dissipation
vs Ambient Temperature



14-Lead Plastic SOIC
Maximum Power Dissipation
vs Ambient Temperature



Simplified Schematic



EL2250C/EL2450C

125 MHz Single Supply Dual/Quad Op Amps

Applications Information

Product Description

The EL2250C/EL2450C are part of a family of the industries fastest single supply operational amplifiers. Connected in voltage follower mode, their -3dB bandwidth is 125 MHz while maintaining a 275 V/ μ s slew rate. With an input and output common mode range that includes ground, these amplifiers were optimized for single supply operation, but will also accept dual supplies. They operate on a total supply voltage range as low as +2.7V or up to +12V. This makes them ideal for +3V applications, especially portable computers.

While many amplifiers claim to operate on a single supply, and some can sense ground at their inputs, most fail to truly drive their outputs to ground. If they do succeed in driving to ground, the amplifier often saturates, causing distortion and recovery delays. However, special circuitry built into the EL2250C/EL2450C allows the output to follow the input signal to ground without recovery delays.

Power Supply Bypassing And Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor has been shown to work well when placed at each supply pin. For single supply operation, where the GND pin is connected to the ground plane, a single 4.7 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor across the V_{S+} and GND pins will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction should be used. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Supply Voltage Range and Single-Supply Operation

The EL2250C/EL2450C have been designed to operate with supply voltages having a span of greater than 2.7V, and less than 12V. In practical terms, this means that the EL2250C/EL2450C will operate on dual supplies ranging from ± 1.35 V to ± 6 V. With a single-supply, the EL2250C/EL2450C will operate from +2.7V to +12V. Performance has been optimized for a single +5V supply.

Pins 8 and 4 are the power supply pins on the EL2250C. The positive power supply is connected to pin 8. When used in single supply mode, pin 4 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4.

Pins 4 and 11 are the power supply pins on the EL2450C. The positive power supply is connected to pin 4. When used in single supply mode, pin 11 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 11.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2250C/EL2450C have an input voltage range that includes the negative supply and extends to within 1.2V of the positive supply. So, for example, on a single +5V supply, the EL2250C/EL2450C have an input range which spans from 0V to 3.8V.

The output range of the EL2250C/EL2450C is also quite large. It includes the negative rail, and extends to within 1V of the top supply rail with a 1 k Ω load. On a +5V supply, the output is therefore capable of swinging from 0V to +4V. On split supplies, the output will swing ± 4 V. If the load resistor is tied to the negative rail and split supplies are used, the output range is extended to the negative rail.

Choice Of Feedback Resistor, R_F

The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value which should not be exceeded for

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optimum performance. If a large value of R_F must be used, a small capacitor in the few picofarad range in parallel with R_F can help to reduce this ringing and peaking at the expense of reducing the bandwidth.

As far as the output stage of the amplifier is concerned, $R_F + R_G$ appear in parallel with R_L for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F has a minimum value that should not be exceeded for optimum performance.

For $A_V = +1$, $R_F = 0 \Omega$ is optimum. For $A_V = -1$ or +2 (noise gain of 2), optimum response is obtained with R_F between 500 Ω and 1 k Ω . For $A_V = -4$ or +5 (noise gain of 5), keep R_F between 2 k Ω and 10 k Ω .

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This can be difficult when driving a standard video load of 150 Ω , because of the change in output current with DC level. Differential Gain and Differential Phase for the EL2250C/EL2450C are specified with the black level of the output video signal set to +1.2V. This allows ample room for the sync pulse even in a gain of +2 configuration. This results in dG and dP specifications of 0.05% and 0.05° while driving 150 Ω at a gain of +2. Setting the black level to other values, although acceptable, will compromise peak performance. For example, looking at the single supply dG and dP curves for $R_L=150 \Omega$, if the output black level clamp is reduced from 1.2V to 0.6V dG/dP will increase from 0.05%/0.05° to 0.08%/0.25°. Note that in a gain of +2 configuration, this is the lowest black level allowed such that the sync tip doesn't go below 0V.

If your application requires that the output goes to ground, then the output stage of the EL2250C/EL2450C, like all other single supply op amps, requires an external pull down resistor tied to ground. As mentioned above, the current flowing through this resistor becomes the DC bias current for the output stage NPN transistor. As this current approaches zero, the NPN turns off, and dG and dP will increase. This becomes more critical as the load resistor is increased in value. While driving a light load, such as 1 k Ω , if the input black level is kept above 1.25V, dG and dP are a respectable 0.03% and 0.03°.

For other biasing conditions see the Differential Gain and Differential Phase vs. Input Voltage curves.

Output Drive Capability

In spite of their moderately low 5 mA of supply current, the EL2250C/EL2450C are capable of providing ± 100 mA of output current into a 10 Ω load, or ± 60 mA into 50 Ω . With this large output current capability, a 50 Ω load can be driven to $\pm 3V$ with $V_S = \pm 5V$, making it an excellent choice for driving isolation transformers in telecommunications applications.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will de-couple the EL2250C/EL2450C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5 Ω and 50 Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output.

Video Sync Pulse Remover Application

All CMOS Analog to Digital Converters (A/Ds) have a parasitic latch-up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off.

Figure 1 shows a unity gain connected amplifier A of an EL2250C. Figure 2 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.

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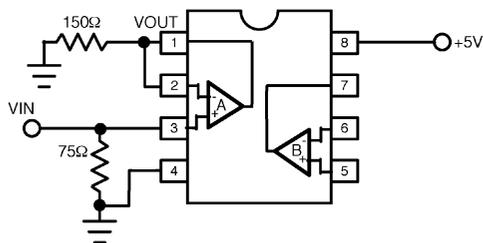


Figure 1.

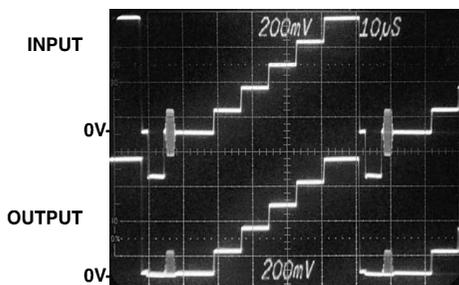


Figure 2.

Short Circuit Current Limit

The EL2250C/EL2450C have internal short circuit protection circuitry that protect it in the event of its output being shorted to either supply rail. This limit is set to around 100 mA nominally and reduces with increasing junction temperature. It is intended to handle temporary shorts. If an output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ± 90 mA. A heat sink may be required to keep the junction temperature below absolute maximum when an output is shorted indefinitely.

Power Dissipation

With the high output drive capability of the EL2250C/EL2450C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if power-supply voltages, load

conditions, or package type need to be modified for the EL2250C/EL2450C to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to [1]:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

where:

T_{JMAX} = Maximum Junction Temperature

T_{AMAX} = Maximum Ambient Temperature

θ_{JA} = Thermal Resistance of the Package

PD_{MAX} = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or [2]

$$PD_{MAX} = N \times \left(V_S \times I_{SMAX} + (V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L} \right)$$

where:

N = Number of amplifiers

V_S = Total Supply Voltage

I_{SMAX} = Maximum Supply Current per amplifier

V_{OUT} = Maximum Output Voltage of the Application

R_L = Load Resistance tied to Ground

If we set the two PD_{MAX} equations, [1] & [2], equal to each other, and solve for V_S , we can get a family of curves for various loads and output voltages according to [3]:

$$V_S = \frac{R_L \times (T_{JMAX} - T_{AMAX}) + (V_{OUT})}{N \times \theta_{JA} + (IS \times R_L) + V_{OUT}}$$

Figures 3 through 6 below show total single supply voltage V_S vs. R_L for various output voltage swings for the PDIP and SOIC packages. The curves assume WORST CASE conditions of $T_A = +85^\circ\text{C}$ and $I_S = 6.5$ mA per amplifier.

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EL2250C Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (PDIP Package)

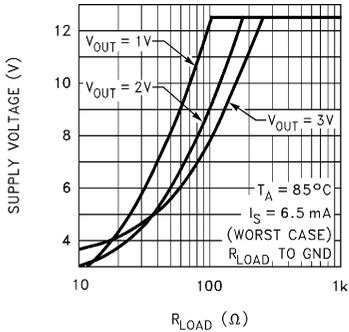


Figure 3.

EL2450C Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (PDIP Package)

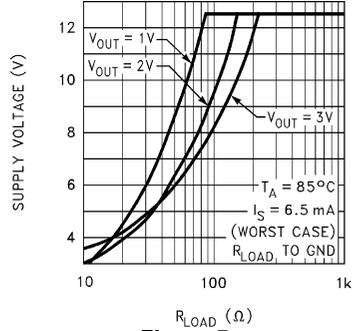


Figure 5.

EL2250C Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)

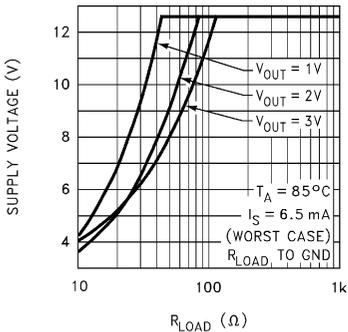


Figure 4.

EL2450C Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)

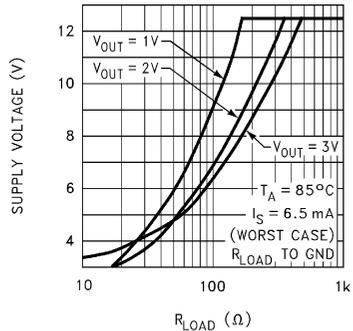
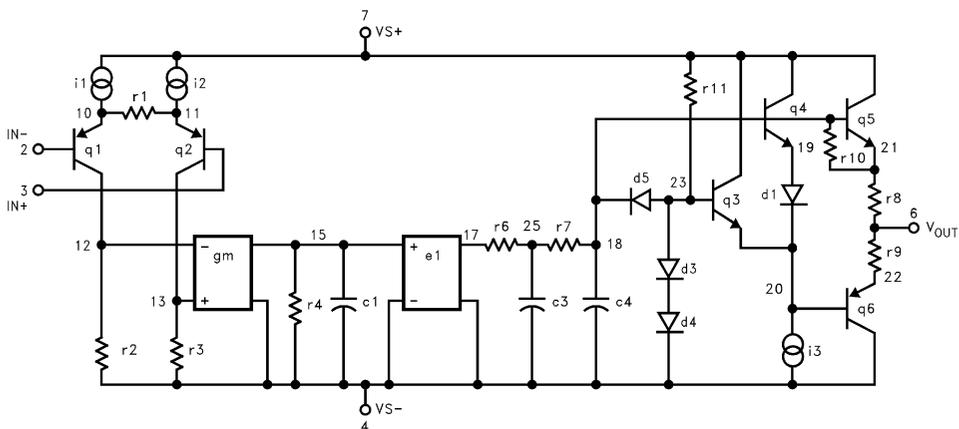


Figure 6.

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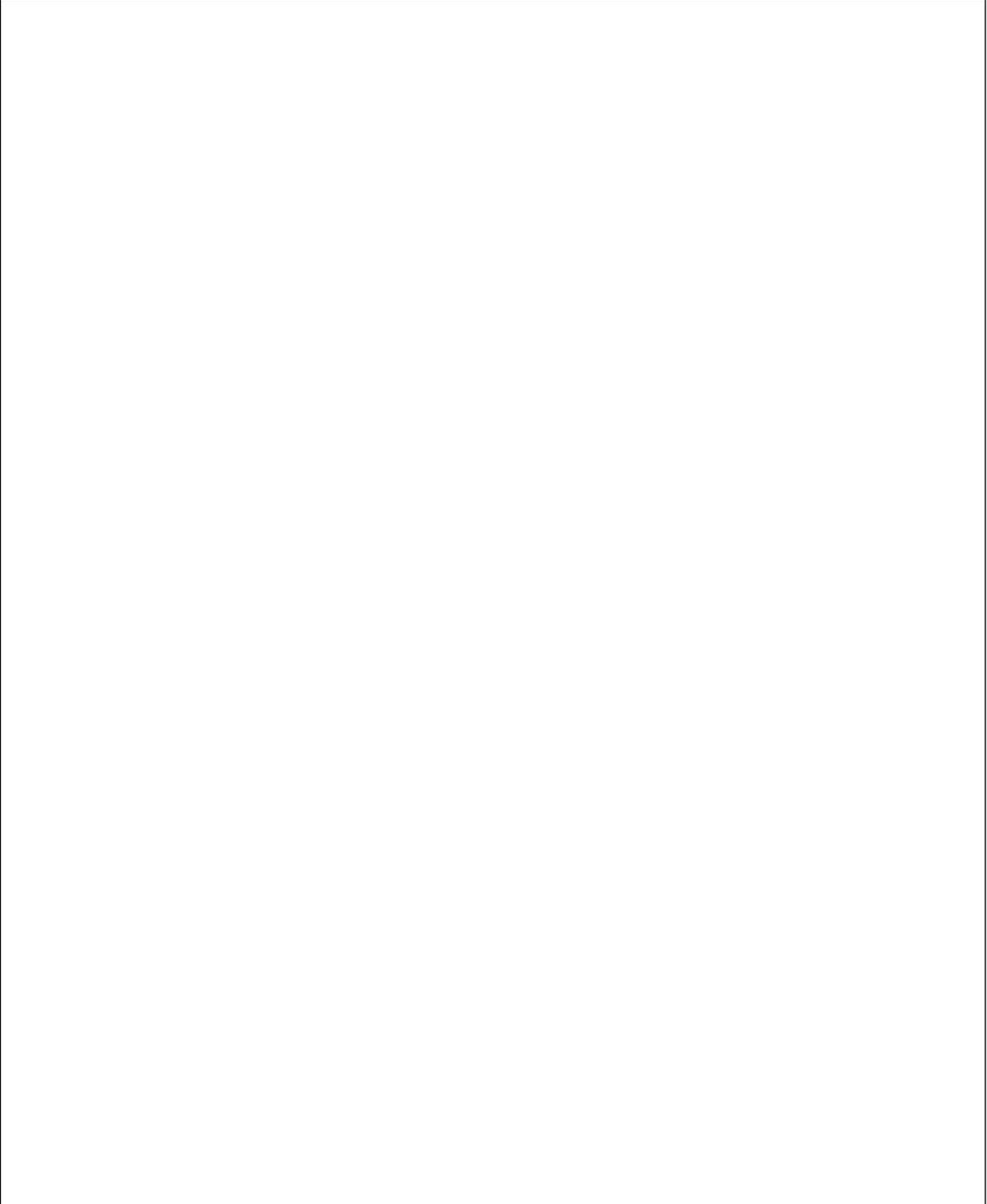
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EL2250C/EL2450C Macromodel (one amplifier)



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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec, Inc.

1996 Tarob Court
Milpitas, CA 95035
Telephone: (408) 945-1323
(800) 333-6314
Fax: (408) 945-9305
European Office: 44-71-482-4596

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