FAIRCHILD
SEMICONDUCTOR™

May 1998

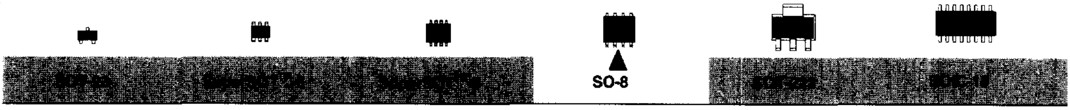
FDS8934A
Dual P-Channel Enhancement Mode Field Effect Transistor

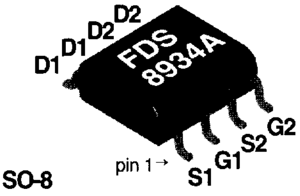
General Description

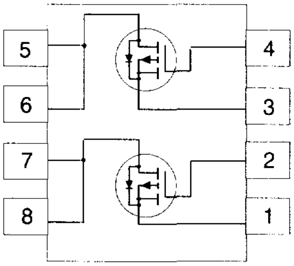
SO-8 P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -4 A , -20 V, $R_{DS(ON)} = 0.055\ \Omega$ @ $V_{GS} = -4.5$ V,
  $R_{DS(ON)} = 0.072\ \Omega$ @ $V_{GS} = -2.5$ V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.







Absolute Maximum Ratings $T_A = 25°C$ unless otherwise noted

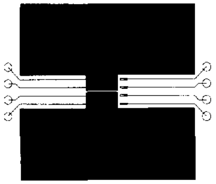
Symbol	Parameter		FDS8934A	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		-8	V
I_D	Drain Current - Continuous	(Note 1a)	- 4	A
	- Pulsed		-20	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

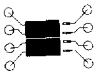
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 °C		-23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			-100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = -250 µA	-0.4	-0.6	-1	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 °C		4		mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -4 A		0.043	0.055	Ω
		T_J =125°C		0.062	0.077	
		V_{GS} = -2.5 V, I_D = -3.4 A		0.059	0.072	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-20			A
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -4 A		13		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		1130		pF
C_{oss}	Output Capacitance			480		pF
C_{rss}	Reverse Transfer Capacitance			120		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DS} = -10 V, I_D = -1 A		8	16	ns
t_r	Turn - On Rise Time	V_{GS} = -4.5 V , R_{GEN} = 6 Ω		23	37	
$t_{D(off)}$	Turn - Off Delay Time			260	360	
t_f	Turn - Off Fall Time			90	125	
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -4 A,		20	28	nC
Q_{gs}	Gate-Source Charge	V_{GS} = -5 V		2.8		
Q_{gd}	Gate-Drain Charge			3.2		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S -1.3 A (Note 2)		-0.7	-1.2	V

Notes:

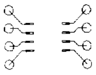
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 78°C/W on a 0.5 in^2 pad of 2oz copper.



b. 125°C/W on a 0.02 in^2 pad of 2oz copper.



c. 135°C/W on a 0.003 in^2 pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

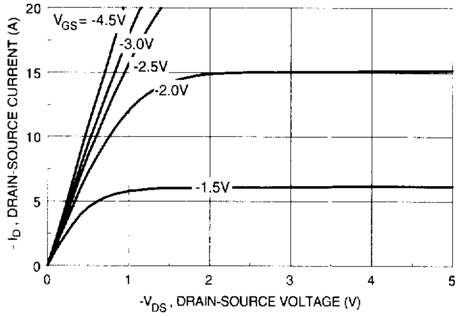


Figure 1. On-Region Characteristics.

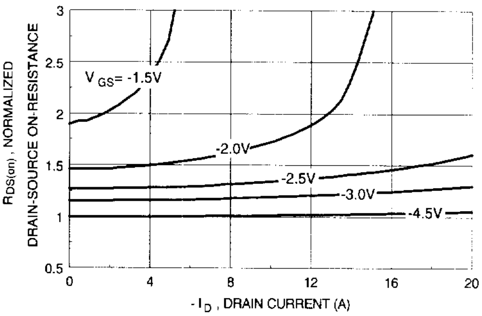


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

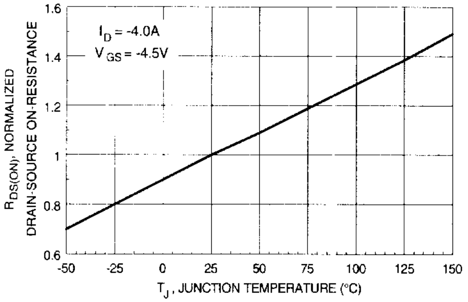


Figure 3. On-Resistance Variation with Temperature.

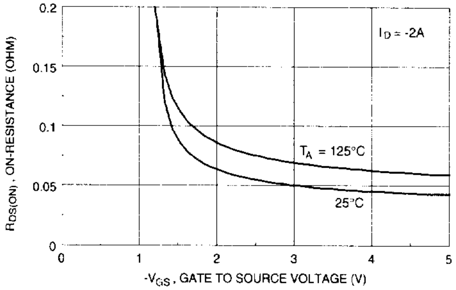


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

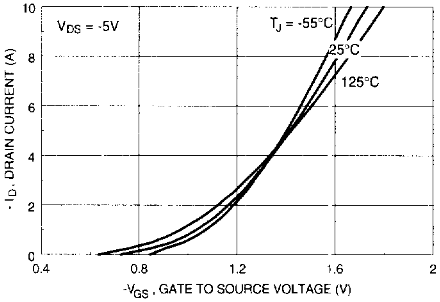


Figure 5. Transfer Characteristics.

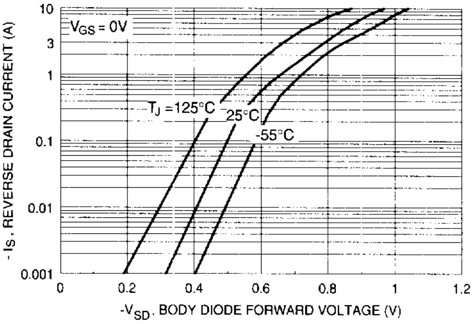


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)

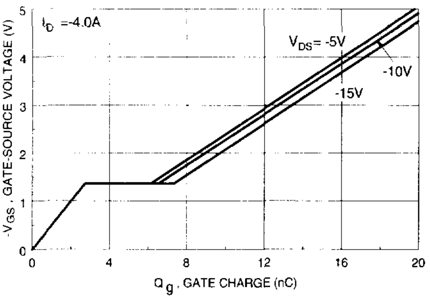


Figure 7. Gate Charge Characteristics.

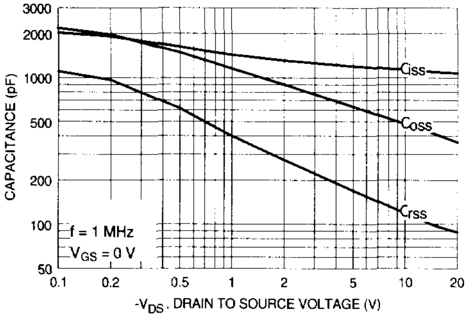


Figure 8. Capacitance Characteristics.

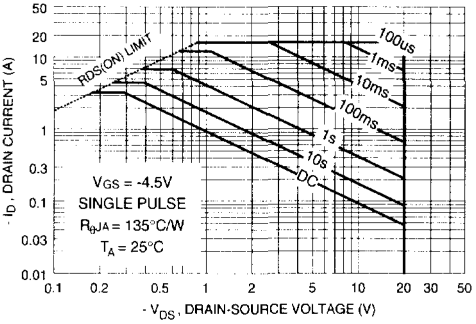


Figure 9. Maximum Safe Operating Area.

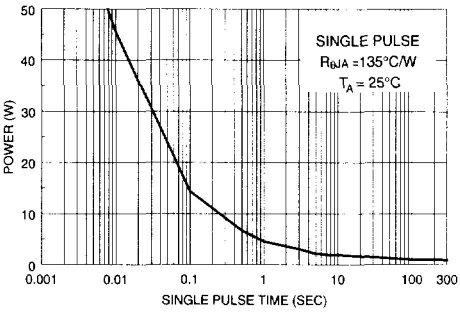


Figure 10. Single Pulse Maximum Power Dissipation.

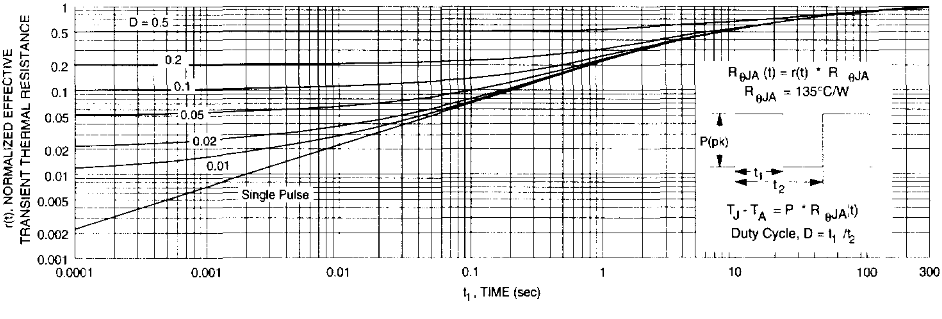


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.