DRAM

4 MEG x 1 DRAM

5V, FAST PAGE MODE, OPTIONAL EXTENDED REFRESH

FEATURES

- 1,024-cycle refresh distributed across 16ms (MT4C1004J) or 128ms (MT4C1004J L only)
- Industry-standard pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN; optional Extended
- FAST PAGE MODE access cycle
- Low power, 0.8mW standby; 225mW active, typical (MT4C1004J L)

OPTIONS — MARKING

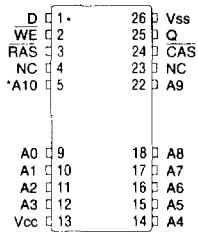
- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - Plastic SOJ (300 mil) — DJ
  - Plastic TSOP (300 mil) — TG
- Refresh Rate
  - Standard 16ms period — None
  - Extended 128ms period — L
- Part Number Example: MT4C1004JDJ-6 L

KEY TIMING PARAMETERS

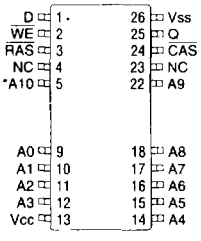
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{RP}
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DA-1)



20/26-Pin TSOP (DB-1)



*Address not used for $\overline{RAS}$-ONLY REFRESH

GENERAL DESCRIPTION

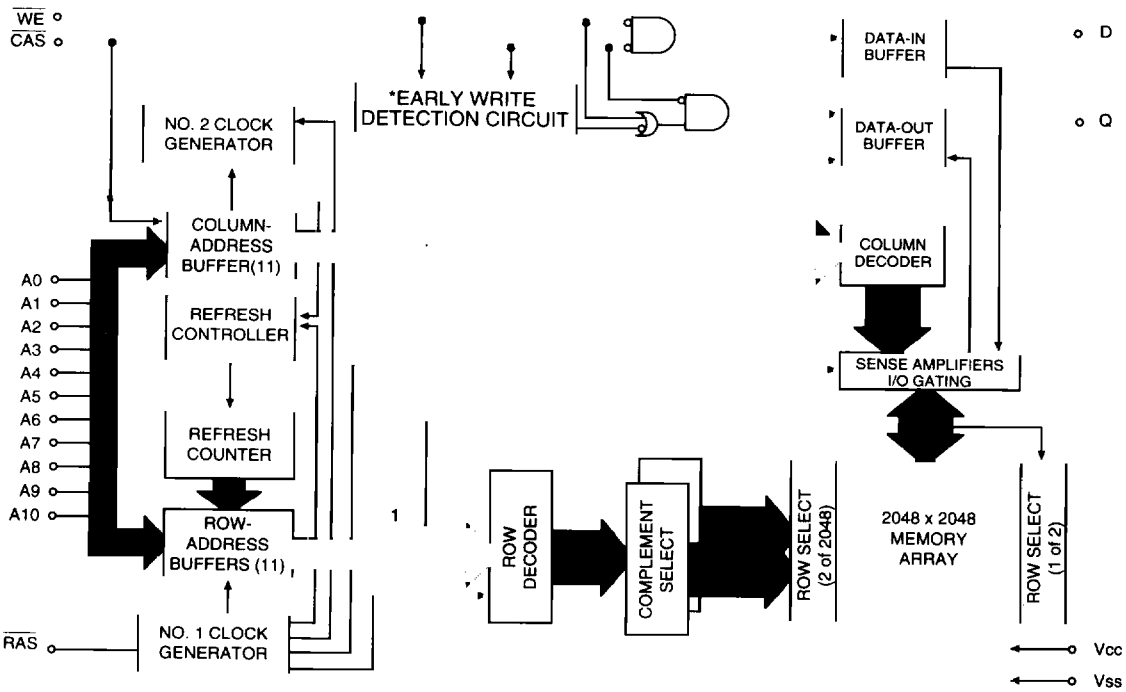
The MT4C1004J(L) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms for the MT4C1004J and every 128ms for the MT4C1004J L, regardless of sequence. The CBR and extended refresh cycles will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES tR	ADDRESSES tC	DATA D (Data-In)	DATA Q (Data-Out)
Standby		H	H→X	X	X	X	"don't care"	High-Z
READ		L	L	H	ROW	COL	"don't care"	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	"don't care"	Data-Out
READ	2nd Cycle	L	H→L	H	n/a	COL	"don't care"	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data-In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data-In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data-In	Data-Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data-In	Data-Out
RAS-ONLY REFRESH		L	H	X	ROW	n/a	"don't care"	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	"don't care"	Data-Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	H	X	X	"don't care"	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 5, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} +1V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA) Output Low Voltage (I_{OUT} = 4.2mA)	V_{OH} V_{OL}	2.4	0.4	V V	

		MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2} I_{CC2} (L only)	1 200	1 200	mA µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, single address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	110	100	mA	3, 25
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	80	70	mA	3, 25
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	110	100	mA	3, 25
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	110	100	mA	3, 4
REFRESH CURRENT: Extended (L version only) Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; A0-A10 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (L only)	300	300	µA	3, 4, 6, 23

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}	7	pF	2
Output Capacitance: Q	C_O	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	45		50		ns	
Column-address setup time	tASC	0		0		ns	
Row-address setup time	tASR	0		0		ns	
Column-address to $\overline{WE}$ delay time	tAWD	30		35		ns	20
Access time from $\overline{CAS}$	tCAC		15		20	ns	14
Column-address hold time	tCAH	10		15		ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	10		10		ns	4
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		ns	
$\overline{CAS}$ precharge time	tCP	10		10		ns	15
Access time from $\overline{CAS}$ precharge	tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		ns	
$\overline{CAS}$ hold time	tCSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	10		10		ns	4
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	15		20		ns	20
Write command to $\overline{CAS}$ lead time	tCWL	15		20		ns	
Data-in hold time	tDH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		ns	
Data-in setup time	tDS	0		0		ns	21
Output buffer turn-off delay	tOFF	3	15	3	20	ns	19, 25
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	60		70		ns	
Access time from $\overline{RAS}$	tRAC		60		70	ns	13
$\overline{RAS}$ to column-address delay time	tRAD	15	30	15	35	ns	17
Row-address hold time	tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	ns	23
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	23
Random READ or WRITE cycle time	tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	ns	16
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	18
Read command setup time	tRCS	0		0		ns	
Refresh period (1,024 cycles)	tREF		16		16	ms	
Refresh period (1,024 cycles) L version	tREF		128		128	ms	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

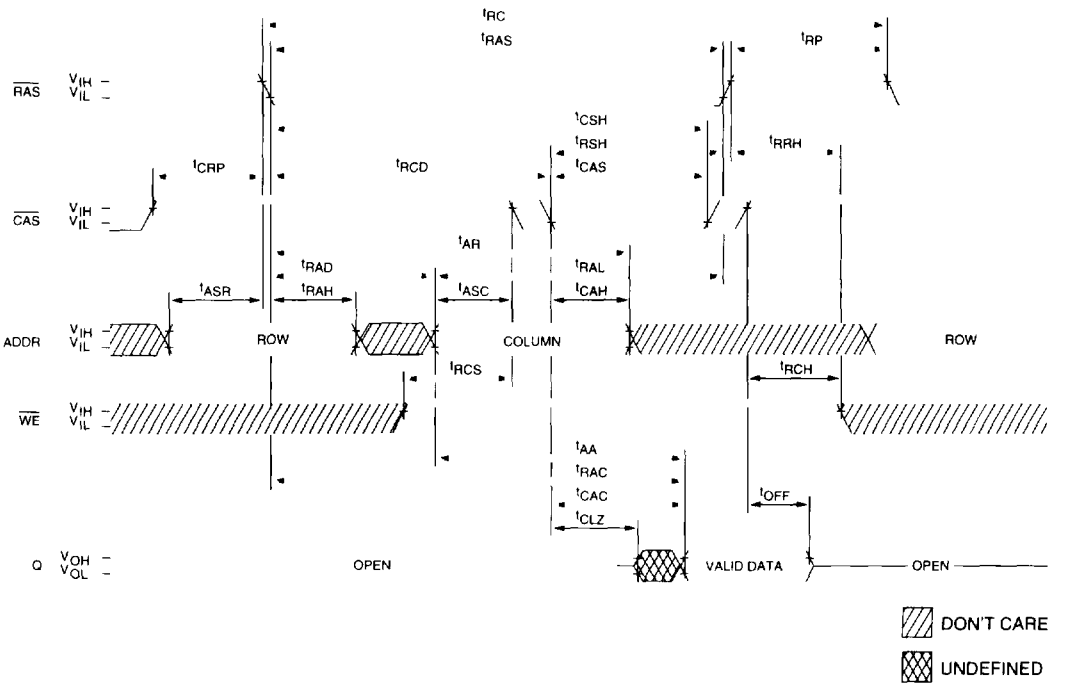
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	18
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ WRITE cycle time	^tRWC	130		155		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	60		70		ns	20
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	20
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 4.5V; f = 1 MHz.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
7. AC characteristics assume ^tT = 5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF.
13. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
14. Assumes that ^tRCD ≥ ^tRCD (MAX).
15. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
16. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
17. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
18. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
19. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
20. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE WRITE, READ WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit through-out the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of data-out is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
21. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. Extended refresh current is reduced as ^tRAS is reduced from its maximum specification during the extended refresh cycle.
24. The 3ns minimum is a parameter guaranteed by design.
25. Column-address changed once each cycle.

READ CYCLE

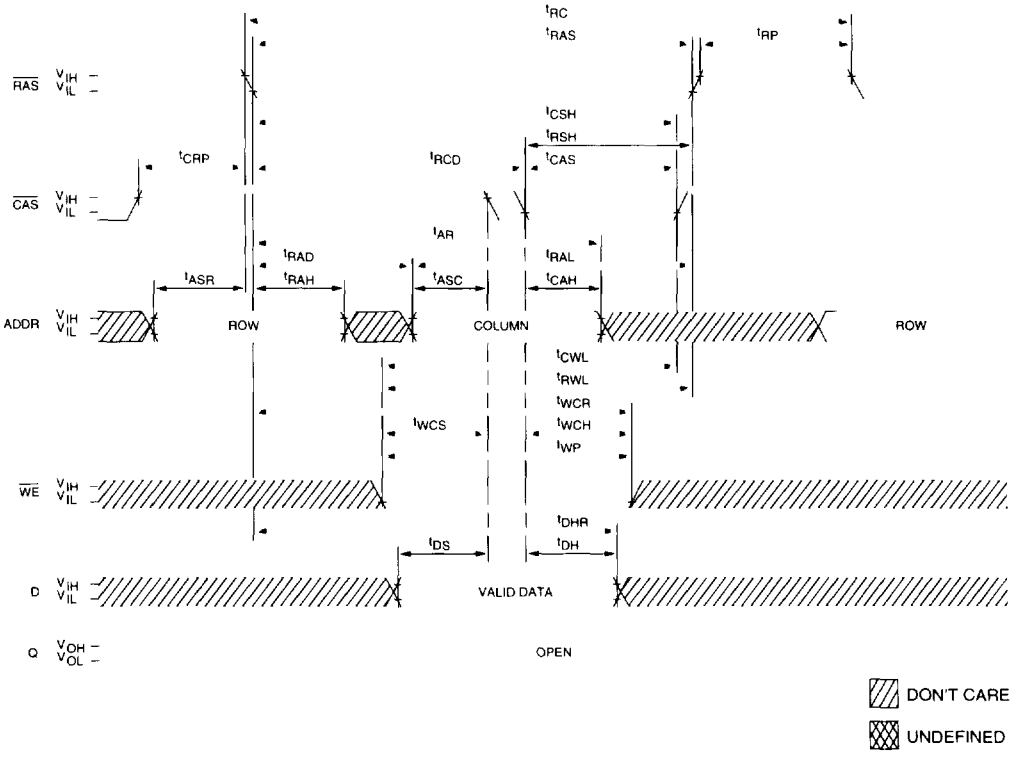


TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	0		0		ns
tCRP	10		10		ns
tCSH	60		70		ns
tOFF	3	15	3	20	ns
tRAC		60		70	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC	110		130		ns
tRCD	20	45	20	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	15		20		ns

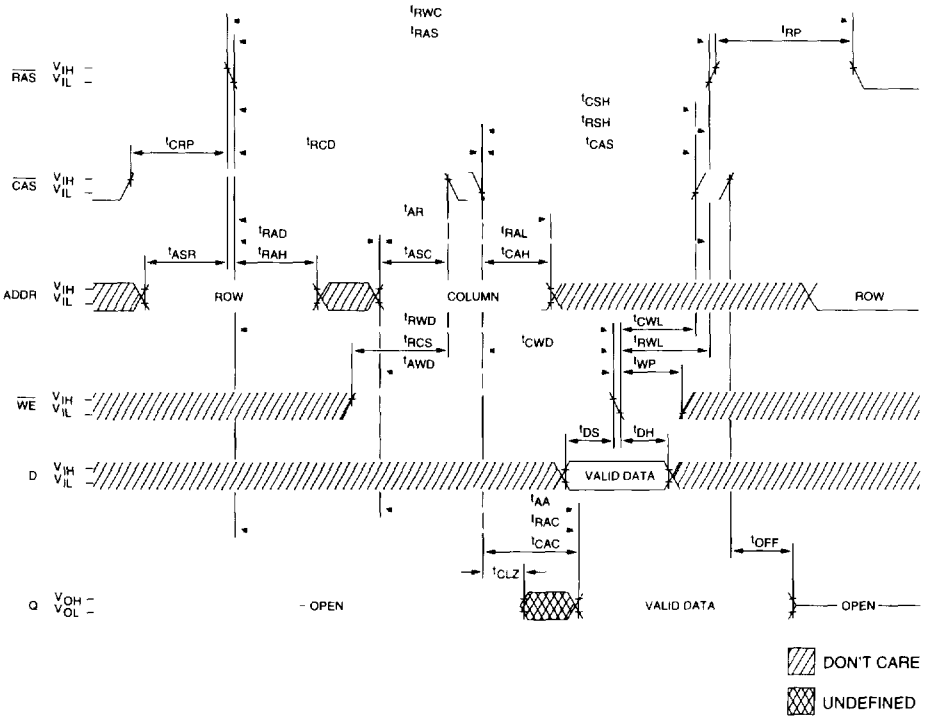
EARLY WRITE CYCLE



TIMING PARAMETERS

	-6		-7				-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS	SYM	MIN	MAX	MIN	MAX	UNITS
tAR	45		50		ns	tRAH	10		10		ns
tASC	0		0		ns	tRAL	30		35		ns
tASR	0		0		ns	tRAS	60	10,000	70	10,000	ns
tCAH	10		15		ns	tRC	110		130		ns
tCAS	15	10,000	20	10,000	ns	tRCD	20	45	20	50	ns
tCRP	10		10		ns	tRP	40		50		ns
tCSH	60		70		ns	tRSH	15		20		ns
tCWL	15		20		ns	tRWL	15		20		ns
tDH	10		15		ns	tWCH	10		15		ns
tDHR	45		55		ns	tWCR	45		55		ns
tDS	0		0		ns	tWCS	0		0		ns
tRAD	15	30	15	35	ns	tWP	10		15		ns

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

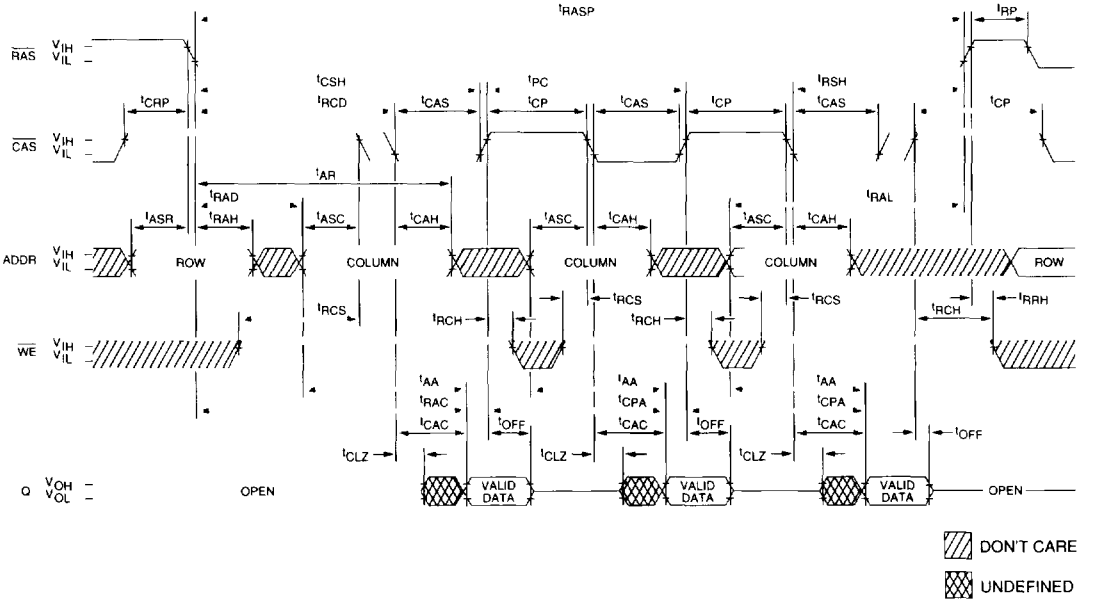


TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	30		35		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	0		0		ns
tCRP	10		10		ns
tCSH	60		70		ns
tCWD	15		20		ns
tCWL	15		20		ns
tDH	10		15		ns
tDS	0		0		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOFF	3	15	3	20	ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRCD	20	45	20	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	15		20		ns
tRWC	130		155		ns
tRWD	60		70		ns
tRWL	15		20		ns
tWP	10		15		ns

FAST-PAGE-MODE READ CYCLE

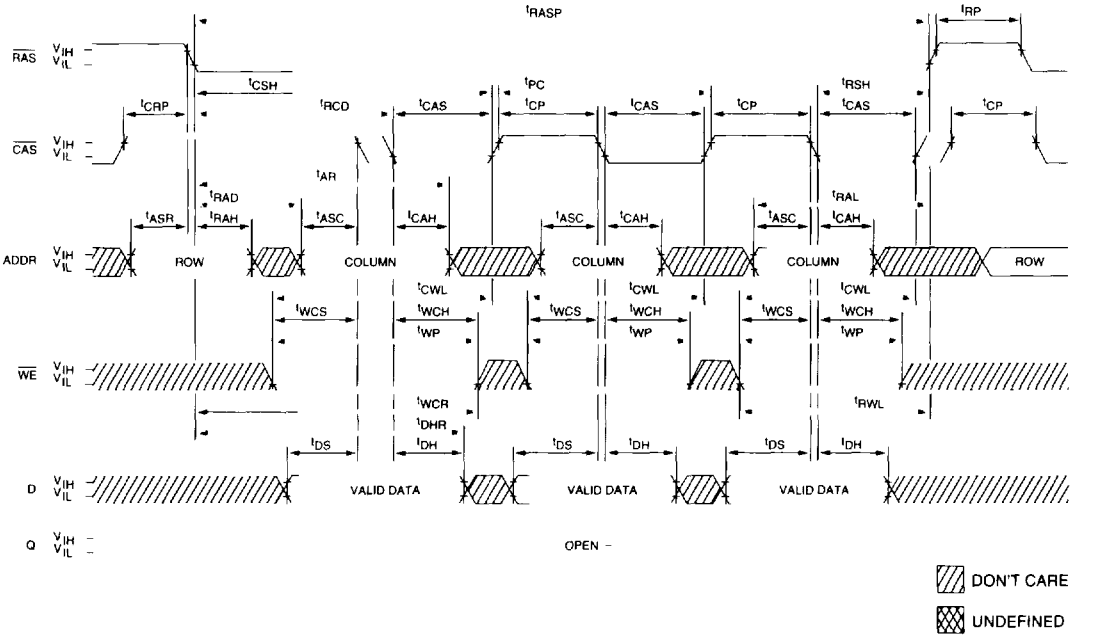


TIMING PARAMETERS

SYM	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	0		0		ns
tCP	10		10		ns
tCPA		35		40	ns
tCRP	10		10		ns
tCSH	60		70		ns
tOFF	3	15	3	20	ns

SYM	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
tPC	35		40		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	15		20		ns

FAST-PAGE-MODE EARLY-WRITE CYCLE

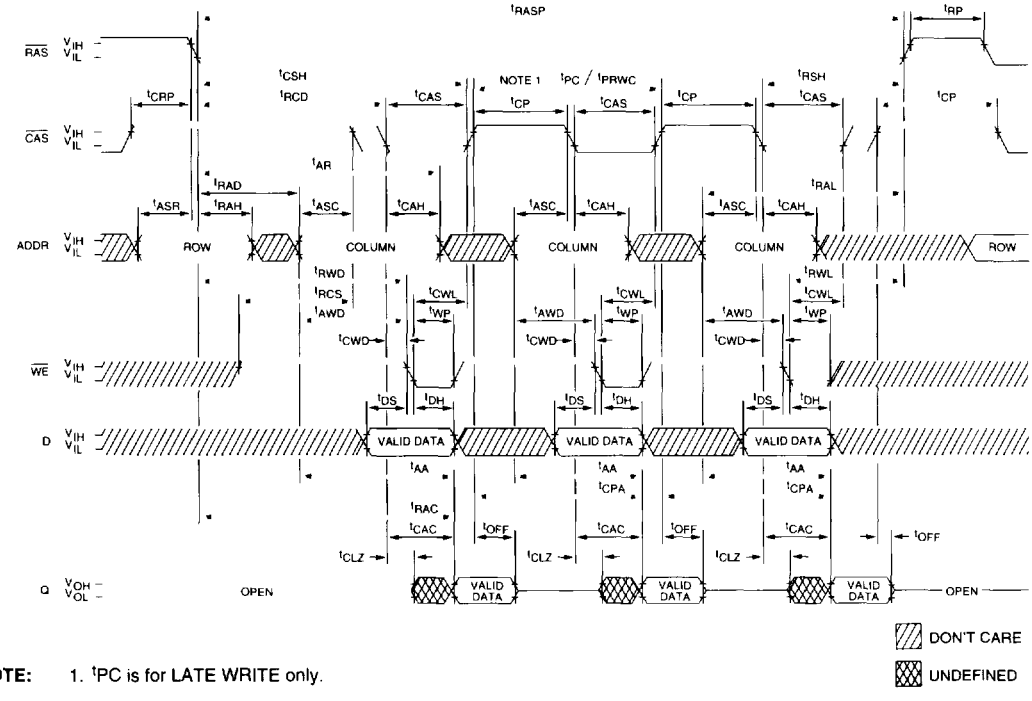


TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCP	10		10		ns
tCRP	10		10		ns
tCSH	60		70		ns
tCWL	15		20		ns
tDH	10		15		ns
tDHR	45		55		ns
tDS	0		0		ns
tPC	35		40		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCR	45		55		ns
tWCS	0		0		ns
tWP	10		15		ns

FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

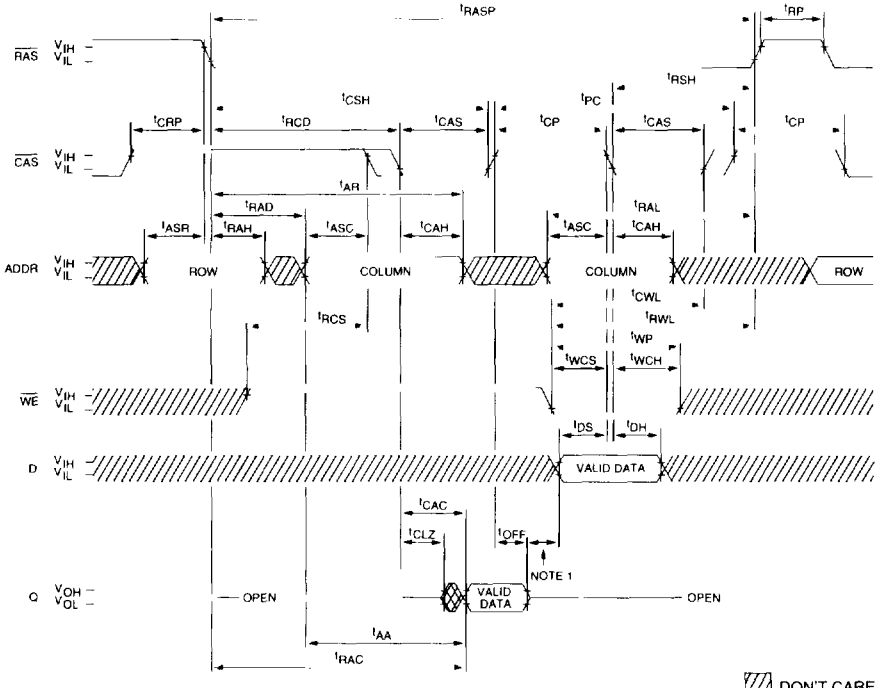


NOTE: 1. tPC is for LATE WRITE only.

TIMING PARAMETERS

	-6		-7				-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS	SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns	tDS	0		0		ns
tAR	45		50		ns	tOFF	3	15	3	20	ns
tASC	0		0		ns	tPC	35		40		ns
tASR	0		0		ns	tPRWC	60		70		ns
tAWD	30		35		ns	tRAC		60		70	ns
tCAC		15		20	ns	tRAD	15	30	15	35	ns
tCAH	10		15		ns	tRAH	10		10		ns
tCAS	15	10,000	20	10,000	ns	tRAL	30		35		ns
tCLZ	0		0		ns	tRASP	60	100,000	70	100,000	ns
tCP	10		10		ns	tRCD	20	45	20	50	ns
tCPA		35		40	ns	tRCS	0		0		ns
tCRP	10		10		ns	tRP	40		50		ns
tCSH	60		70		ns	tRSH	15		20		ns
tCWD	15		20		ns	tRWD	60		70		ns
tCWL	15		20		ns	tRWL	15		20		ns
tDH	10		15		ns	tWP	10		15		ns

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE



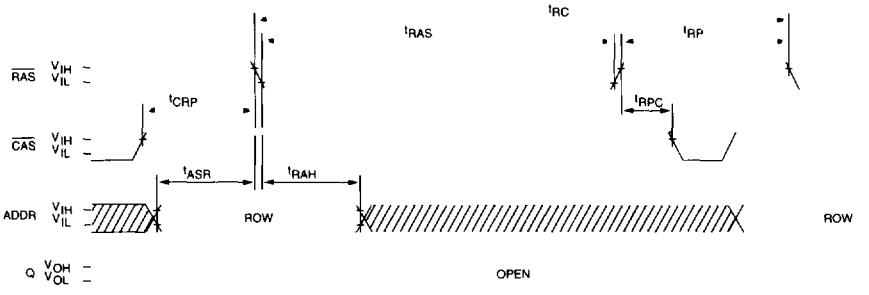
NOTE: 1. Do not drive data prior to tristate.
2. Assumes D and Q are tied together.

TIMING PARAMETERS

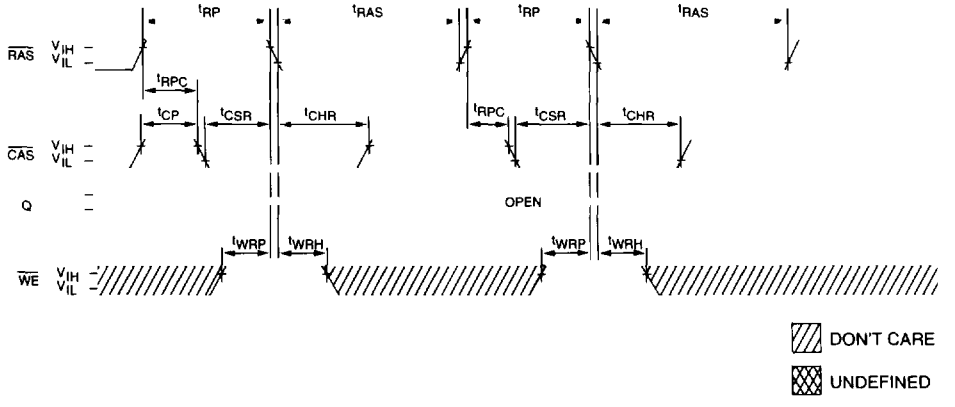
	-6		-7		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	0		0		ns
tCP	10		10		ns
tCRP	10		10		ns
tCSH	60		70		ns
tCWL	15		20		ns
tDH	10		15		ns
tDS	0		0		ns
tOFF	3	15	3	20	ns

	-6		-7		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tPC	35		40		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCS	0		0		ns
tWP	10		15		ns

RAS-ONLY REFRESH CYCLE
(WE and A10 = DON'T CARE)



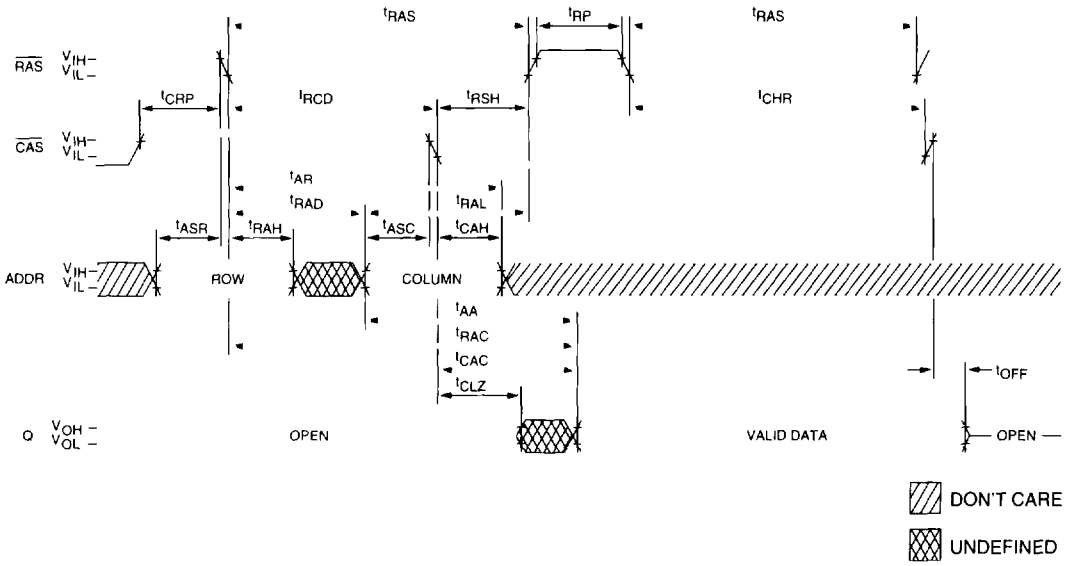
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



TIMING PARAMETERS

	-6		-7				-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS	SYM	MIN	MAX	MIN	MAX	UNITS
tASR	0		0		ns	tRAS	60	10,000	70	10,000	ns
tCHR	10		10		ns	tRC	110		130		ns
tCP	10		10		ns	tRP	40		50		ns
tCRP	10		10		ns	tRPC	0		0		ns
tCSR	10		10		ns	tWRH	10		10		ns
tRAH	10		10		ns	tWRP	10		10		ns

HIDDEN REFRESH CYCLE [22]
($\overline{WE}$ = HIGH)



TIMING PARAMETERS

	-6		-7				-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS	SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns	tOFF	3	15	3	20	ns
tAR	45		50		ns	tRAC		60		70	ns
tASC	0		0		ns	tRAD	15	30	15	35	ns
tASR	0		0		ns	tRAH	10		10		ns
tCAC		15		20	ns	tRAL	30		35		ns
tCAH	10		15		ns	tRAS	60	10,000	70	10,000	ns
tCHR	10		10		ns	tRCD	20	45	20	50	ns
tCLZ	0		0		ns	tRP	40		50		ns
tCRP	10		10		ns	tRSH	15		20		ns