SDC-14580
PROGRAMMABLE SYNCHRO/RESOLVER-TO-DIGITAL CONVERTER

FEATURES

- Wide Bandwidth
- High Carrier Frequency
- Programmable Resolution: 10, 12, 14, or 16 Bits
- High Quality Velocity Output Eliminates Tachometer
- Accuracy to ±1.3 Arc Minutes
- Synchro, Resolver, or Direct Inputs
- Synthesized Reference Eliminates 180° Lock-Up
- MIL-PRF-38534 Processing Available

DESCRIPTION

The SDC-14580 series are versatile state-of-the-art Synchro-to-Digital (S/D) or Resolver-to-Digital (R/D) converters featuring programmable resolution and a velocity output voltage. Based on the popular SDC-14560 Series, the SDC-14580 offers a higher carrier frequency of 1 to 5 kHz and a higher bandwidth of 540 Hz. Tracking rate has also been increased and settling times decreased.

Resolution programming allows selection of 10, 12, 14, or 16 bits and are available with corresponding accuracies of up to 1 minute +1 LSB. Resolution programming combines the high tracking rate of a 10-bit converter with the precision of a 16-bit device in one package. The velocity output (VEL) from the SDC-14580 is a ground-based voltage of 0 to ±10 Vdc with a linearity of 2%. Output voltage is positive for an increasing angle. The digital angle output from the SDC-14580 is a natural binary code, parallel positive logic and is TTL/CMOS compatible.

APPLICATIONS

Because of its high reliability, accuracy, small size, and low power consumption, the SDC-14580 Series are ideal for the most stringent and severe industrial and military ground or avionics applications. Military processing is available (consult factory).

Designed with three-state outputs, the SDC-14580 is especially well-suited for use with computer-based systems. Among the many applications are: radar and navigation systems, fire control systems, flight instrumentation, and flight trainers/simulators.

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7771

SOLID STATE SYNCHRO INPUT OPTION

S1
S2
S3

ELECTRONIC SCOTT T

SIN θ
COS θ

SOLID STATE RESOLVER INPUT OPTION

S1
S2
S3
S4

ELECTRONIC SCOTT T

SIN θ
COS θ

SOLID STATE RESOLVER INPUT OPTION

SIN θ
COS θ

ELECTRONIC SCOTT T

SIN θ
COS θ

V ← INTERNAL DC REFERENCE

INPUT OPTIONS

REF IN

RH   RL

REFERENCE CONDITIONER

R

SYNTHESIZED REF

BIT DETECT

BIT

+15 V   -15 V

DIFF GAIN OF 2

e

DIFF GAIN OF 2.75

VEL

INPUT OPTION

SIN θ
COS θ

HIGH ACCURACY CONTROL TRANSFORMER

GAIN

e
SIN (θ-φ)

DEMOD

D

ERROR PROCESSOR

VEL

VCO

E
T   U

16 BIT CT TRANSPARENT LATCH

1 LSB ANTIJITTER FEEDBACK

CB

DIGITAL ANGLE φ

16 BIT U-D COUNTER

U

T

50 ns DELAY   0.4-1 µs

+5 V

INH

Q

INHIBIT TRANSPARENT LATCH

INH

3 STATE TTL BUFFER

16 BIT OUTPUT TRANSPARENT LATCH

3 STATE TTL BUFFER

EDGE TRIGGERED LATCH

T

+10 V
INTERNAL DC REF V (+5 V)

POWER SUPPLY CONDITIONER

+15

EM   BITS 1-8

BITS 9-16   EL   S

A   B
RESOLUTION CONTROL

FIGURE 1. SDC-14580 BLOCK DIAGRAM

TABLE 1. SDC-14580 SPECIFICATIONS		
These specifications apply over temperature range, power supply range, reference frequency, and amplitude range +10% signal amplitude variation and up to 10% harmonic distortion in the reference.		
PARAMETER	**VALUE**	**COMMENT**
RESOLUTION **ACCURACY GRADES**	10, 12, 14, or 16 bits ±4, ±2, or ±1 minutes	Pin Programmable. Max +1 LSB of selected resolution, see TABLE 8 and Ordering Information.
DIFFERENTIAL LINEARITY **REPEATABILITY**	1 LSB max in the 16th bit 1 LSB max	

REF INPUT CHARACTERISTICS
 Voltage Range
 Carrier Frequency Ranges
  10, 12, or 14 bit
  16 bit
 Input Impedance
  Single Ended Input
  Differential
 Common Mode Range
	
	 1-35 Vrms
	
	 1-5 kHz (full accuracy)
	 2-5 kHz
	
	 50 kOhm min
	 100 kOhm min
	 50 V peak max
	 200 V transient peak
		
		 Up to 10 kHz with reduced accuracy.

SIGNAL INPUT CHARACTERISTICS
 	
 Synchro
  Zin Line to Line
  Zin Each line to ground
  Common Mode Range
 	
 Resolver
  Zin Single Ended
  Zin Differential
  Zin Each line to ground
  Common Mode Range
 	
 Direct (2.0 V L-L)
  Input Signal Type
 	
  sin/cos Range
  Max Voltage Without Damage
 	
  Input Impedance
	
	 11.8 V L-L
	 17.5 kOhm
	 11.5 kOhm
	 60 V max
	
	 11.8 V L-L
	 23 kOhm
	 46 kOhm
	 23 kOhm
	 60 V max
	
	 2 Vrms nom, 2.2 Vrms max
	 15 V CONTINUOUS,
	 100 V PEAK TRANSIENT
	
	 Zin > 20M//10 pF
		Voltage options and minimum input impedance balanced.
		
		 Sin and cos resolver signals referenced to converter internal DC reference voltage, V.

REFERENCE SYNTHESIZER ±Sig/Ref Phase Shift	 60° typ, 45° min	
DIGITAL INPUTS Logic Type Inputs **Max Input Voltage w/o Damage** Loading INH (Inhibit) EN (Enable bits 1-8) and EL (Enable bits 9-16) S (Control Transformer) Resolution Control 10 Bit 12 Bit 14 Bit 16 Bit	 Logic 0 = 0.8 V max Logic 1 = 2.0 V min **-0.3 Vdc to +8 Vdc** 10 µA max B (pin 36) A (pin 35) 0 0 0 1 1 0 1 1	TTL/CMOS compatible. Pull-up current source to +5 V//5 pF max, CMOS transient protected. Logic 0 inhibits, Logic 1 enables, Data stable within 0.3 µs. Logic 0 enables, Logic 1 high Z within 100 ns, Data valid within 150 ns. Logic 0 for Control Transformer, Logic 1 for normal tracking. Unused output bits are at logic 0.
DIGITAL OUTPUTS Parallel Data CB (Converter Busy) BIT (Built-In-Test)	 10, 12, 14, or 16 bits 0.4 µs to 1.0 µs	Natural binary angle positive logic. Positive pulse; leading edge indicates counter update. Logic 0 for BIT condition.

TABLE 1. SDC-14580 SPECIFICATIONS (CONTINUED)

These specifications apply over temperature range, power supply range, reference frequency, and amplitude range;
+10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE			COMMENT

DIGITAL OUTPUTS (CONTINUED)
Drive Capability
  50 pF plus rated logic drive.
    Logic 0
    Logic 1
    Logic 0
    Logic 1
    High Z
	-1.6 mA at 0.4 V max
	0.4 mA at 2.8 V min
	100 mV max
	+5 V supply minus 100 mV min
	10 µA//5 pF max
				1 TTL Load
				10 TTL Loads
				driving CMOS
				driving CMOS

ANALOG OUTPUTS
VEL (Velocity)
e (AC error)
  10 bit mode
  12 bit mode
  14 bit mode
  16 bit mode
Load
	50 mVrms
	25 mVrms
	12.5 mVrms
	6.3 mVrms
	3 kOhm min
				See TABLE 5, Velocity Characteristics.
				
				per LSB of error
				per LSB of error
				per LSB of error
				per LSB of error

DYNAMIC CHARACTERISTICS				See TABLE 7, Dynamic Characteristics.
POWER SUPPLY **CHARACTERISTICS** Nominal Voltage and Range **Max Voltage w/o Damage** Max Current	+15 Vdc ±5% **+18 V** 25 mA	+5 Vdc ±10% **+8 V** 10 mA	-15 Vdc ±5% **-18 V** 15 mA	

TEMPERATURE RANGES
Operating
  -30X
  -10X
Storage
	0 °C to +70 °C
	-55 °C to +125 °C
	-65 °C to +150 °C			

PHYSICAL CHARACTERISTICS Size Weight	1.9 x 0.78 x 0.21 inches (48.3 x 19.8 x 5.3 mm) 0.7 oz (20 gm)			36 pin DDIP

TABLE 2. MAXIMUM RATINGS WITHOUT DAMAGE

PARAMETER	VALUE			COMMENT
Reference Inputs	130 Vrms			
Direct signal Inputs	15 V continuous, 100 V peak transient			
Digital Inputs	-0.3 Vdc to +8 Vdc			**ALL POWER (I.E., POWER SUPPLY AND SIGNAL INPUTS) SHOULD BE REMOVED FROM THE CIRCUIT WHEN ADDING OR REMOVING THE CONVERTER.**
Supply Voltage	+15 Vdc +18 V	+5 Vdc +8 V	-15 Vdc -18 V	
Storage Temperature	-65 °C to 150 °C			
Lead Temperature (soldering, ten seconds)	300 °C			

Thermal Resistance:
  Junction to Case (θ_{JC})
  Case to Ambient (θ_{CA})
	8 °C/W
	20 °C/W			

THEORY OF OPERATION

The SDC-14580 Series are small, 36 pin DDIP Synchro-to-Digital or Resolver-to-Digital hybrid converters. As shown in the block diagram (FIGURE 1), the SDC-14580 can be broken down into the following functional parts: Signal Input Option, Converter, Analog Conditioner, Power Supply Conditioner, and Digital Interface.

CONVERTER OPERATION

As shown in FIGURE 1, the converter section of the SDC-14580 contains a high accuracy control transformer, demodulator, error processor, voltage controlled oscillator (VCO), up-down counter, and reference conditioner. The converter produces a digital angle which tracks the analog input angle to within the specified accuracy of the converter.

The control transformer performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta \cos\phi - \cos\theta \sin\phi$$

Where:

θ is angle theta representing the resolver shaft position.
ϕ is digital angle phi contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) = 0$, so that ϕ will represent the shaft position θ.

The output of the demodulator is an analog DC level proportional to $\sin(\theta-\phi)$. The error processor receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives the VCO. The VCO's clock pulses are accumulated by the up/down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which makes the converter a Type II tracking servo.

In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The reference conditioner is a comparator that produces the square wave reference voltage which drives the demodulator. Its single ended Input Z is 50k Ohms min, 100k Ohms differential.

SPECIAL FUNCTIONS
REFERENCE SYNTHESIZER-QUADRATURE VOLTAGES

The synthesized reference section of the SDC-14580 eliminates errors caused by quadrature voltage. Due to the inductive nature of synchros and resolvers, their signals typically lead the reference signal (RH and RL) by about 6°. When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. In a

12- or 14-bit converter it is not necessary to compensate for the reference signal's phase shift. A 6° phase shift will, however, cause problems for the one minute accuracy converters. As shown in FIGURE 1, the converter synthesizes its own $\cos(\omega t+\alpha)$ reference signal from the $\sin\theta\cdot\cos(\omega t+\alpha)$, $\cos\theta\cdot\cos(\omega t+\alpha)$ signal inputs and from the $\cos\omega t$ reference input. The phase angle of the synthesized reference is determined by the signal input. The reference input is used to choose between the +180° and -180° phases. The synthesized reference will always be exactly in phase with the signal input, and quadrature errors will therefore be eliminated. **The synthesized reference circuit also eliminates the 180° false error null hangup.**

Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error=(Quadrature Voltage/F.S.signal) • $\tan(\alpha)$

Where:

Magnitude of Error is in radians.
Quadrature Voltage is in volts.
Full Scale signal is in volts.
α = signal to REF phase shift

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8 mV
Let: F.S. signal = 11.8 V
Let: α = 6°

Then: Magnitude of Error = 0.35 min $\cong$ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the synchro or resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage=(rotational speed/carrier frequency) • F.S. signal

Where: Speed Voltage is the quadrature due to rotation.
Rotational speed is the RPS (rotations per second) of the synchro or resolver.
Carrier frequency is the REF in Hz

BUILT-IN-TEST ($\overline{BIT}$, PIN 34)

The Built-In-Test output ($\overline{BIT}$) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero. If it exceeds approximately 65 LSBs (of the selected resolution), the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will

TABLE 3. RESOLUTION CONTROL		
B **(PIN 36)**	**A** **(PIN 35)**	**RESOLUTION**
0	0	10 Bit
0	1	12 Bit
1	0	14 Bit
1	1	16 Bit

also change to logic 0 for an over-velocity condition, because the converter loop cannot maintain input-output or if the converter malfunctions where it cannot maintain the loop at a null. $\overline{BIT}$ will also be set if a Loss-of-Signal (LOS) and/or a Loss-of-Reference (LOR) occurs.

PROGRAMMABLE RESOLUTION (A, PIN 35; B, PIN 36)

Resolution is controlled by two logic inputs, A and B (see TABLE 3). The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, inputs A and B are latched internally on the trailing edge of CB (see FIGURE 2). For more information refer to the Accuracy and Resolution section.

Note: All unused digital output data bits are at logic 0.

SPECIAL DESIGN CONSIDERATIONS

Due to its high dynamic capability in 10- and 12-bit mode, the SDC-14580 series of converters has a potential for a spin-around condition. A spin-around condition occurs when the converter does not track and the angular input and the digital output continuously counts (spins) from 0° to 359.999°. An indication of a spin-around condition is the digital output changing as the synchro or resolver input is stationary. During this time, the $\overline{BIT}$ may flag an error condition and the velocity output may be at the maximum positive or negative output voltage. This potential problem may happen at the time the unit is powered up, during a step, or during instantaneous acceleration.

To avoid the spin-around condition when using the SDC-14580 converters in 10- or 12-bit mode, the following is required:

1) Power up the SDC-14580 converter in either the 14- or 16-bit resolution mode and once it has settled change to the 10- or 12-bit mode.

2) Avoid large steps and instantaneous accelerations.

3) If the dynamics required by the system do not exceed the dynamics of the SDC-14580 converter in the 14-bit mode, then set the unit for the 14-bit mode and disregard the additional LSBs.

INTERFACING - INPUT
SIGNAL INPUT OPTIONS

The SDC-14580 series offers three input options: synchro, resolver, or direct resolver input. In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form $\sin\theta-\cos\omega t$, $\sin(\theta+120°)\cos\omega t$, and $\sin(\theta+240°)\cos\omega t$ are internally
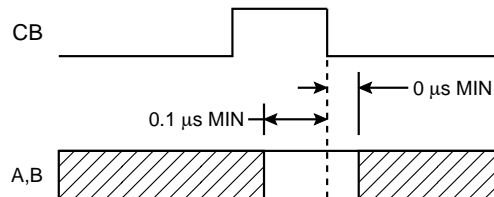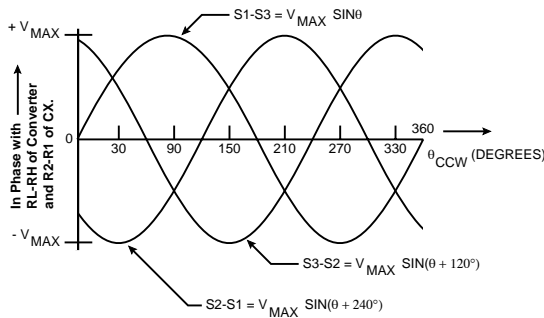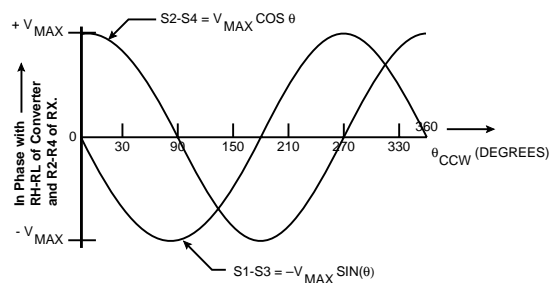

FIGURE 2. RESOLUTION CONTROL TIMING DIAGRAM

Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).

Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.
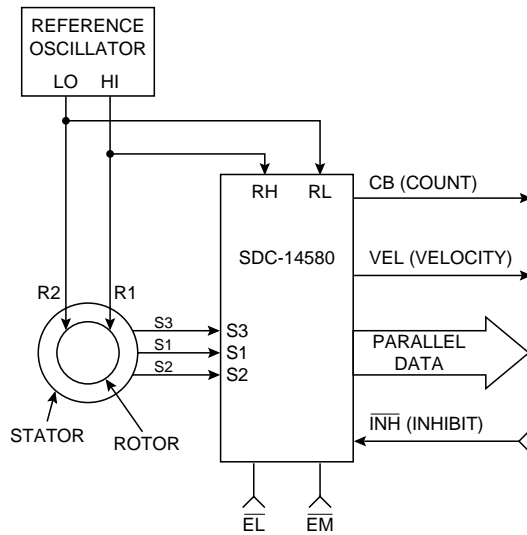
FIGURE 3. SYNCHRO AND RESOLVER SIGNALS
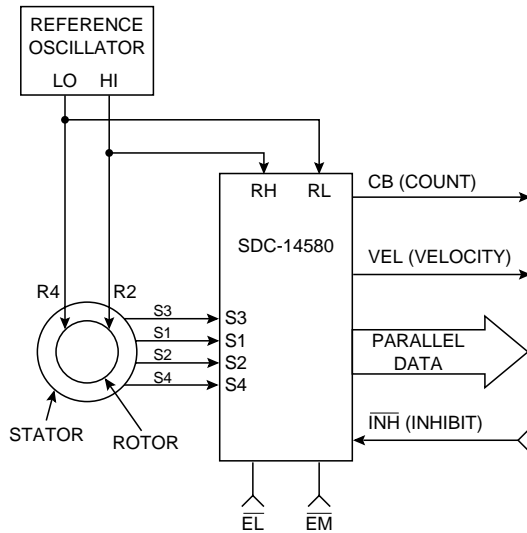
FIGURE 4. SYNCHRO INPUT CONNECTION DIAGRAM

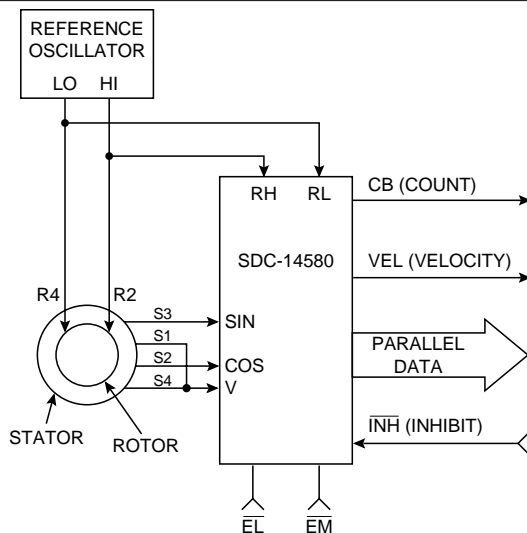**FIGURE 5. RESOLVER INPUT CONNECTION DIAGRAM**

FIGURE 6. DIRECT INPUT CONNECTION DIAGRAM

converted to resolver format; $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. Direct Resolver inputs accept 2.0 Vrms inputs in resolver form, ($\sin\theta-\cos\omega t$ and $\cos\theta\cos\omega t$) and are buffered prior to conversion. FIGURE 3 illustrates synchro and resolver signals as a function of the angle θ.

The solid-state signal and reference inputs are true differential inputs with high AC and DC common mode rejection. *Input impedance is maintained with power off.* The Synchro and Resolver input options are shown in FIGURES 4 and 5. The direct resolver inputs are transient protected voltage followers which accept 2.0 Vrms resolver inputs as shown in FIGURE 6.

RESISTOR PROGRAMMING FOR NON-STANDARD INPUT VOLTAGES

When applying voltages greater than 2.0 Vrms to the direct input option, a simple voltage divider can be used to attenuate both the sin and cos inputs. Since the converter inputs are voltage followers there will be no loading on the resistor dividers. (See FIGURE 7.)

The resolver input conditioner consists of two differential amplifiers. The input is currently scaled down with 23 kOhm resistors for the 11.8 V resolver. When applying resolver input voltages greater than the rated voltages, four additional resistors are used to scale down the voltage. These resistors are placed one in series with each input line (see FIGURE 8).

INTERFACING - DIGITAL OUTPUTS AND CONTROLS
### *DIGITAL INTERFACE*

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{\text{INH}}$) command allowing stable data to be read out of the SDC-14580.

2. Furnishes parallel tri-state data formats.

3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the SDC-14580 applying an Inhibit ($\overline{\text{INH}}$) command will lock the data in the inhibit transparent latch without interfering with the continuous tracking of the converter's feedback loop. Therefore the digital angle ϕ is always updated, and the $\overline{\text{INH}}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50 ns delay are part of the inhibit circuitry. For further information see the INHIBIT ($\overline{\text{INH}}$, PIN 33) paragraph.

DIGITAL ANGLE OUTPUTS (LOGIC INPUT/OUTPUT)
The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{\text{EM}}$ (pin 26) to a logic 0. Depending on the user-programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{\text{EL}}$ (pin 25) to a logic 0.
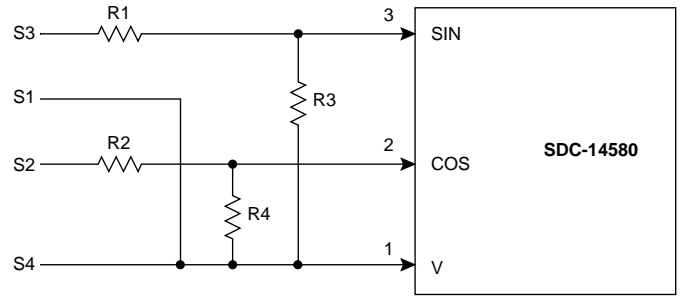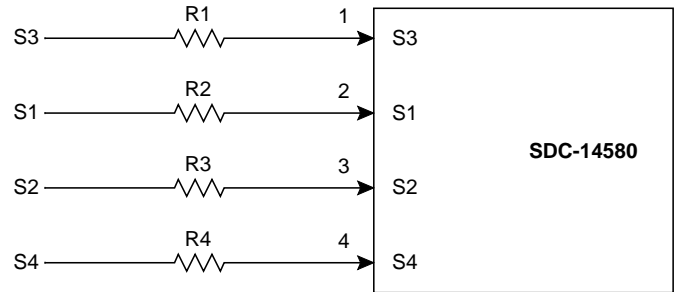

$$\frac{\text{Input Voltage L-L}}{1V} = \frac{R1+R3}{R3}$$

Notes:
(1) R1 = R2; R3 = R4 to 0.1% match.
(2) R1 + R3 and R2 + R4 should be as high as possible to minimize resolver loading.

FIGURE 7. DIRECT INPUT RESISTOR SCALING

$$\frac{R + 23k}{23k} = \frac{\text{Input Voltage L-L}}{11.8 \text{ V}}$$

Notes:
(1) Input Voltage L-L is greater than 11.8 V.
(2) R = R1 = R2 = R3 = R4 to 0.1% match.
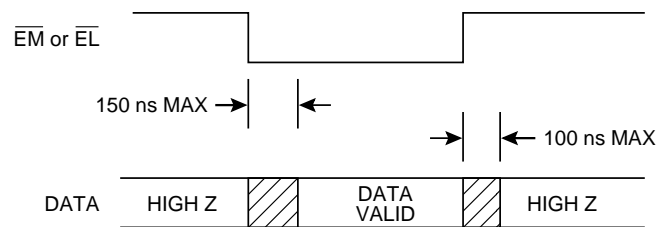
FIGURE 8. RESOLVER INPUT CONNECTION DIAGRAM

FIGURE 9. TRI-STATE OUTPUT TIMING

TABLE 4. DIGITAL ANGLE OUTPUTS		
BIT	**DEG/BIT**	**MIN/BIT**
1 (MSB ALL MODES)	180	10800
2	90	5400
3	45	2700
4	22.5	1350
5	11.25	675
6	5.625	337.5
7	2.8125	168.75
8	1.4063	84.38
9	0.7031	42.19
10 (LSB 10 BIT MODE)	0.3516	31.09
11	0.1758	10.55
12 (LSB 12 BIT MODE)	0.0879	5.27
13	0.0439	2.64
14 (LSB 14 BIT MODE)	0.0220	1.32
15	0.0110	0.66
16 (LSB 16 BIT MODE)	0.0055	0.33

Note: $\overline{EM}$ enables the 8 MSBs and $\overline{EL}$ enables the LSBs.

The second byte will contain either bits 9-10 (10-bit resolution), bits 9-12 (12-bit resolution), bits 9-14 (14-bit resolution), or bits 9-16 (16-bit resolution). All unused LSBs will be at logic 0. TABLE 4 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{EM}$ or $\overline{EL}$ are activated with a logic 0 and are high impedance within 100 ns, max after $\overline{EM}$ and $\overline{EL}$ are set to logic 1 (see FIGURE 9). Both enables are internally pulled up to +5 V // 5 pf max current sources.

DIGITAL ANGLE OUTPUT TIMING
The digital angle outputs 10, 12, 14, or 16 parallel data bits and CONVERTER BUSY (CB). All logic outputs are short-circuit proof to ground and +5 V. The CB output is a positive, 0.4 to 1.0 µs pulse.

The digital output data changes approximately 50 ns after the leading edge of the CB pulse because of an internal delay. Data is valid 0.2 µs after the leading edge of CB (see FIGURE 10). The angle is determined by the sum of the bits at logic 1. The digital outputs are valid 150 ns max after $\overline{EM}$ or $\overline{EL}$ go low and are high impedance within 100 ns max of $\overline{EM}$ or $\overline{EL}$ going high.

INHIBIT ($\overline{INH}$, PIN 33)
When an Inhibit ($\overline{INH}$) input is applied to the SDC-14580, the Output Transparent Latch is locked causing the output data bits to remain stable while data is being transferred. (See FIGURE 11.) The output data bits are stable 0.5 µs after $\overline{INH}$ goes to logic 0.

A logic 0 at the T input of the Inhibit Transparent Latch latches the data, and a logic 1 applied to T allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and $\overline{INH}$. While the counter is not being updated, CB is at logic 0 and the $\overline{INH}$ latch is transparent; when CB goes to logic 1, the $\overline{INH}$ latch is locked. If CB occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not
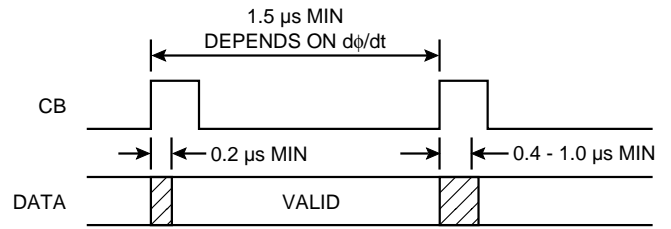

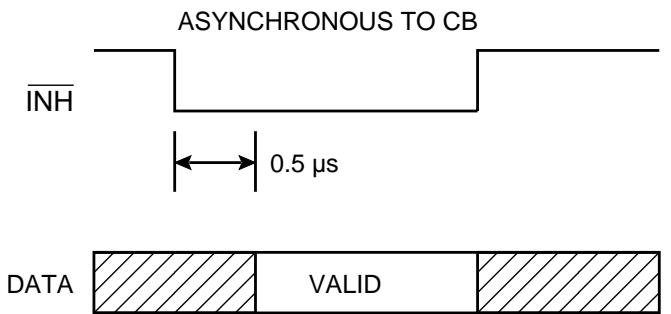**FIGURE 10. CONVERTER BUSY TIMING DIAGRAM**
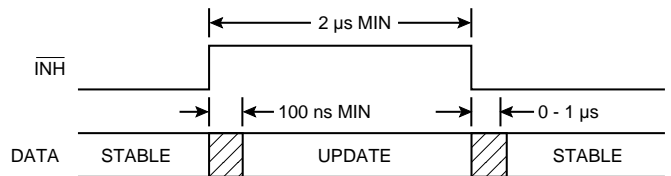

FIGURE 11. INHIBIT TIMING DIAGRAM

FIGURE 12. OUTPUT DATA UPDATE TIMING

change until CB returns to logic 0; if $\overline{INH}$ is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is: (1) Apply $\overline{INH}$; (2) Wait 0.5 µs min; (3) Transfer the data; (4) Release $\overline{INH}$.

A logic 1 for the $\overline{INH}$ enables the output data to be updated. The time it takes for $\overline{INH}$ to go to a logic 1 should be 100 ns minimum before valid data is transferred. To allow the update of the output data with valid information the $\overline{INH}$ must remain at a logic 1 for 1 µs minimum (see FIGURE 12).

DATA TRANSFERS
Digital output data from the SDC-14580 can be transferred to 8-bit and 16-bit bus systems. For 8-bit systems, the MSB and LSB bytes are transferred sequentially. For 16-bit systems all bits are transferred at the same time.

Data Transfer To 8-Bit Bus
FIGURES 13 and 14 show the connections and timing for transferring data from the SDC-14580 to an 8-bit bus.

As can be seen by the timing diagram the following occurs:

1. The converter $\overline{INH}$ control is applied and must remain low for a minimum of 500 ns before valid data is transferred.

2. $\overline{EM}$ is set to a low state (logic 0) 150 ns MIN after $\overline{INH}$ goes low and must remain low for a minimum of 150 ns before the MSB data (1-8) is valid and transferred.

3. As $\overline{EM}$ is set to a high state (logic 1), $\overline{EL}$ is brought low for 150 ns MIN before the LSB data is valid and transferred.

4. $\overline{EL}$ should go high (to logic 1) at least 100 ns MAX before another device uses the bus.

5. $\overline{INH}$ goes high and data transfer is done and the data refresh cycle can begin. Note the time it takes for $\overline{INH}$ to go to a logic 1 should be 100 ns minimum before valid data is transferred.

Note: For further understanding refer to the beginning of this section (i.e., Digital Interface, Digital Angle Outputs, Digital Angle Output Timing, and Inhibit).

16-Bit Data Transfer
Data transfer to the 16-bit bus is much simpler than the 8-bit bus. FIGURES 15 and 16 show the connections and timing for transferring data from the SDC-14580 to a 16-bit bus.

As can be seen by the timing diagram (FIGURE 16) the following occurs:

1. The converter $\overline{INH}$ control is applied and must remain low for a minimum of 500 ns before valid data is transferred.

2. $\overline{EM}$ and $\overline{EL}$ are set to a low state (logic 0) 150 ns MIN after $\overline{INH}$ goes low and must remain low for a minimum of 150 ns before the data (1-16) is valid and transferred.

3. $\overline{EM}$ and $\overline{EL}$ should go high (to logic 1) at least 100 ns MAX before another device uses the bus.

4. $\overline{INH}$ goes high and data transfer is done and the data refresh cycle can begin. Note the time it takes for $\overline{INH}$ to go to a logic 1 should be 100 ns minimum before valid data is transferred.

Note: For further understanding refer to the beginning of this section (i.e., Digital Interface, Digital Angle Outputs, Digital Angle Output Timing, and Inhibit).

INTERFACING - ANALOG OUTPUTS
The analog outputs are AC error (e), Internal DC Reference Voltage, and Velocity (VEL).

AC ERROR (e, PIN 27)
AC Error Out (e) is used in CT mode. The AC error is proportional to the difference between the input angle θ and the digital input angle ϕ, $(\theta - \phi)$, with a scaling of:

50 mV rms/LSB (10-bit mode)
25 mV rms/LSB (12-bit mode)
12.5 mV rms/LSB (14-bit mode)
6.3 mV rms/LSB (16-bit mode)

TABLE 5. VELOCITY CHARACTERISTICS

PARAMETER	UNITS	TYP	MAX
Polarity		Positive for increasing angle	
Output Voltage	V	±13	±10 min
Voltage Scaling	RPS/V	See voltage scaling TABLE 6	
Scale Factor	%	5	10
Scale Factor TC	PPM/°C	100	200
Reversal Error	%	1	2
Reversal Error TC	PPM/°C	25	50
Linearity	% output	1	2
Linearity TC	PPM/°C	25	50
Zero Offset	mV	15	40
Zero Offset TC	µV/°C	25	50
Load	kOhms	—	3 min

TABLE 6. VOLTAGE SCALING RESOLUTION (VALUES IN RPS/VOLT)

10 BIT	12 BIT	14 BIT	16 BIT
80	20	5	1.25

Note: If the resolution is changed while the input is changing, then the velocity output voltage and the digital output will have a transient until it settles to the new velocity scaling at a speed determined by the bandwidth. If additional information is required, consult the factory.
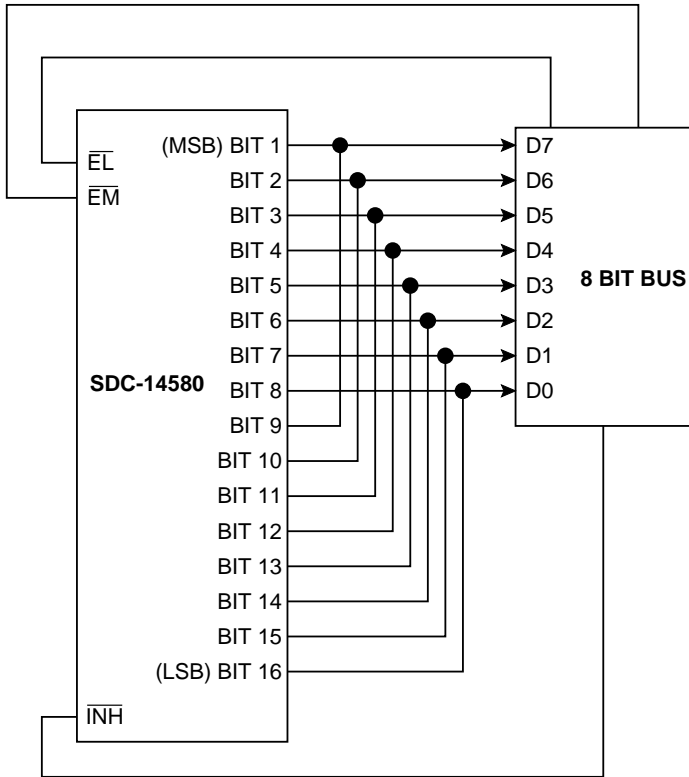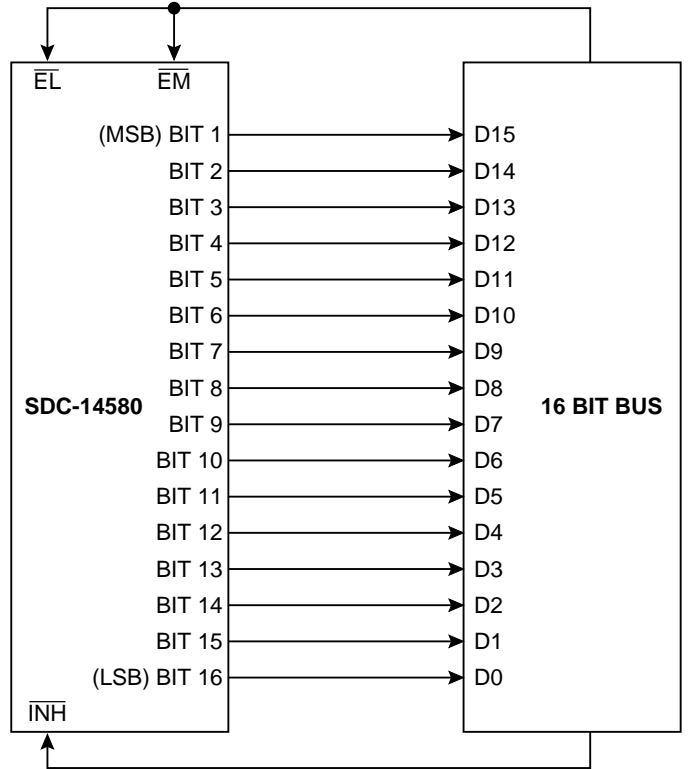
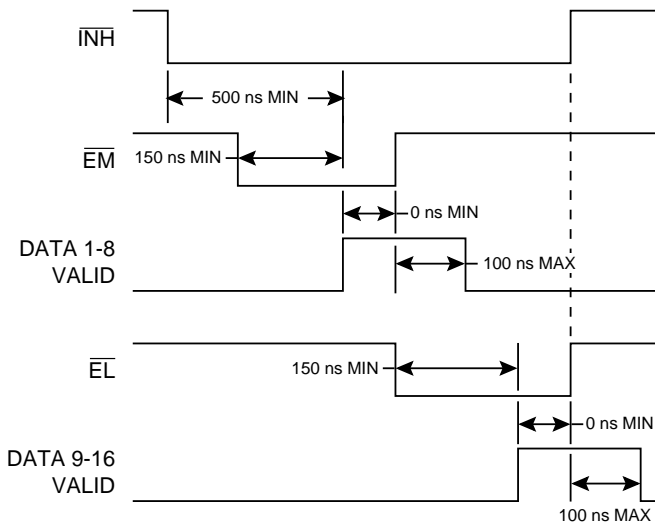**FIGURE 13. 8-BIT DATA TRANSFER**

FIGURE 15. 16-BIT DATA TRANSFER
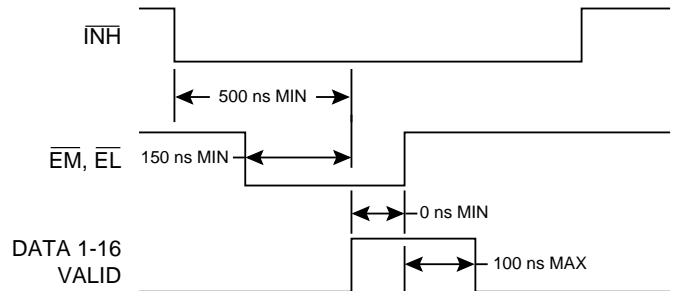

FIGURE 14. 8-BIT DATA TRANSFER TIMING

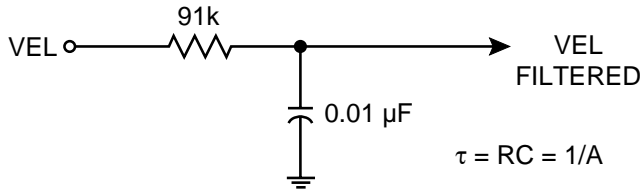**FIGURE 16. 16-BIT DATA TRANSFER TIMING**

FIGURE 17. VEL OUTPUT FILTER

The error is positive if it is in phase with the reference and negative if it is out of phase with the reference.

The e output can swing ±10 V min with respect to ground when the voltage level of the ±15 V power supplies are 15 V. The output level range changes proportionally with the power supply level.

INTERNAL DC REFERENCE VOLTAGE (V, PIN 1)

This internal voltage is not required externally for normal operation of the converter. It is used as the internal dc reference common with the direct input option. It is nominally +5 V and is proportional to the +15 Vdc supply.

VELOCITY (VEL, PIN 23)

The velocity output (VEL, pin 23) is a dc voltage proportional to angular velocity $d\theta/dt$. The velocity is the input to the voltage controlled oscillator (VCO), as shown in FIGURE 1. Its linearity and accuracy are dependent solely on the linearity and accuracy of the VCO.

The VEL output can swing ±10 V with respect to ground when the voltage level of the ±15 V power supplies are 15 V. The output level range changes proportionally with the power supply level. The analog output VEL characteristics are listed in TABLES 5 and 6.

The VEL output has dc tachometer quality specifications such that it can be used as the velocity feedback in servo applications.

TABLE 7. DYNAMIC CHARACTERISTICS

PARAMETER	UNITS	BANDWIDTH			
RESOLUTION	BITS	10	12	14	16
Input Freq.	kHz	1-5	1-5	1-5	2-5
Tracking Rate	RPS min	800	200	50	12.5
bandwidth	Hz	540	←	←	←
K_a	1/sec^2	1.5M	←	←	←
A_1	1/sec	6.2	←	←	←
A_2	1/sec	200k	←	←	←
A	1/sec	1.2k	←	←	←
B	1/sec	600	←	←	←
acc - 1 LSB lag	Deg/sec^2	512k	128k	32k	8k
Settling Time	ms max	15	20	35	70
← Same as value to left					

Note: For 400 Hz and 60 Hz Reference frequencies, use SDC-14560 Series converters.
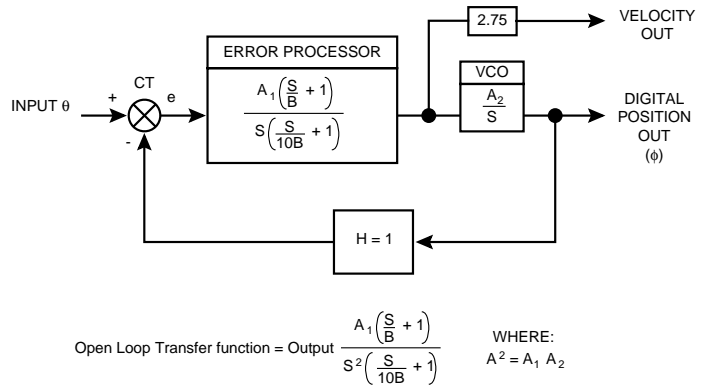
FIGURE 18. TRANSFER FUNCTION BLOCK DIAGRAM

Open Loop Transfer function = Output $\dfrac{A_1\left(\dfrac{S}{B} + 1\right)}{S^2\left(\dfrac{S}{10B} + 1\right)}$ WHERE: $A^2 = A_1\,A_2$
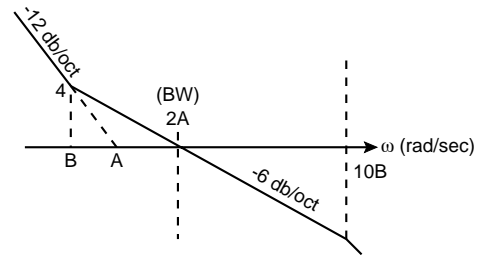
FIGURE 19. OPEN LOOP BODE PLOT

CLOSED LOOP BW (Hz) = $\dfrac{\sqrt{2}\,A}{\pi}$

FIGURE 20. CLOSED LOOP BODE PLOT

FIGURE 21. RESPONSE TO A STEP INPUT

VELOCITY RESPONSE

A filter on the VEL output will, for a step input in velocity, eliminate the velocity overshoot (normally critically damped) and filter carrier frequency ripple. The VEL filter is shown in FIGURE 17.

INTERFACING - DYNAMIC PERFORMANCE

A Type II servo loop (K$_V$ = ∞) and very high acceleration constants give the SDC-14580 superior dynamic performance.

If the power supply voltages are not the +5 Vdc nominal value, the specified input rates will increase or decrease in proportion to the fractional change in voltage.

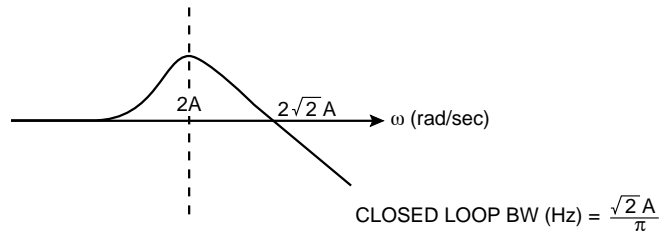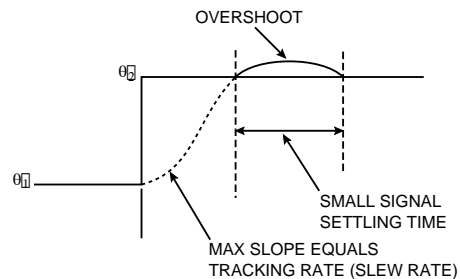### TRANSFER FUNCTIONS

The dynamic performance of the converter can be determined from its transfer function block diagram (FIGURE 18) and open and closed loop Bode plots (FIGURES 19 and 20). Values for the transfer function block can be obtained from TABLE 7.

RESPONSE PARAMETERS

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. FIGURE 21 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

ACCURACY AND RESOLUTION

TABLE 8 lists the total accuracy including quantization for the various resolution and accuracy grades.

FASTER SETTLING TIME USING $\overline{BIT}$ TO REDUCE RESOLUTION

Since the SDC-14580 has higher precision in the higher resolution mode and faster settling in the lower resolution modes, the $\overline{BIT}$ output can be used to program the SDC-14580 for lower resolution, allowing the converter to settle faster for step inputs. High precision, faster settling can therefore be obtained simultaneously and automatically in one unit.

When the resolution is changed, the VEL scaling is also changed. Since the VEL output is from an integrator with a capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth.

SPECIAL APPLICATIONS
CONTROL TRANSFORMER (CT) MODE

The SDC-14580 can also be used as a Control Transformer (CT). The CT mode is used when the AC error (e) is needed to drive an external control loop by the difference angle of the analog input and the digital input. It is also used for presetting the converter to a specific angle to reduce the step response time.

Referring to the equation below, the output is an AC voltage (e) which varies as the sine of the difference between the analog input angle and the digital angle.

$$e = \sin(\theta - \phi) \cos \omega t$$

This is analogous to the function of the rotary control transformer except in this case the rotary shaft input is replaced by a digital signal.

FIGURE 22 illustrates the CT block diagram. The CT mode is enabled by placing S (pin 30) to a logic 0 and by using the digital output lines (now bidirectional) as digital inputs.

When the SDC-14580 functions as a CT the digital inputs are double buffered, $\overline{EM}$ is redefined as $\overline{LM}$ (Latch MSBs), $\overline{EL}$ is redefined as $\overline{LL}$ (Latch LSBs) and $\overline{INH}$ becomes $\overline{LA}$ (Latch All).

Control transformers are frequently used as error signal generators in closed servo loops. The CT mode can be applied in servo systems, as shown in FIGURE 23. In this application, changes in position are commanded by the microcomputer through signals fed to the CT. The CT then drives the motors through dc power amplifiers.

USING THE SDC-14580 AS AN S/D WITH VEL TO STABILIZE POSITION LOOP

FIGURE 24 illustrates a typical use of a SDC-14580 connected as an S/D using the VEL output to stabilize the position loop.

CONNECTING THE SDC-14580 TO A PC BOARD

The SDC-14580 can be attached to a PC board using hand solder or wave soldering techniques. Limit exposure to 300°C (572°F) max, for 10 seconds maximum.

Since the SDC-14580 Series converters contain a CMOS device, standard CMOS handling procedures should be followed.

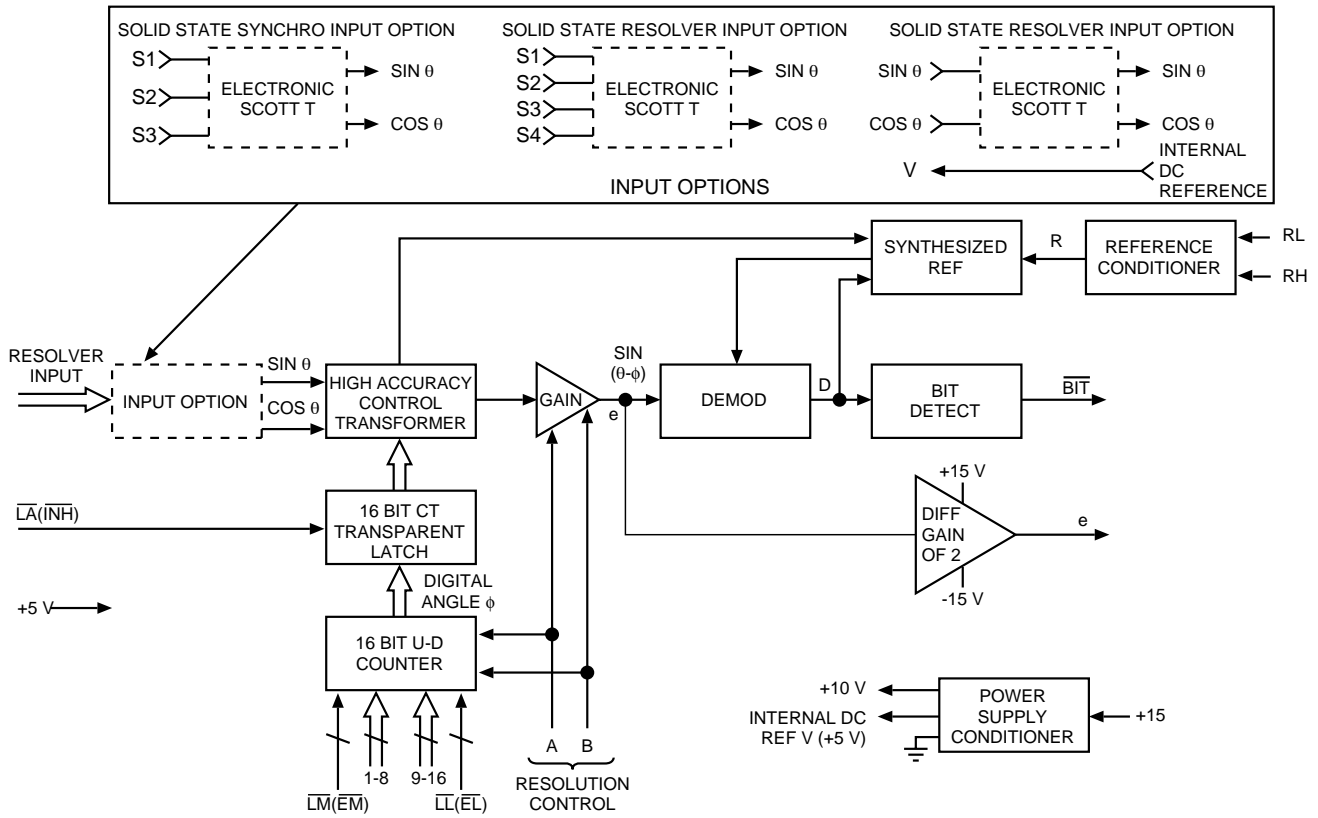| TABLE 8. ACCURACY / RESOLUTION				
ACCURACY (MINUTES)	ACCURACY / RESOLUTION			
	10 BIT	12 BIT	14 BIT	16 BIT
±1 + 1 LSB	22.1	6.3	2.3	1.3
±2 + 1 LSB	23.1	7.3	3.3	2.3
±6 + 1 LSB	25.1	9.3	5.3	4.3
±4 + 1 LSB	27.1	11.3	7.3	6.3

FIGURE 22. CT MODE BLOCK DIAGRAM
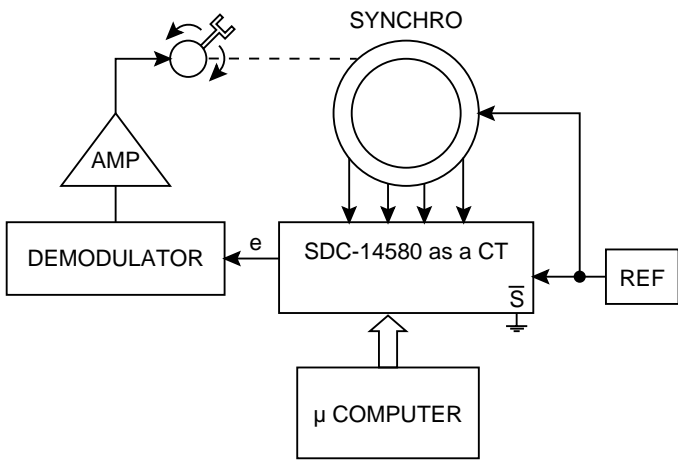
FIGURE 23. CT MODE APPLICATION
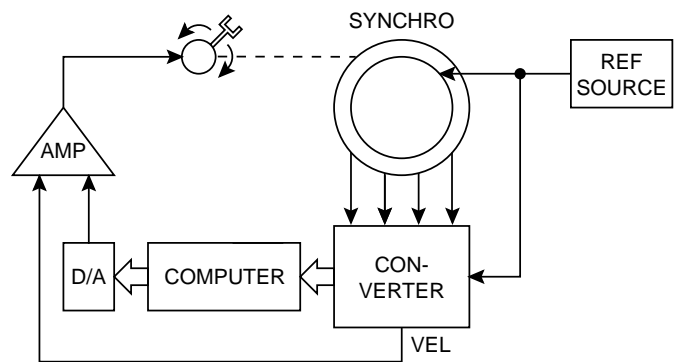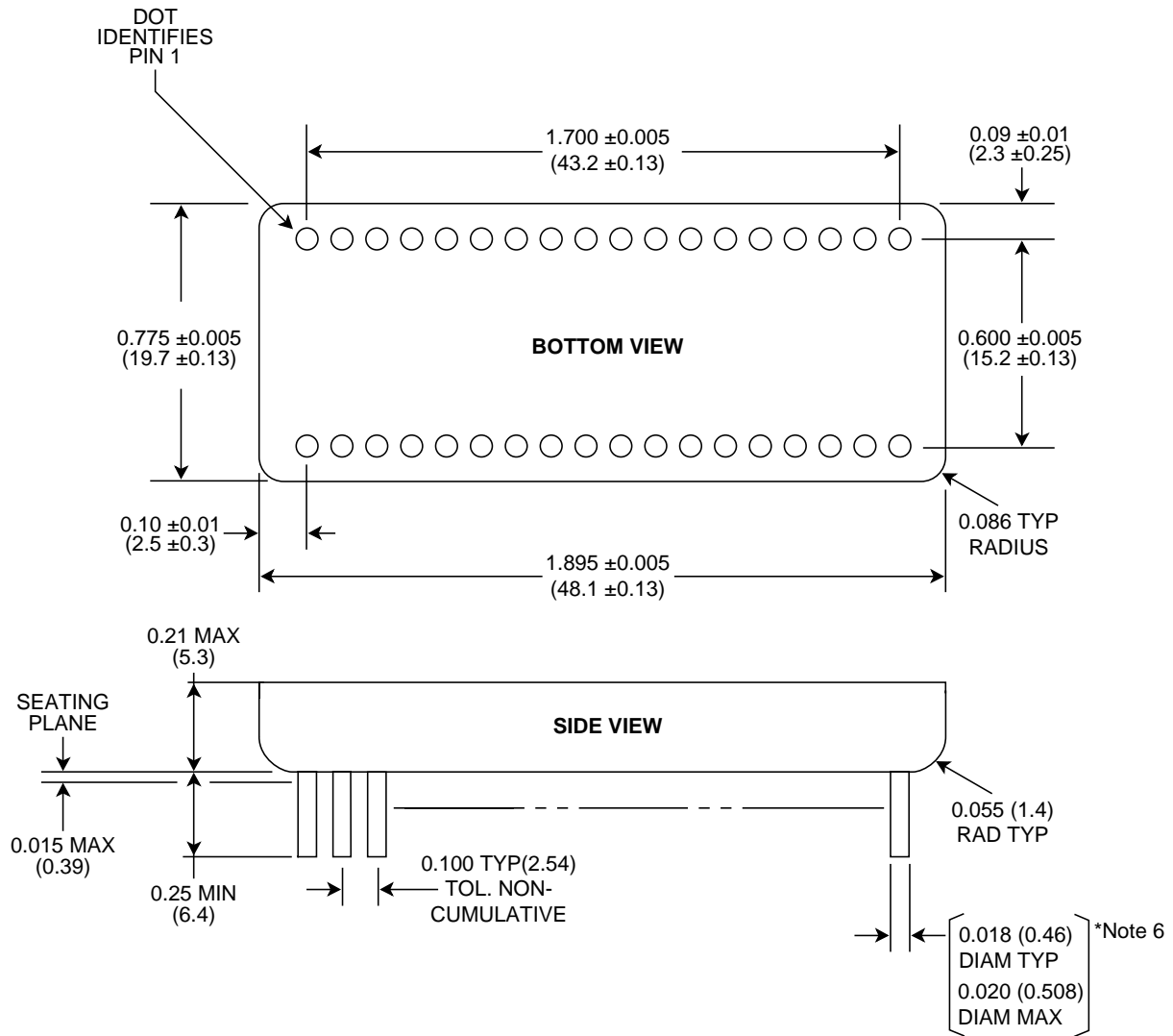

FIGURE 24. CONVERTER WITH VEL TO STABILIZE POSITION

```
        ┌──────┬──────────┬──────┐
   S1   │  1   │          │  36  │  B
   S2   │  2   │          │  35  │  A
   S3   │  3   │          │  34  │  BIT̄
   S4   │  4   │  TOP     │  33  │  ĪNH
   B1   │  5   │  VIEW    │  32  │  +15 V
   B2   │  6   │          │  31  │  -15 V
   B3   │  7   │          │  30  │  S̄
   B4   │  8   │          │  29  │  GND
   B5   │  9   │          │  28  │  +5 V
   B6   │ 10   │          │  27  │  e
   B7   │ 11   │          │  26  │  ĒM
   B8   │ 12   │          │  25  │  ĒL
   B9   │ 13   │          │  24  │  CB
   B10  │ 14   │          │  23  │  VEL
   B11  │ 15   │          │  22  │  B16
   B12  │ 16   │          │  21  │  B15
   B13  │ 17   │          │  20  │  RL
   B14  │ 18   │          │  19  │  RH
        └──────┴──────────┴──────┘
```

FIGURE 25. SDC-14580 PIN LOCATIONS

PIN NO.	TITLE	I/O	FUNCTION
			TABLE 9. SDC-14580 PIN FUNCTIONS
1	S1(S) S1(R) V(X)	I	(S)=Synchro input; (R)=Resolver input; (X)=Direct input
2	S2(S) S2(R) +C(X)	I	(S)=Synchro input; (R)=Resolver input; (X)=Direct input
3	S3(S) S3(R) +S(X)	I	(S)=Synchro input; (R)=Resolver input; (X)=Direct input
4	S4(R)	I	(R)=Resolver input
5	B1	O	Digital Output Bit 1 (MSB)
6	B2	O	Digital Output Bit 2
7	B3	O	Digital Output Bit 3
8	B4	O	Digital Output Bit 4
9	B5	O	Digital Output Bit 5
10	B6	O	Digital Output Bit 6
11	B7	O	Digital Output Bit 7
12	B8	O	Digital Output Bit 8
13	B9	O	Digital Output Bit 9
14	B10	O	Digital Output Bit 10 (LSB - 10-BIT MODE)
15	B11	O	Digital Output Bit 11
16	B12	O	Digital Output Bit 12 (LSB - 12-BIT MODE)
17	B13	O	Digital Output Bit 13
18	B14	O	Digital Output Bit 14 (LSB - 14-BIT MODE)
19	RH	I	AC Reference Input. Used to drive internal demodulator
20	RL	I	AC Reference Input. Used to drive internal demodulator
21	B15	O	Digital Output Bit 15
22	B16	O	Digital Output Bit 16 (LSB - 16-BIT MODE)
23	VEL	O	Velocity. DC voltage proportional to angular velocity
24	CB	O	Converter Busy. Indicates digital output update.
25	$\overline{EL}$	I	Enable LSBs. Logic 0 enables digital output bits 9-16. Logic 1 disables these bits.
26	$\overline{EM}$	I	Enable MSBs. Logic 0 enables digital output bits 1-8. Logic 1 disables these bits.
27	e	O	AC Error. Used in CT mode; e is proportional to the difference between the input angle θ and the digital input angle ϕ ($\theta-\phi$).
28	+5 V	I	Supply Voltage
29	GND	—	Ground
30	S	I	Control Transformer Set. Logic 1 for normal tracking; logic 0 for CT operation. Used when AC error (e) is needed to drive external control loop by the difference angle of the resolver input and the digital input and for presetting the converter to a specific angle to reduce the step response time.
31	-15 V	I	Supply Voltage
32	+15 V	I	Supply Voltage
33	$\overline{INH}$	O	Inhibit. Logic 0 prevents digital output bits from changing.
34	$\overline{BIT}$	O	Built-ln-Test. Monitors level of error (D) and will change to logic 0 if it exceeds 65 bits approx. Also logic 0 for an over-velocity condition.
35	A	I	Resolution Control. Changes resolution during converter operation to 10, 12, 14, or 16 bits dependent on logic level.
36	B	I	Resolution Control. Changes resolution during converter operation to 10, 12, 14, or 16 bits dependent on logic level.

DOT
IDENTIFIES
PIN 1

1.700 ±0.005
(43.2 ±0.13)

0.09 ±0.01
(2.3 ±0.25)

BOTTOM VIEW

0.775 ±0.005
(19.7 ±0.13)

0.600 ±0.005
(15.2 ±0.13)

0.10 ±0.01
(2.5 ±0.3)

0.086 TYP
RADIUS

1.895 ±0.005
(48.1 ±0.13)

0.21 MAX
(5.3)

SEATING
PLANE

SIDE VIEW

0.055 (1.4)
RAD TYP

0.015 MAX
(0.39)

0.100 TYP(2.54)
TOL. NON-
CUMULATIVE

0.25 MIN
(6.4)

0.018 (0.46)
DIAM TYP   *Note 6

0.020 (0.508)
DIAM MAX

Notes:
1. Dimensions shown are in inches (mm).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.01 (0.25) of outline dimensions.
   Lead spacing dimensions apply only at seating plane.
4. Package is Kovar with electroless nickel plating.
5. Case is electrically floating.
6. After pre-tinning diameter maximum is 0.021

FIGURE 26. SDC-14580 MECHANICAL OUTLINE 36-PIN DDIP

ORDERING INFORMATION

SDC-1458X-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = 100% Pull Test
- Q = 100% Pull Test and Pre-Cap Source Inspection
- K = One Lot Date Code
- W = One Lot Date Code and Pre-Cap Source Inspection
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test
- Blank = None of the Above

Accuracy:
- 2 = 4 minutes + 1 LSB
- 4 = 2 minutes + 1 LSB
- 5 = 1 minute + 1 LSB

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Configuration:
- 0 = 11.8V, Synchro
- 5 = 11.8V, Resolver
- 7 = 2 V, Direct Resolver

NOTES:
For 400 Hz and 60 Hz reference frequencies use the SDC-14560 Series converters.
Drawings to DESC format available from factory.
* Standard DDC Processing with burn-in and full temperature test—see table below.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
TEST	**MIL-STD-883**	
	METHOD(S)	**CONDITION(S)**
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 [note 1], 1030 [note 2]	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.

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Germany - Tel: +49-(0)8141-349-087, Fax: +49-(0)8141-349-089
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