## Features

- Fast Read Access Time - 100 ns
- Low Power CMOS Operation
    - 100 µA max. Standby
    - 40 mA max. Active at 5 MHz
- JEDEC Standard Packages
    - 32-Lead 600-mil PDIP and Cerdip
    - 32-Lead 450-mil SOIC (SOP)
    - 32-Lead TSOP
- 5V ± 10% Supply
- High Reliability CMOS Technology
    - 2,000V ESD Protection
    - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 50 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Industrial and Commercial Temperature Ranges

## 8 Megabit (1M x 8) UV Erasable CMOS EPROM

**3**

## Description

The AT27C080 chip is a low power, high performance 8,388,608 bit ultraviolet erasable programmable read only memory (EPROM) organized as 1M by 8 bits. The AT27C080 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 100 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

Atmel's scaled CMOS technology provides low active power consumption and fast programming. Power consumption is typically 10 mA in active mode and less than 10 µA in standby mode.
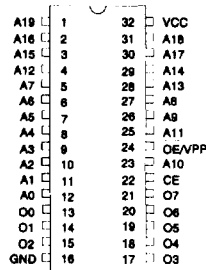
*(continued)*

## Pin Configurations

| Pin Name | Function |
|----------|----------|
| A0 - A19 | Addresses |
| O0 - O7 | Outputs |
| CE | Chip Enable |
| OE | Output Enable |

### CDIP, PDIP, SOIC Top View

| | | | | |
|---|---|---|---|---|
| A19 | 1 | | 32 | VCC |
| A16 | 2 | | 31 | A18 |
| A15 | 3 | | 30 | A17 |
| A12 | 4 | | 29 | A14 |
| A7 | 5 | | 28 | A13 |
| A6 | 6 | | 27 | A8 |
| A5 | 7 | | 26 | A9 |
| A4 | 8 | | 25 | A11 |
| A3 | 9 | | 24 | OE/VPP |
| A2 | 10 | | 23 | A10 |
| A1 | 11 | | 22 | CE |
| A0 | 12 | | 21 | O7 |
| O0 | 13 | | 20 | O6 |
| O1 | 14 | | 19 | O5 |
| O2 | 15 | | 18 | O4 |
| GND | 16 | | 17 | O3 |

### TSOP Top View
### Type 1

| | | | |
|---|---|---|---|
| A11 | 1 | 32 | OE/VPP |
| A9 | 2 | 31 | A10 |
| A8 | 3 | 30 | CE |
| A13 | 4 | 29 | O7 |
| A14 | 5 | 28 | O6 |
| A17 | 6 | 27 | O4 |
| A18 | 7 | 26 | O5 |
| VCC | 8 | 25 | O3 |
| A19 | 9 | 24 | GND |
| A16 | 10 | 23 | O2 |
| A15 | 11 | 22 | O1 |
| A12 | 12 | 21 | O0 |
| A7 | 13 | 20 | A1 |
| A6 | 14 | 19 | A0 |
| A5 | 15 | 18 | A3 |
| A4 | 16 | 17 | A2 |

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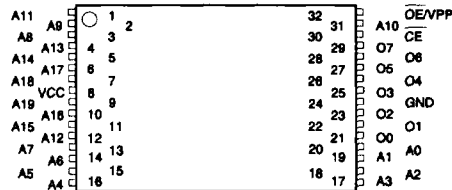
## Description (Continued)

The AT27C080 is available in a choice of packages, including; one-time programmable (OTP) plastic PDIP, SOIC (SOP), and TSOP, as well as windowed ceramic Cerdip. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 1M byte storage capability, the AT27C080 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C080 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

## Erasure Characteristics

The entire memory array of the AT27C080 is erased (all outputs read as $V_{OH}$) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm$^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm$^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

## System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the $V_{CC}$ and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the $V_{CC}$ and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

**AT27C080**

## Block Diagram
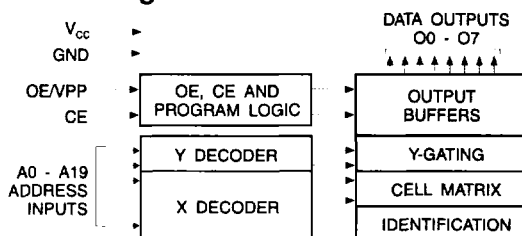


## Absolute Maximum Ratings*

| | |
|---|---|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7.0V [1] |
| Voltage on A9 with Respect to Ground | -2.0V to +14.0V [1] |
| $V_{PP}$ Supply Voltage with Respect to Ground | -2.0V to +14.0V [1] |
| Integrated UV Erase Dose | 7258 W•sec/cm$^2$ |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC}$ + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

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## Operating Modes

| Mode \ Pin | $\overline{CE}$ | $\overline{OE}/V_{PP}$ | Ai | Outputs |
|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | Ai | $D_{OUT}$ |
| Output Disable | X | $V_{IH}$ | X [1] | High Z |
| Standby | $V_{IH}$ | X | X | High Z |
| Rapid Program [2] | $V_{IL}$ | $V_{PP}$ | Ai | $D_{IN}$ |
| PGM Verify | $V_{IL}$ | $V_{IL}$ | Ai | $D_{OUT}$ |
| PGM Inhibit | $V_{IH}$ | $V_{PP}$ | X | High Z |
| Product Identification [4] | $V_{IL}$ | $V_{IL}$ | A9 = $V_H$ [3] <br> A0 = $V_{IH}$ or $V_{IL}$ <br> A1 - A19 = $V_{IL}$ | Identification Code |

Notes: 1. X can be $V_{IL}$ or $V_{IH}$.
2. Refer to Programming characteristics.
3. $V_H$ = 12.0 ± 0.5V.

4. Two identifier bytes may be selected. All Ai inputs are held low ($V_{IL}$), except A9 which is set to $V_H$ and A0 which is toggled low ($V_{IL}$) to select the Manufacturer's Identification byte and high ($V_{IH}$) to select the Device Code byte.

## DC and AC Operating Conditions for Read Operation

| | | AT27C080 | | |
|---|---|---|---|---|
| | | -10 | -12 | -15 |
| Operating Temperature (Case) | Com. | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C |
| | Ind. | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C |
| V$_{CC}$ Power Supply | | 5V ± 10% | 5V ± 10% | 5V ± 10% |

## DC and Operating Characteristics for Read Operation

| Symbol | Parameter | Condition | | Min | Max | Units |
|---|---|---|---|---|---|---|
| I$_{LI}$ | Input Load Current | V$_{IN}$ = 0V to V$_{CC}$ | Com., Ind. | | ±1 | µA |
| I$_{LO}$ | Output Leakage Current | V$_{OUT}$ = 0V to V$_{CC}$ | Com., Ind. | | ±5 | µA |
| I$_{SB}$ | V$_{CC}$ [(1)] Standby Current | I$_{SB1}$ (CMOS), $\overline{CE}$ = V$_{CC}$ ± 0.3V | | | 100 | µA |
| | | I$_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to V$_{CC}$ + 0.5V | | | 1 | mA |
| I$_{CC}$ | V$_{CC}$ Active Current | f = 5 MHz, I$_{OUT}$ = 0 mA, $\overline{CE}$ = V$_{IL}$ | | | 40 | mA |
| V$_{IL}$ | Input Low Voltage | | | -0.6 | 0.8 | V |
| V$_{IH}$ | Input High Voltage | | | 2.0 | V$_{CC}$ + 0.5 | V |
| V$_{OL}$ | Output Low Voltage | I$_{OL}$ = 2.1 mA | | | 0.4 | V |
| V$_{OH}$ | Output High Voltage | I$_{OH}$ = -400 µA | | 2.4 | | V |

Note: 1. V$_{CC}$ must be applied simultaneously or before $\overline{OE}$/V$_{PP}$, and removed simultaneously or after $\overline{OE}$/V$_{PP}$.

## AC Characteristics for Read Operation

| | | | AT27C080 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | -10 | | -12 | | -15 | | |
| Symbol | Parameter | Condition | Min | Max | Min | Max | Min | Max | Units |
| t$_{ACC}$ [(4)] | Address to Output Delay | $\overline{CE}$ = $\overline{OE}$/V$_{PP}$ = V$_{IL}$ | | 100 | | 120 | | 150 | ns |
| t$_{CE}$ [(3)] | $\overline{CE}$ to Output Delay | $\overline{OE}$/V$_{PP}$ = V$_{IL}$ | | 100 | | 120 | | 150 | ns |
| t$_{OE}$ [(3, 4)] | $\overline{OE}$/V$_{PP}$ to Output Delay | $\overline{CE}$ = V$_{IL}$ | | 35 | | 35 | | 40 | ns |
| t$_{DF}$ [(2, 5)] | $\overline{OE}$/V$_{PP}$ or $\overline{CE}$ High to Output Float, whichever occurred first | | | 30 | | 35 | | 40 | ns |
| t$_{OH}$ | Output Hold from Address, $\overline{CE}$ or $\overline{OE}$/V$_{PP}$, whichever occurred first | | 0 | | 0 | | 0 | | ns |

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

**AT27C080**

## AC Waveforms for Read Operation [1]
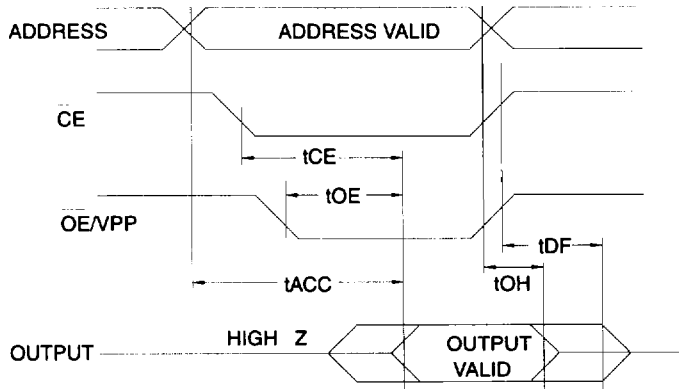


Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $t_{DF}$ is specified from $\overline{OE}$ /$V_{PP}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$/$V_{PP}$ may be delayed up to $t_{CE}$ - $t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$.
4. $\overline{OE}$ /$V_{PP}$ may be delayed up to $t_{ACC}$ - $t_{OE}$ after the address is valid without impact on $t_{ACC}$.
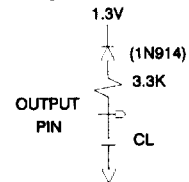5. This parameter is only sampled and is not 100% tested.

## Input Test Waveforms and Measurement Levels
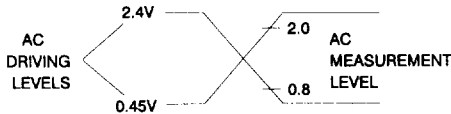


$t_R$, $t_F$ < 20ns (10% to 90%)

## Output Test Load



Note: $C_L$ = 100 pF including jig capacitance.
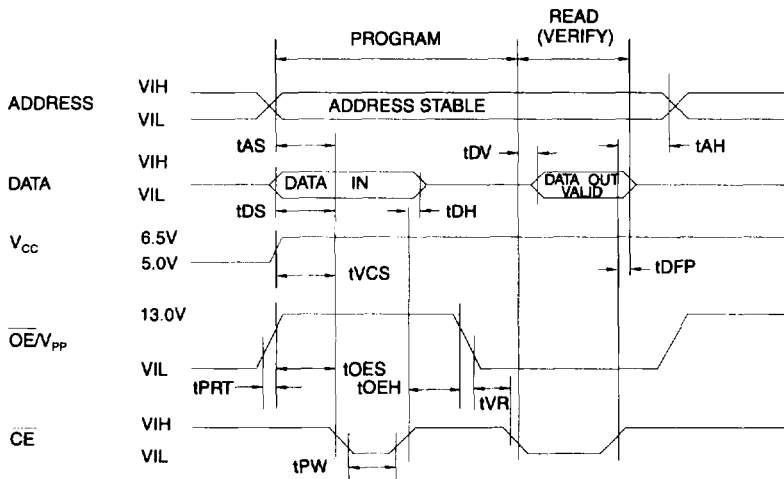
## Pin Capacitance  (f = 1 MHz  T = 25°C) [1]

|  | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 8 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

Note:   1. Typical values for nominal supply voltage.  This parameter is only sampled and is not 100% tested.

## Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for $V_{IL}$ and 2.0V for $V_{IH}$.
2. $t_{OE}$ and $t_{DFP}$ are characteristics of the device but must be accommodated by the programmer.

## DC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

| Symbol | Parameter | Test Conditions | Limits Min | Limits Max | Units |
|--------|-----------|-----------------|-----|-----|-------|
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{IL}, V_{IH}$ | | ±10 | µA |
| $V_{IL}$ | Input Low Level | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input High Level | | 2.0 | $V_{CC} + 1$ | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL} = 2.1$ mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH} = -400$ µA | 2.4 | | V |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program and Verify) | | | 40 | mA |
| $I_{PP2}$ | $\overline{OE}/V_{PP}$ Current | $\overline{CE} = V_{IL}$ | | 25 | mA |
| $V_{ID}$ | A9 Product Identification Voltage | | 11.5 | 12.5 | V |

## AT27C080

## AC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

| Symbol | Parameter | Test Conditions* (1) | Limits Min | Limits Max | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address Setup Time | | 2 | | μs |
| $t_{OES}$ | $\overline{OE}/V_{PP}$ Setup Time | | 2 | | μs |
| $t_{OEH}$ | $\overline{OE}/V_{PP}$ Hold Time | | 2 | | μs |
| $t_{DS}$ | Data Setup Time | | 2 | | μs |
| $t_{AH}$ | Address Hold Time | | 0 | | μs |
| $t_{DH}$ | Data Hold Time | | 2 | | μs |
| $t_{DFP}$ | $\overline{CE}$ High to Output Float Delay (2) | | 0 | 130 | ns |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | μs |
| $t_{PW}$ | $\overline{CE}$ Program Pulse Width (3) | | 47.5 | 52.5 | μs |
| $t_{DV}$ | Data Valid from $\overline{CE}$ (2) | | | 1 | μs |
| $t_{VR}$ | $\overline{OE}/V_{PP}$ Recovery Time | | 2 | | μs |
| $t_{PRT}$ | $\overline{OE}/V_{PP}$ Pulse Rise Time During Programming | | 50 | | ns |

*AC Conditions of Test:
Input Rise and Fall Times (10% to 90%)...............20 ns
Input Pulse Levels.....................................0.45V to 2.4V
Input Timing Reference Level....................0.8V to 2.0V
Output Timing Reference Level.................0.8V to 2.0V

Notes: 1. $V_{CC}$ must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 50 μsec ± 5%.

## Atmel's 27C080 Integrated Product Identification Code

| Codes | A0 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E |
| Device Type | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 8A |

The "Pins" header spans columns A0 through O0.

## Rapid Programming Algorithm

A 50 μs $\overline{CE}$ pulse width is used to program. The address is set to the first location. $V_{CC}$ is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 50 μs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 50 μs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to $V_{IL}$ and $V_{CC}$ to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



3
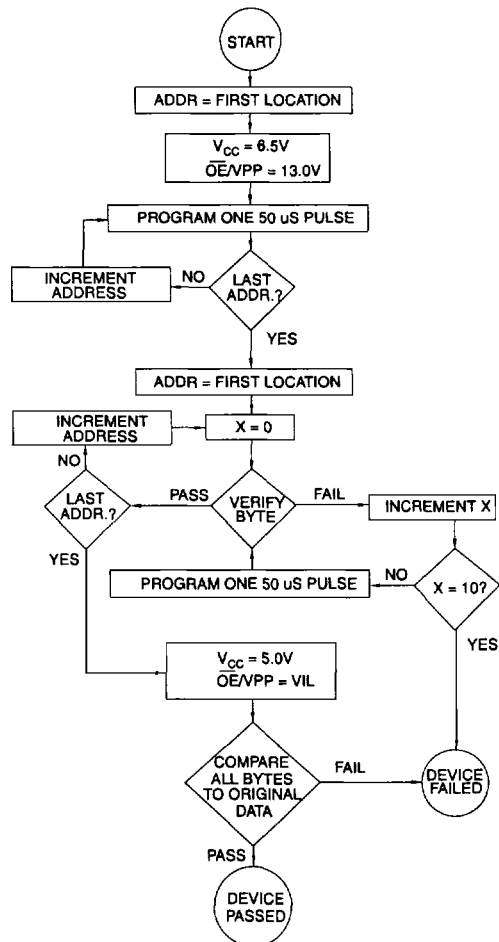
## Ordering Information

| tACC | ICC (mA) | | Ordering Code | Package | Operation Range |
|------|----------|---------|---------------|---------|-----------------|
| (ns) | Active | Standby | | | |
| 100 | 40 | 0.1 | AT27C080-10DC<br>AT27C080-10PC<br>AT27C080-10RC<br>AT27C080-10TC | 32DW6<br>32P6<br>32R<br>32T | Commercial<br>(0°C to 70°C) |
| 120 | 40 | 0.1 | AT27C080-12DC<br>AT27C080-12PC<br>AT27C080-12RC<br>AT27C080-12TC | 32DW6<br>32P6<br>32R<br>32T | Commercial<br>(0°C to 70°C) |
| | 40 | 0.1 | AT27C080-12DI<br>AT27C080-12PI<br>AT27C080-12RI<br>AT27C080-12TI | 32DW6<br>32P6<br>32R<br>32T | Industrial<br>(-40°C to 85°C) |
| 150 | 40 | 0.1 | AT27C080-15DC<br>AT27C080-15PC<br>AT27C080-15RC<br>AT27C080-15TC | 32DW6<br>32P6<br>32R<br>32T | Commercial<br>(0°C to 70°C) |
| | 40 | 0.1 | AT27C080-15DI<br>AT27C080-15PI<br>AT27C080-15RI<br>AT27C080-15TI | 32DW6<br>32P6<br>32R<br>32T | Industrial<br>(-40°C to 85°C) |

| Package Type | |
|--------------|--|
| 32DW6 | 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip) |
| 32P6 | 32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| 32R | 32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline (SOIC) |
| 32T | 32 Lead, Plastic Thin Small Outline Package (TSOP) |

**AT27C080**