SMALL-OUTLINE SYNCFLASH® MODULE

MT8LSFT3232(R)H, MT8LSFT3264(R)H, MT8LSFT32128(R)H

For the latest data sheet, please refer to the Micron Web-site: www.micron.com/syncflash

FEATURES

- PC100 and PC133 SDRAM-compatible read timing
- JEDEC-standard form factor, 144-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 133 MHz SyncFlash/SDRAM components
- Unbuffered
- 32MB (4 Meg x 64) SyncFlash memory + 32MB, 64MB, or 128MB SDRAM
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access
- Programmable burst lengths
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Package: 144-pin SODIMM (gold)

OPTIONS — MARKING

- On-board reset controller — R
- Frequency/CAS Latency
  - 133 MHz/CL = 2 — -13E
  - 133 MHz/CL = 3 — -133

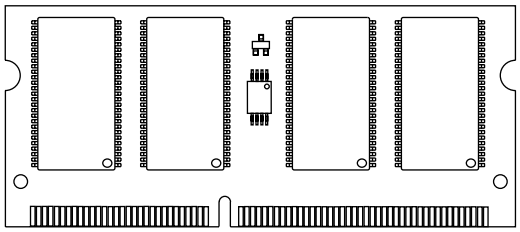
Timing Parameters

MODULE MARKING	PC133 (CL - ^{t}RCD - ^{t}RP)	PC100 (CL - ^{t}RCD - ^{t}RP)
-13E	2 - 3 - 2	2 - 3 - 2
-133	3 - 4 - 3	2 - 3 - 2

Address Table

	32MB SYNCFLASH		
	32MB SDRAM	64MB SDRAM	128MB SDRAM
Refresh Count	4K	4K	8K
Device Banks	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	4 Meg x 16	8 Meg x 16	16 Meg x 16
Row Addressing	4K (A0–A11)	4K (A0–A11)	8K (A0–A12)
Column Addressing	256 (A0–A7)	512 (A0–A8)	512 (A0–A8)

144-Pin Small-Outline DIMM



Part Numbers

PART NUMBER[1, 2]	CONFIG.[3]	VERSION
MT8LSFT3232(R)H-13E__	32MB SDRAM	133 MHz, CL = 2
MT8LSFT3232(R)H-133__	32MB SDRAM	133 MHz, CL = 3
MT8LSFT3264(R)H-13E__	64MB SDRAM	133 MHz, CL = 2
MT8LSFT3264(R)H-133__	64MB SDRAM	133 MHz, CL = 3
MT8LSFT32128(R)H-13E__	128MB SDRAM	133 MHz, CL = 2
MT8LSFT32128(R)H-133__	128MB SDRAM	133 MHz, CL = 3

NOTE:

1. (R) specifies on-board reset controller.
2. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8LSFT32128(R)H-13EA1.
3. All modules have 32MB SyncFlash.

GENERAL DESCRIPTION

The MT8LSFT3232(R)H, MT8LSFT3264(R)H, and MT8LSFT32128(R)H are SyncFlash/SDRAM-based memory modules organized in a x64 configuration. These modules use internally configured quad-bank SyncFlash/SDRAM devices with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0–CK1).

Read accesses to the SyncFlash/SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank,

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A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SyncFlash modules provide for programmable READ and WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page (SDRAM only), with a burst terminate option.

These SyncFlash/SDRAM modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access.

These modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs, and clocks are LVTTL-compatible.

SyncFlash modules offer substantial advances in Flash operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SyncFlash operation, refer to the 64Mb, x16 SyncFlash data sheet.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM.

These nonvolatile storage devices contain 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SyncFlash organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals.

SYNCFLASH INITIALIZATION OPTIONS

The SyncFlash device must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Initializing Module Without On-Board Reset Controller

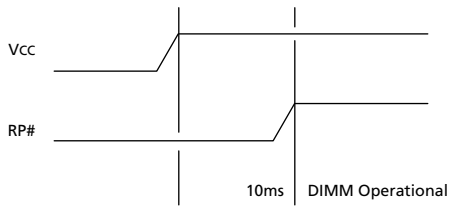
Systems that do not have an RP# signal can initialize SyncFlash memory through software. Using the INITIALIZE DEVICE command, the RP# pin does not require the LOW-to-HIGH transition that would otherwise be required for initialization. After the INITIALIZE DEVICE command has been issued, the power-up initialization process will complete within 100µs. Refer to the MT28S4M16B1LC data sheet for details on software command sequences.

For systems that have an RP# signal, RP# must be brought from LOW to HIGH. A 100µs delay is required after RP# transitions HIGH to complete internal device initialization.

Initializing Module with On-Board Reset Controller

For systems that do not have an RP# signal, an optional on-board reset controller is used to fully automate the reset of the SyncFlash devices after power-up. The RP# line is held LOW for 10ms after V_{DD} reaches 2.85V (see Figure 1). The SyncFlash devices will be ready for normal operation 100µs after the RP# line goes HIGH.

Figure 1:
On-Board Reset Operation



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Pin Assignment (Front View)

PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	2	VSS	73	RP#	74	CK1
3	DQ0	4	DQ32	75	VSS	76	VSS
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	VSS	92	VSS
21	VSS	22	VSS	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	VSS	36	VSS	107	VSS	108	VSS
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	VDD	46	VDD	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	VSS	120	VSS
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	VSS	56	VSS	127	DQ27	128	DQ59
57	NC	58	NC	129	VDD	130	VDD
59	NC	60	NC	131	DQ28	132	DQ60
61	CK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RAS#	66	CAS#	137	DQ31	138	DQ63
67	WE#	68	CKE1	139	VSS	140	VSS
69	S0#	70	A12	141	SDA	142	SCL
71	S1#	72	RFU (A13)	143	VDD	144	VDD

NOTE:

Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

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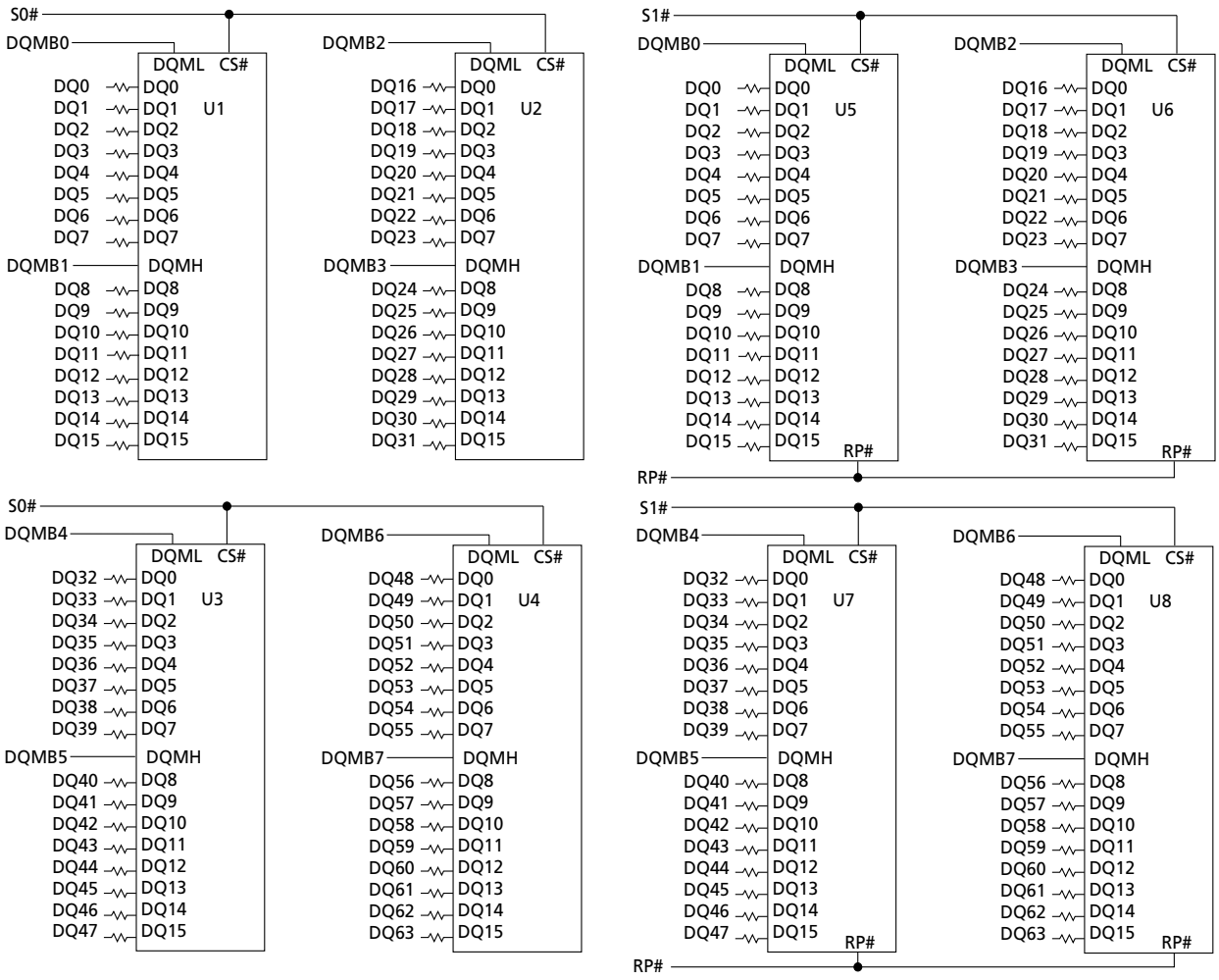
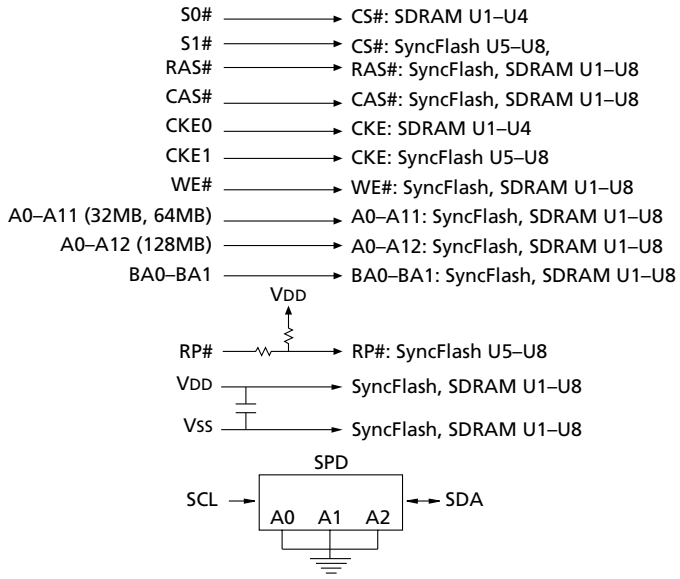
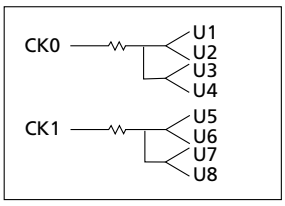
Functional Block Diagram
(32MB SyncFlash with 32MB/64MB/128MB SDRAM)







U1–U4 = MT48LC4M16A2TG SDRAM for 32MB
U1–U4 = MT48LC8M16A2TG SDRAM for 64MB
U1–U4 = MT48LC16M16A2TG SDRAM for 128MB
U5–U8 = MT28S4M16B1LCTG SyncFlash for 32MB

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Pin Descriptions

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
65–67	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S0#) define the command being entered.
61, 74	CK0, CK1	Input	Clock: CK0 and CK1 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
62, 68	CKE0, CKE1	Input	Clock Enable: CKE0 and CKE1 activate (HIGH) and deactivate (LOW) the CK0–CK1 signals. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE0 and CKE1 are synchronous except after the device enters power-down and self refresh modes, where CKE0 and CKE1 become asynchronous until after exiting the same mode. The input buffers, including CK0–CK1, are disabled during power-down and self refresh modes, providing low standby power.
69, 71	S0#, S1#	Input	Chip Select: S0# and S1# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0# and S1# are registered HIGH. S0# and S1# are considered part of the command code.
23–26, 115–118	DQMB0–DQMB7	Input	Input Mask: DQMB is an input mask signal for write accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
106, 110	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 is also used to program the twelfth bit of the mode register.
29–34, 103–105, 109, 111, 112, 70 (128MB)	A0–A11 (32MB, 64MB) A0–A12 (128MB)	Input	Address Inputs: A0–A11/A12 are sampled during the ACTIVE command (row address A0–A11/A12) and READ WRITE command (column address A0–A7/A8), to select one location out of the memory array in the respective bank. The address inputs provide the op-code during LOAD MODE REGISTER command and the operation code during a LOAD COMMAND REGISTER command.
142	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
73	RP#	Input	Device Initialize: RP# must be held HIGH during normal operation (not RESET). When RP# = V_{HH}, all protection modes are ignored during PROGRAM and ERASE.
3–10, 13–20, 37–44, 47–54, 83–90, 93–100, 121–128, 131–138	DQ0–DQ63	Input/ Output	Data I/Os: Data bus.
141	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
11, 12, 27, 28, 45, 46, 63, 64, 81, 82, 101, 102, 113, 114, 129, 130, 143, 144	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.

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Pin Descriptions (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 2, 21, 22, 35, 36, 55, 56, 75, 76, 91, 92, 107,108, 119, 120, 139, 140	Vss	Supply	Ground.
57, 58, 59, 60, 77, 78, 79, 80	NC	No Connect	These pins should be left unconnected.
72	RFU	–	Reserved for Future Use: This pin should be left unconnected.

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SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 2 and 3).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 4).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode, the SPD device will transmit eight bits of data, release the SDA line, and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 2:
Data Validity

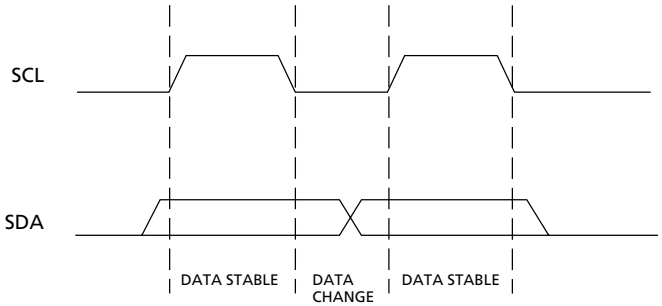


Figure 3:
Definition of Start and Stop

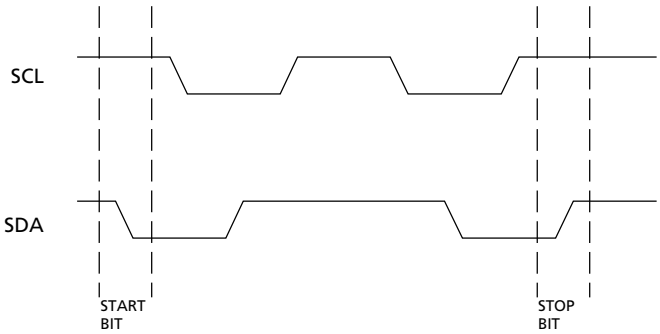
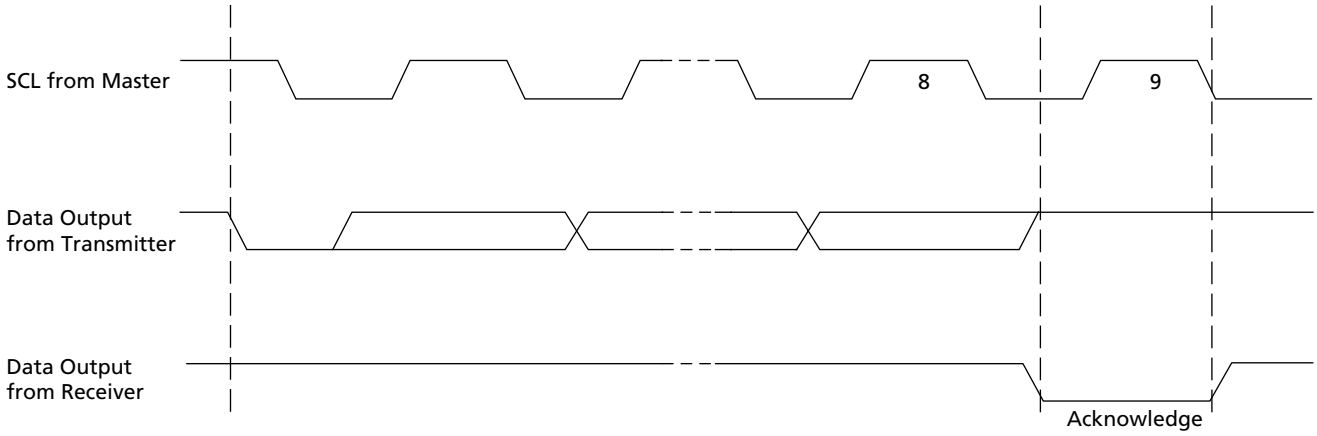


Figure 4:
Acknowledge Response From Receiver



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Serial Presence-Detect Matrix

(Notes: 1, 2)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8LSFT[3]
0	NUMBER OF BYTES USED BY MICRON	128	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	08
2	MEMORY TYPE	SYNCFLASH + SDRAM	24
3	SYNCFLASH/SDRAM NUMBER OF ROW ADDRESSES	32MB/32MB 32MB/64MB 32MB/128MB	0C CC CD
4	SYNCFLASH/SDRAM NUMBER OF COLUMN ADDRESSES	32MB/32MB 32MB/64MB 32MB/128MB	08 89 89
5	NUMBER OF MODULE BANKS	2	02
6	MODULE DATA WIDTH	64	40
7	MODULE DATA WIDTH (continued)	0	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL	01
9	SYNCFLASH/SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 3)	7 (-13E) 7.5 (-133)	70 75
10	SYNCFLASH/SDRAM ACCESS FROM CLOCK, ^{t}AC (CAS LATENCY = 3)	5.4(-13E/-133)	54
11	MODULE CONFIGURATION TYPE	NONPARITY	00
12	SDRAM REFRESH RATE/TYPE	15.6µs/SELF 7.81µs/SELF (128MB)	80 82
13	SDRAM DEVICE WIDTH	16	10
14	ERROR-CHECKING SYNCFLASH DATA WIDTH	NONE	00
15	MINIMUM CLOCK DELAY, ^{t}CCD	1	01
16	SYNCFLASH/SDRAM BURST LENGTHS SUPPORTED (READ ONLY)	1, 2, 4, 8, PAGE	8F
17	NUMBER OF BANKS ON SYNCFLASH/SDRAM DEVICE	4	04
18	CAS LATENCIES SUPPORTED	2, 3	06
19	CS LATENCY	0	01
20	WE LATENCY	0	01
21	SYNCFLASH/SDRAM MODULE ATTRIBUTES	UNBUFFERED	00
22	SYNCFLASH/SDRAM DEVICE ATTRIBUTES: GENERAL	0E	0E
23	SYNCFLASH/SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 2)	7.5 (-13E) 10 (-133)	75 A0
24	SYNCFLASH/SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 2)	5.4 (-13E) 6 (-133)	54 60
25	SYNCFLASH/SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 1)	–	00
26	SYNCFLASH/SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 1)	–	00
27	SDRAM: MINIMUM ROW PRECHARGE TIME, ^{t}RP	15 (-13E) 20 (-133)	0F 14
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, ^{t}RRD	14 (-13E) 15 (-133)	0E 0F
29	MINIMUM RAS# TO CAS# DELAY, ^{t}RCD	22 (-13E) 25 (-133)	16 19

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Serial Presence-Detect Matrix (continued)

(Notes: 1, 2)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8LSFT[3]
30	MINIMUM RAS# PULSE WIDTH, ^{t}RAS	45 (-13E) 45 (-133)	2D 2D
31	DENSITY OF EACH BANK ON MODULE	32MB/32MB 64MB/32MB 128MB/32MB	08 18 28
32	COMMAND AND ADDRESS SETUP TIME	1.5 (-13E/-133)	15
33	COMMAND AND ADDRESS HOLD TIME	0.8 (-13E/-133)	08
34	DATA SIGNAL INPUT SETUP TIME	1.5 (-13E/-133)	15
35	DATA SIGNAL INPUT HOLD TIME	0.8 (-13E/-133)	08
36–61	RESERVED	–	00
62	SPD REVISION	1.2 (-13E/-133)	12
63	CHECKSUM FOR BYTES 0–62	-13E -133	TBD
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C
65–71	MANUFACTURER'S JEDEC ID CODE (CONT.)	–	00
72	MANUFACTURING LOCATION	–	01 02 03 04 05 06
73–90	MODULE PART NUMBER (ASCII)	–	x
91	PCB IDENTIFICATION CODE	1 2 3 4	01 02 03 04
92	IDENTIFICATION CODE (CONT.)	0	00
93	YEAR OF MANUFACTURE IN BCD	–	00
94	WEEK OF MANUFACTURE IN BCD	–	00
95–98	MODULE SERIAL NUMBER	x	00
99	MEMORY MIX[4]	SDRAM + SYNCFLASH	02
100–125	MANUFACTURER-SPECIFIC DATA (RSVD)	–	00
126	SYSTEM FREQUENCY	100 MHz/ 133 MHz	64
127	SYNCFLASH/SDRAM COMPONENT AND CLOCK DETAIL	CF	CF

NOTE:

1. "1"/"0": serial data, "driven to HIGH"/"driven to LOW."
2. x = variable data.
3. Values are in hexadecimal.
4. DIMM memory mix: 0 (bank 0 = SyncFlash, bank 1 = Unpopulated); 1 (bank 0 = SyncFlash, bank 1 = SyncFlash); 2 (bank 0 = SDRAM, bank 1 = SyncFlash).

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COMMANDS

Truth Table 1 provides a quick reference of available commands for SDRAM-compatible operation. For a more detailed description of commands and operations, refer to the SyncFlash and SDRAM data sheets.

TRUTH TABLE 1
SDRAM-Compatible Interface Commands and DQM Operation

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQS	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/ Row	X	2
READ (Select bank, column, and start READ burst)	L	H	L	H	X	Bank/ Col	X	3
WRITE (Select bank, column, and start WRITE)	L	H	L	L	X	Bank/ Col	Valid	3, 4
BURST TERMINATE	L	H	H	L	X	X	Active	
ACTIVE TERMINATE/PRECHARGE	L	L	H	L	X	X	X	5
LOAD COMMAND REGISTER/REFRESH	L	L	L	H	X	Com- Code	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op- Code	X	8
Write Enable/Output Enable	–	–	–	–	L	–	Active	9
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	9

NOTE:

1. CKE is HIGH for all commands shown.
2. A0–A11 provide row address, and BA0 and BA1 determine which bank is made active.
3. A0–A7 provide column address, and BA0 and BA1 determine which bank is being read from or written to.
4. A PROGRAM SETUP command sequence (see MT28S4M16B1LC data sheet) must be completed prior to executing a WRITE.
5. ACTIVE TERMINATE is functionally equivalent to the SDRAM PRECHARGE command; however, PRECHARGE (deactivate row in bank or banks) is not required for SyncFlash memory.
   A10 LOW: BA0 and BA1 determine the bank to be active terminated.
   A10 HIGH: All banks are active terminated and BA0 and BA1 are "Don't Care."
6. A0–A7 define the com-code, and A8–A11 are "Don't Care" for this operation. See MT28S4M16B1LC data sheet.
7. LOAD COMMAND REGISTER (LCR) replaces the SDRAM auto refresh or self refresh mode, which is not required for SyncFlash memory. See MT28S4M16B1LC data sheet.
8. A0–A11 define the op-code written to the mode register. The mode register can be dynamically loaded each cycle, provided ^{t}MRD is satisfied. The default mode register value is stored in the nvmode register. The contents of the nvmode register are automatically loaded into the mode register during device initialization.
9. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

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Figure 5: Mode Register Definition

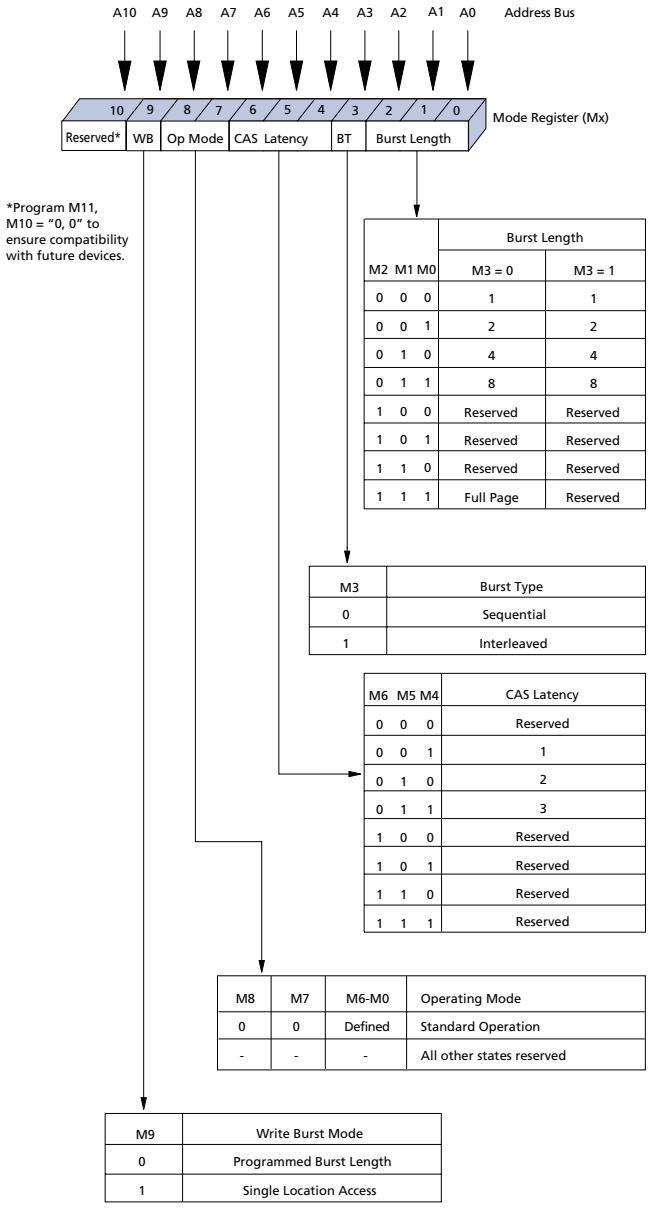

Table 1: Burst Definition Table

BURST LENGTH	STARTING COLUMN ADDRESS	ORDER OF ACCESSES WITHIN A BURST	
		TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full page (y)	n = A0–A7 (location 0–y)	Cn, Cn+1, Cn+2 Cn+3, Cn+4... ...Cn-1, Cn...	Not supported

NOTE:

1. For a burst length of two, A1–A7 select the block-of-two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2–A7 select the block-of-four burst; A0–A1 select the starting column within the block.
3. For a burst length of eight, A3–A7 select the block-of-eight burst; A0–A2 select the starting column within the block.
4. For a full-page burst, the full row is selected and A0–A7 select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. For a burst length of one, A0–A7 select the unique column to be accessed, and mode register bit M3 is ignored.
7. Burst write of 1, 2, 4, or 8 Dwords is supported (not full page).
8. The contents of the mode register can be read using the READ DEVICE CONFIGURATION command (004h).

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ABSOLUTE MAXIMUM RATINGS*

Voltage on RP# Relative to V_{SS} ..... -1V to +9V
Voltage on V_{DD} Supply Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 8W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 2) V_{DD} = +3.3V ±0.3V

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	3
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	-0.3	0.8	V	3
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	CK0, CK1, S0#, S1#, CKE0, CKE1	I_{I1}	-20	20	µA	4
	RAS#, CAS#, WE#, BA0, BA1, A0–A11	I_{I2}	-40	40	µA	
	DQMB0–DQMB7	I_{I3}	-5	5	µA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DD}	DQ0–DQ63	I_{OZ}	-40	40	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)		V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)		V_{OL}	–	0.4	V	
HARDWARE PROTECT VOLTAGE (RP# only)		V_{HH}	7.0	8.5	V	

NOTE:

1. All voltages referenced to V_{SS}.
2. An initial pause of 100µs is required after power-up.
3. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one-third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one-third of the cycle rate.
4. CK0 = 20µA.

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IDD Specifications and Conditions (SyncFlash)

(Notes: 1, 2, 3; notes appear following the parameter tables);
Commercial Temperature ($0°C \le T_A \le +70°C$); V_{DD} = +3.3V ±0.3V

PARAMETER/CONDITION	SYMBOL	MAX		UNITS	NOTES
		-13E	-133		
OPERATING CURRENT: Active Mode; Burst = 2; READ; tRC = tRC (MIN); CAS latency = 3	IDDR1	500	480	mA	4, 5, 6
OPERATING CURRENT: Burst Mode; Continuous Burst; All banks active; READ; CAS latency = 3	IDDR2	320	280	mA	4, 5, 6
STANDBY CURRENT: Active Mode; CS# = HIGH; CKE = LOW; All banks active; No burst in progress	IDDS1	200	200	mA	
STANDBY CURRENT: Power-Down Mode; CKE = LOW; No burst in progress	IDDS2	8	8	mA	
DEEP POWER-DOWN CURRENT: RP# = VSS ±0.2V	IDDDP	400	400	µA	
PROGRAM CURRENT	IDDW	240	240	mA	
ERASE CURRENT	IDDE	320	320	mA	

IDD Specifications and Conditions* (32MB SDRAM)

(Notes: 1, 15, 16, 17, 18; notes appear following the parameter tables); V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V

PARAMETER/CONDITION		SYMBOL	MAX		UNITS	NOTES
			-13E	-133		
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; tRC = tRC (MIN)		IDD1[a]	500	460	mA	8, 11, 12, 13
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW		IDD2[b]	8	8	mA	13
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after tRCD met; No accesses in progress		IDD3[a]	180	180	mA	8, 11, 12, 13
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active		IDD4[a]	600	560	mA	8, 11, 12, 13
AUTO REFRESH CURRENT	tRFC = tRFC (MIN)	IDD5[b]	920	840	mA	8, 10, 11, 12, 13, 14
CS# = HIGH; CKE = HIGH	tRFC = 15.625µs	IDD6[b]	12	12	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD7[b]	4	4	mA	9

*DRAM components only.
a - Value calculated as one module bank in this operating condition, and all other module banks in power-down mode.
b - Value calculated reflects all module banks in this operating condition.

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IDD Specifications and Conditons* (64MB SDRAM)

(Notes: 1, 15, 16, 17, 18; notes appear following the parameter tables); VDD, VDDQ = +3.3V ±0.3V

PARAMETER/CONDITION		SYMBOL	MAX		UNITS	NOTES
			-13E	-133		
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		IDD1[a]	508	468	mA	8, 11, 12, 13
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW		IDD2[b]	8	8	mA	13
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		IDD3[a]	188	188	mA	8, 11, 12, 13
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active		IDD4[a]	608	568	mA	8, 11, 12, 13
AUTO REFRESH CURRENT CS# = HIGH; CKE = HIGH	^{t}RFC = ^{t}RFC (MIN)	IDD5[b]	920	840	mA	8, 10, 11, 12, 13, 14
	^{t}RFC = 15.625µs	IDD6[b]	12	12	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD7[b]	4	4	mA	9

IDD Specifications and Conditons* (128MB SDRAM)

(Notes: 1, 15, 16, 17, 18; notes appear following the parameter tables); VDD, VDDQ = +3.3V ±0.3V

PARAMETER/CONDITION		SYMBOL	MAX		UNITS	NOTES
			-13E	-133		
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		IDD1[a]	648	608	mA	8, 11, 12, 13
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW		IDD2[b]	8	8	mA	13
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		IDD3[a]	208	208	mA	8, 11, 12, 13
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active		IDD4[a]	668	608	mA	8, 11, 12, 13
AUTO REFRESH CURRENT	^{t}RFC = ^{t}RFC (MIN)	IDD5[b]	1320	1240	mA	8, 10, 11, 12, 13, 14
CS# = HIGH; CKE = HIGH	^{t}RFC = 7.8µs	IDD6[b]	12	12	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD7[b]	8	8	mA	9

*DRAM components only.
a - Value calculated as one module bank in this operating condition, and all other module banks in power-down mode.
b - Value calculated reflects all module banks in this operating condition. .

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Capacitance

PARAMETER	SYMBOL	-13E		-133		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Input Capacitance: S0#, S1#, CKE0, CKE1, CK0, CK1	C_{I1}	22	34	22	34	pF	7
Input Capacitance: All other input-only pins	C_{I2}	12	18	12	18	pF	7
Input Capacitance: DQMB0#–DQMB7#	C_{I3}	7	10	4	6	pF	7
Input/Output Capacitance: DQ0–DQ63	C_{IO1}	10	15	6	8	pF	7

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SYNCFLASH/SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 19–22; notes appear following the parameter tables)
Commercial Temperature (0°C ≤ T_A ≤ +70°C); V_{DD} = +3.3V ±0.3V

AC CHARACTERISTICS			-13E		-133			
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from CLK (positive edge)	CL = 3	^tAC		5.4		5.4	ns	
	CL = 2	^tAC		5.4		6	ns	
Address hold time		^tAH	0.8		0.8		ns	
Address setup time		^tAS	1.5		1.5		ns	
CLK high-level width		^tCH	2.5		2.5		ns	
CLK low-level width		^tCL	2.5		2.5		ns	
Clock cycle time	CL = 3	^tCK	7		7.5		ns	24
	CL = 2	^tCK	7.5		10		ns	24
CKE hold time		^tCKH	0.8		0.8		ns	
CKE setup time		^tCKS	1.5		1.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8		0.8		ns	23
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		1.5		ns	23
Data-in hold time		^tDH	0.8		0.8		ns	
Data-in setup time		^tDS	1.5		1.5		ns	
Data-out High-Z time	CL = 3	^tHZ		5.4		5.4	ns	25
	CL = 2	^tHZ		5.4		6	ns	25
Data-out Low-Z time		^tLZ	1		1		ns	
Data-out hold time (load)		^tOH	3		3		ns	
Data-out hold time (no load)		^tOHN	1.8		1.8		ns	26
ACTIVE to ACTIVE command period		^tRC	60		66		ns	
ACTIVE to READ or WRITE delay		^tRCD	22.5		25		ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	14		15		ns	
Transition time		^tT	0.3	1.2	0.3	1.2	ns	27

SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 19–22; notes appear following the parameter tables)
Commercial Temperature (0°C ≤ T_A ≤ +70°C); V_{DD} = +3.3V ±0.3V

AC CHARACTERISTICS		-13E		-133			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
ACTIVE to PRECHARGE command	^tRAS	37	120,000	44	120,000	ns	
ACTIVE to READ or WRITE delay	^tRCD	15		20		ns	
Refresh period (4,096 and 8,192 rows)	^tREF		64		64	ns	
AUTO REFRESH period	^tRFC	66		66		ns	
PRECHARGE command period	^tRP	15		20		ns	28
WRITE recovery time	^tWR	1 CK + 7.5ns		1 CK + 7.5ns		–	
		14		15			
Exit SELF REFRESH to ACTIVE command	^tXSR	67		75		ns	29

*Specifications for the SyncFlash/SDRAM components used on the module.

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SYNCFLASH/SDRAM AC FUNCTIONAL CHARACTERISTICS

(Notes: 19–22; notes appear following the parameter tables)
Commercial Temperature (0°C ≤ T_A ≤ +70°C); V_{DD} = +3.3V ±0.3V

PARAMETER	SYMBOL	-13E	-133	UNITS	NOTES
READ/WRITE command to READ/LOAD COMMAND REGISTER	^tCCD	1	1	^tCK	30
CKE to clock disable or power-down entry mode	^tCKED	1	1	^tCK	31
CKE to clock enable or power-down exit setup mode	^tPED	1	1	^tCK	30
DQM to input data delay	^tDQD	0	0	^tCK	30
DQM to data mask during WRITEs	^tDQM	0	0	^tCK	30
DQM to data High-Z during READs	^tDQZ	2	2	^tCK	32
WRITE command to input data delay	^tDWD	0	0	^tCK	30
Data-in to ACTIVE command	^tDAL	4	5	^tCK	33
Data-in to ACTIVE TERMINATE command	^tDPL	2	2	^tCK	33
LOAD MODE REGISTER command to ACTIVE command	^tMRD	2	2	^tCK	
Last data-in to ACTIVE TERMINATE command	^tRDL	2	2	^tCK	33

SDRAM AC FUNCTIONAL CHARACTERISTICS

(Notes: 19–22; notes appear following the parameter tables)
Commercial Temperature (0°C ≤ T_A ≤ +70°C); V_{DD} = +3.3V ±0.3V

PARAMETER		SYMBOL	-13E	-133	UNITS
Last data-in to burst STOP command		^tBDL	4	5	^tCK
Last data-in to new READ/WRITE command		^tCDL	2	2	^tCK
Data-out to high-impedance from PRECHARGE command	CL = 3	$^tROH(3)$	2	2	^tCK
	CL = 2	$^tROH(2)$	2	2	^tCK

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SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Note: 1) V_{DD} = +3.3V ±0.3V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DD}	3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Note: 1) V_{DD} = +3.3V ±0.3V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	4		µs	
Clock HIGH period	$^{t}HIGH$	4		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	$^{t}SU:DAT$	250		ns	
Start condition setup time	$^{t}SU:STA$	4.7		µs	
Stop condition setup time	$^{t}SU:STO$	4.7		µs	
WRITE cycle time	^{t}WRC		10	ms	34

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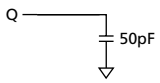
NOTES

1. All voltages referenced to V_{SS}.
2. An initial pause of 200ms is required after power-up. (V_{CC} and $V_{CC}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.)
3. I_{DD} specifications are tested after the device is properly initialized.
4. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. The I_{DD} current will decrease as the CAS latency is reduced. This is because the maximum cycle rate is slower as the CAS latency is reduced.
6. Address transitions average one transition every 30ns.
7. This parameter is sampled. $V_{CC} = V_{CC}Q$; f = 1 MHz, $T_A = +25^{\circ}C$.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with mininum cycle time and the outputs open.
9. Enables on-chip refresh and address counters.
10. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
11. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
12. Address transitions average one transition every two clocks.
13. For -13E, CL = 2 and ^{t}CK = 7.5ns; for -133, CL = 3 and ^{t}CK = 7.5ns.
14. CKE is HIGH during refresh command period ^{t}RFC (MIN), else CKE is LOW. The $I_{DD}6$ limit is actually a nominal value and does not result in a fail value.
15. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured ($0^{\circ}C \le T_A \le +70^{\circ}C$ for commercial).
16. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at the same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
17. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the ISV crossover point. Refer to Technical Note, TN-48-09, "LVTTL Derating for SDRAM Slew Rate Violations," for additional information on SDRAM timing.
18. I_{DD} specifications are tested after the device is properly initialized.
19. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}C \le T_A \le +70^{\circ}C$) is ensured.
20. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
21. Outputs measured at 1.5V with equivalent load:



22. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point.
23. 3ns < ^{t}PDL < 5ns.
24. The clock frequency must remain constant during access or precharge states (READ and WRITE commands). CKE may be used to reduce the data rate.
25. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
26. Parameter guaranteed by design.
27. AC characteristics assume ^{t}T = 1ns.
28. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 7.5ns/7ns after the first clock delay, after the last WRITE is executed.
29. CLK must be toggled a minimum of two times during this period.
30. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
31. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
32. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
33. Based on ^{t}CK = 133 MHz.
34. Timing actually specified by ^{t}WR.

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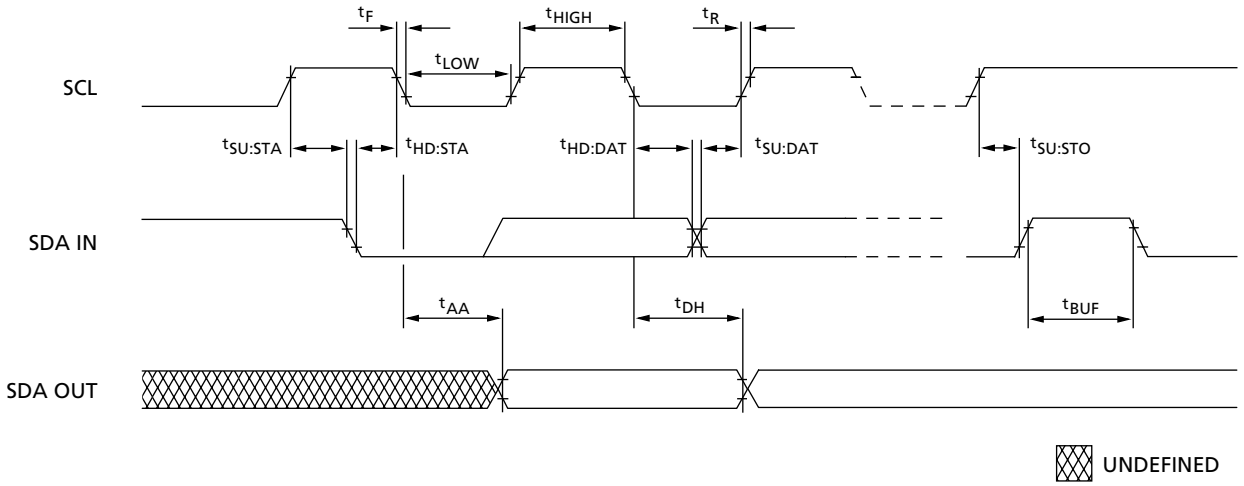
SPD EEPROM Timing Diagram



Serial Presence-Detect Timing Parameters

SYMBOL	MIN	MAX	UNITS
^{t}AA	0.3	3.5	µs
^{t}BUF	4.7		µs
^{t}DH	300		ns
^{t}F		300	ns
^{t}HD:DAT	0		µs
^{t}HD:STA	4		µs

Serial Presence-Detect Timing Parameters

SYMBOL	MIN	MAX	UNITS
^{t}HIGH	4		µs
^{t}LOW	4.7		µs
^{t}R		1	µs
^{t}SU:DAT	250		ns
^{t}SU:STA	4.7		µs
^{t}SU:STO	4.7		µs

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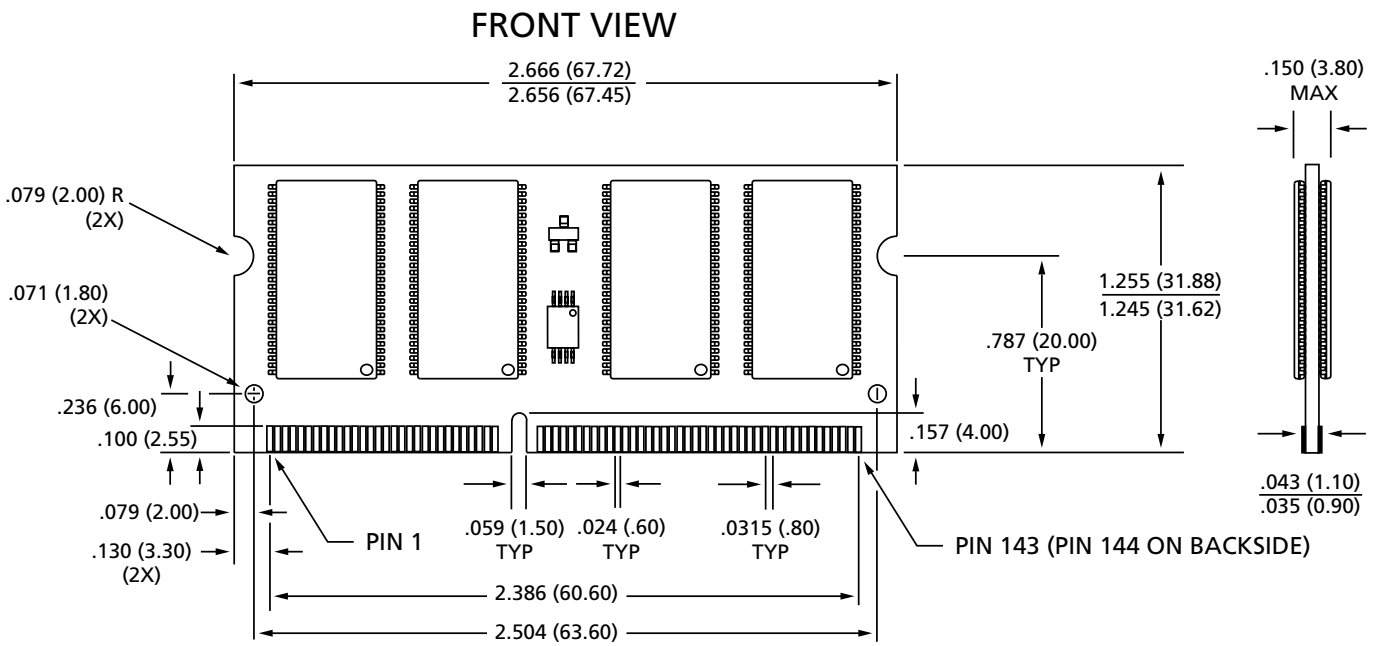
144-PIN SODIMM
(32MB SyncFlash/32MB, 64MB, 128MB SDRAM)



NOTE:

All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

DATA SHEET DESIGNATION

Advance: This datasheet contains initial descriptions of products still under development.

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REVISION HISTORY

- Rev. 3, Advance 8/02
  Changed Timing Parameters ^{t}RCD
  Updated the Serial Presence-Detect Matrix

- Rev. 2, Advance 5/02
  Updated General Description and Initializing Module with On-Board Reset Controller text
  Updated RP# text in Pin Description table

- Original document, Rev. 1, Advance 4/02

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