CMOS single-chip 8-bit microcontrollers   80C32/87C52

DESCRIPTION

The Philips 80C32/87C52 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

The 87C52 contains an 8k × 8 EPROM and the 80C32 is ROMless. Both contain a 256 × 8 RAM, 32 I/O lines, three 16-bit counter/timers, a six-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.
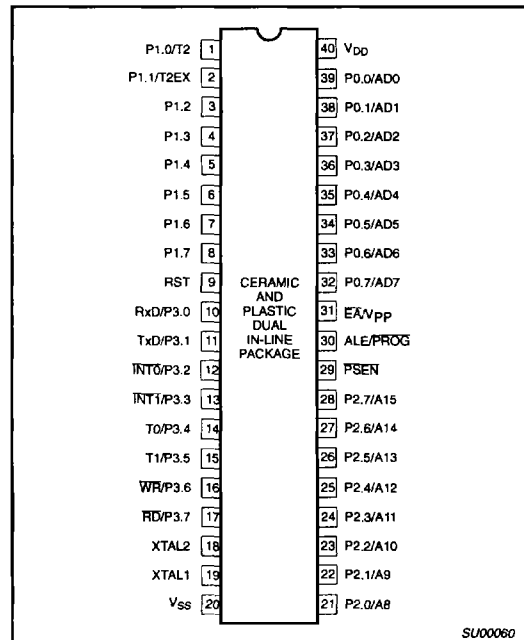
In addition, the 80C32/87C52 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

See 80C52/80C54/80C58 datasheet for ROM device specifications.

FEATURES

- 80C51 based architecture
- 8032 compatible
  - 8k × 8 EPROM (87C52)
  - ROMless (80C32)
  - 256 × 8 RAM
  - Three 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Three speed ranges:
  - 3.5 to 16MHz
  - 3.5 to 24MHz
  - 3.5 to 33MHz
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATIONS

Pin			Pin
P1.0/T2	1	40	V_{DD}
P1.1/T2EX	2	39	P0.0/AD0
P1.2	3	38	P0.1/AD1
P1.3	4	37	P0.2/AD2
P1.4	5	36	P0.3/AD3
P1.5	6	35	P0.4/AD4
P1.6	7	34	P0.5/AD5
P1.7	8	33	P0.6/AD6
RST	9	32	P0.7/AD7
RxD/P3.0	10	31	$E\overline{A}/V_{PP}$
TxD/P3.1	11	30	ALE/$\overline{PROG}$
$\overline{INT0}$/P3.2	12	29	$\overline{PSEN}$
$\overline{INT1}$/P3.3	13	28	P2.7/A15
T0/P3.4	14	27	P2.6/A14
T1/P3.5	15	26	P2.5/A13
$\overline{WR}$/P3.6	16	25	P2.4/A12
$\overline{RD}$/P3.7	17	24	P2.3/A11
XTAL2	18	23	P2.2/A10
XTAL1	19	22	P2.1/A9
V_{SS}	20	21	P2.0/A8

CERAMIC AND PLASTIC DUAL IN-LINE PACKAGE

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ORDERING INFORMATION

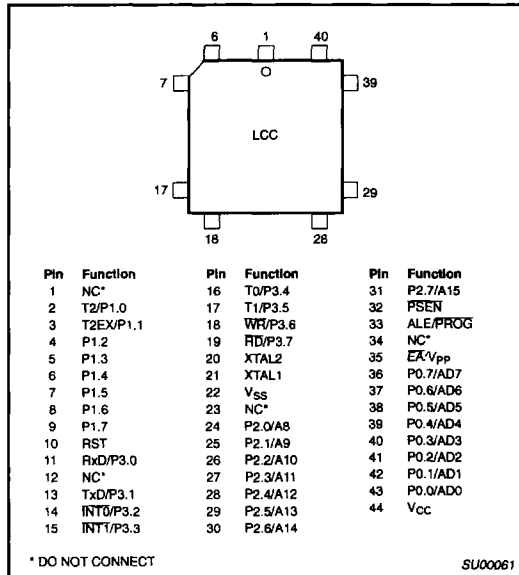| ROMless	EPROM[1]		TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz	DRAWING NUMBER
P80C32EBP N	P87C52EBP N	OTP	0 to +70, Plastic Dual In-line Package	16	SOT129-1
P80C32EBA A	P87C52EBA A	OTP	0 to +70, Plastic Leaded Chip Carrier	16	SOT187-2
	P87C52EBF FA	UV	0 to +70, Ceramic Dual In-line Package	16	0590B
	P87C52EBL KA	UV	0 to +70, Ceramic Leaded Chip Carrier	16	1472A
P80C32EBB B	P87C52EBB B	OTP	0 to +70, Plastic Quad Flat Pack	16	SOT307-2
P80C32EFP N	P87C52EFP N	OTP	−40 to +85, Plastic Dual In-line Package	16	SOT129-1
P80C32EFA A	P87C52EFA A	OTP	−40 to +85, Plastic Leaded Chip Carrier	16	SOT187-2
	P87C52EFF FA	UV	−40 to +85, Ceramic Dual In-line Package	16	0590B
P80C32EFB B	P87C52EFB B	OTP	−40 to +85, Plastic Quad Flat Pack	16	SOT307-2
P80C32IBP N	P87C52IBP N	OTP	0 to +70, Plastic Dual In-line Package	24	SOT129-1
P80C32IBA A	P87C52IBA A	OTP	0 to +70, Plastic Leaded Chip Carrier	24	SOT187-2
P80C32IBB B			0 to +70, Plastic Quad Flat Pack	24	SOT307-2
	P87C52IBF FA	UV	0 to +70, Ceramic Dual In-line Package	24	0590B
	P87C52IBL KA	UV	0 to +70, Ceramic Leaded Chip Carrier	24	1472A
P80C32IFP N	P87C52IFP N	OTP	−40 to +85, Plastic Dual In-line Package	24	SOT129-1
P80C32IFA A	P87C52IFA A	OTP	−40 to +85, Plastic Leaded Chip Carrier	24	SOT187-2
P80C32IFB B			−40 to +85, Plastic Quad Flat Pack	24	SOT307-2
	P87C52IFF FA	UV	−40 to +85, Ceramic Dual In-line Package	24	0590B
P80C32NBA A			0 to +70, Plastic Leaded Chip Carrier	33	SOT187-2
P80C32NBP N			0 to +70, Plastic Dual In-line Package	33	SOT129-1
P80C32NBB B			0 to +70, Plastic Quad Flat Pack	33	SOT307-2
P80C32NFA A			−40 to +85, Plastic Leaded Chip Carrier	33	SOT187-2
P80C32NFP N			−40 to +85, Plastic Dual In-line Package	33	SOT129-1
P80C32NFB B			−40 to +85, Plastic Quad Flat Pack	33	SOT307-2

NOTE:
1. OTP = One Time Programmable EPROM. UV = UV erasable EPROM
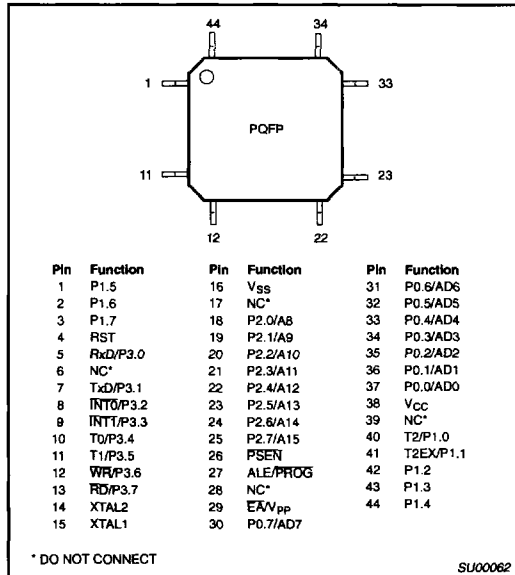2. For 33MHz ROM 80C52 operation, see 80C52/80C54/80C58 data sheet.
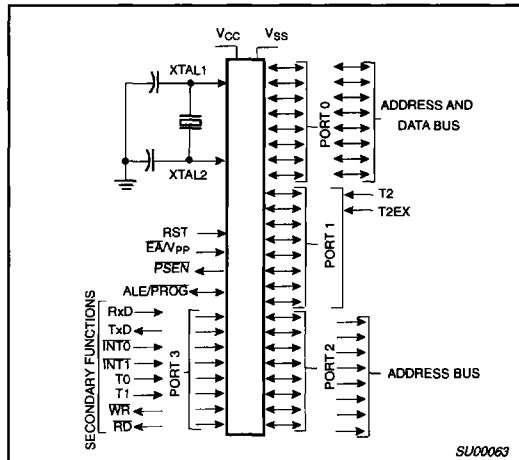
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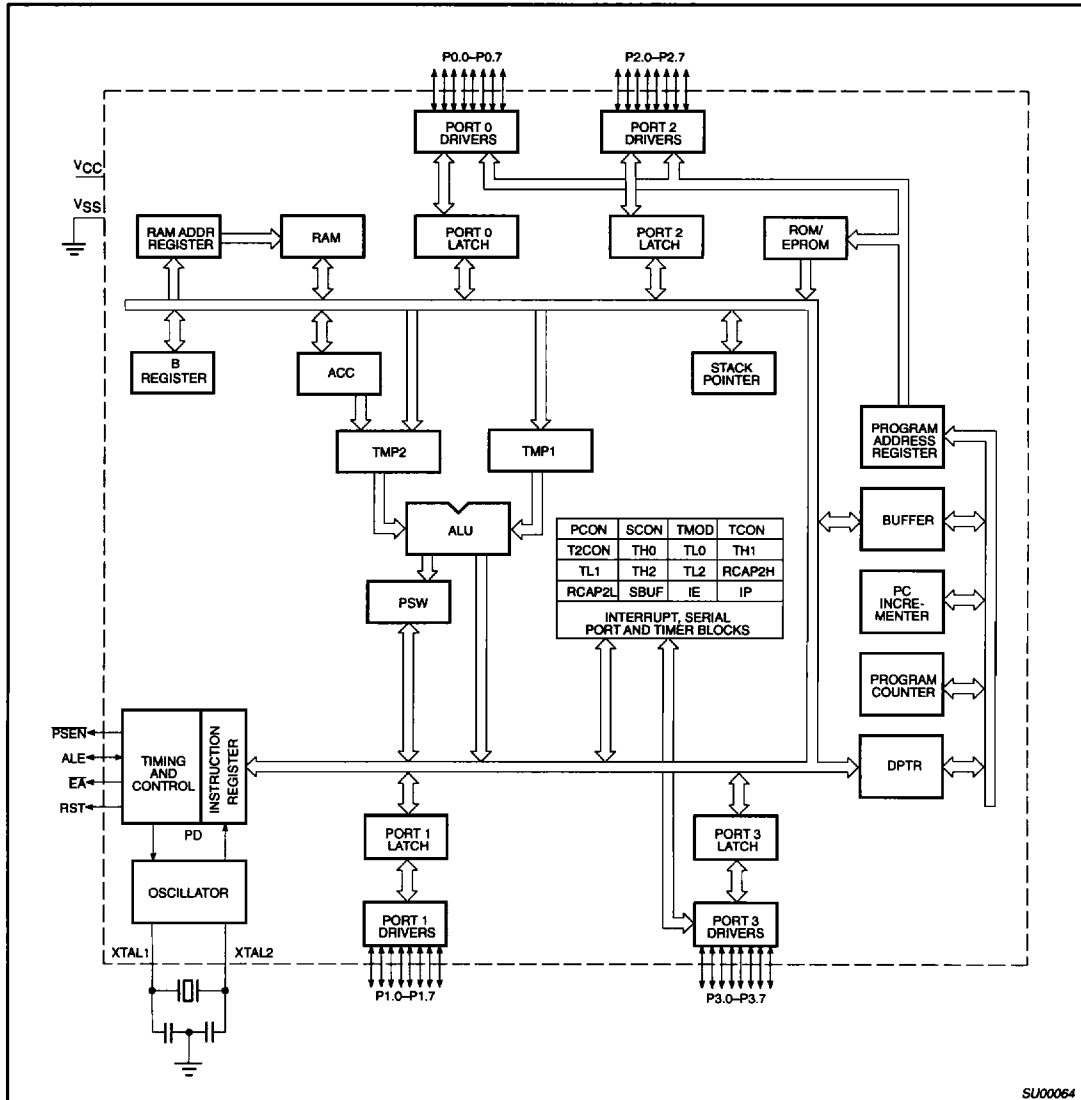## CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

Pin	Function	Pin	Function	Pin	Function
1	NC*	16	T0/P3.4	31	P2.7/A15
2	T2/P1.0	17	T1/P3.5	32	PSEN
3	T2EX/P1.1	18	WR/P3.6	33	ALE/PROG
4	P1.2	19	RD/P3.7	34	NC*
5	P1.3	20	XTAL2	35	EA/Vpp
6	P1.4	21	XTAL1	36	P0.7/AD7
7	P1.5	22	Vss	37	P0.6/AD6
8	P1.6	23	NC*	38	P0.5/AD5
9	P1.7	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	RxD/P3.0	26	P2.2/A10	41	P0.2/AD2
12	NC*	27	P2.3/A11	42	P0.1/AD1
13	TxD/P3.1	28	P2.4/A12	43	P0.0/AD0
14	INT0/P3.2	29	P2.5/A13	44	Vcc
15	INT1/P3.3	30	P2.6/A14		

* DO NOT CONNECT

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PLASTIC QUAD FLAT PACK PIN FUNCTIONS

Pin	Function	Pin	Function	Pin	Function
1	P1.5	16	Vss	31	P0.6/AD6
2	P1.6	17	NC*	32	P0.5/AD5
3	P1.7	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	RxD/P3.0	20	P2.2/A10	35	P0.2/AD2
6	NC*	21	P2.3/A11	36	P0.1/AD1
7	TxD/P3.1	22	P2.4/A12	37	P0.0/AD0
8	INT0/P3.2	23	P2.5/A13	38	Vcc
9	INT1/P3.3	24	P2.6/A14	39	NC*
10	T0/P3.4	25	P2.7/A15	40	T2/P1.0
11	T1/P3.5	26	PSEN	41	T2EX/P1.1
12	WR/P3.6	27	ALE/PROG	42	P1.2
13	RD/P3.7	28	NC*	43	P1.3
14	XTAL2	29	EA/Vpp	44	P1.4
15	XTAL1	30	P0.7/AD7		

* DO NOT CONNECT

SU00062

LOGIC SYMBOL

SU00063

BLOCK DIAGRAM

SU00064

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Table 1.   8XC52 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR: DPH DPL	Data pointer (2 bytes) Data pointer high Data pointer low	 83H 82H									 00H 00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt enable	A8H	EA	–	ET2	ES	ET1	EX1	ET0	EX0	0x000000B
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt priority	B8H	–	–	PT2	PS	PT1	PX1	PT0	PX0	xx000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	–	–	–	–	–	–	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	A15	A14	A13	A12	A11	A10	A9	A8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD	FFH
PCON[1]	Power control	87H	SMOD	–	–	–	GF1	GF0	PD	IDL	0xxxxxxxB
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
RCAP2H# RCAPL#	Capture high Capture low	CBH CAH									00H 00H
SBUF	Serial data buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial controller	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*#	Timer 2 control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00H
TH0 TH1 TH2# TL0 TL1 TL2#	Timer high 0 Timer high 1 Timer high 2 Timer low 0 Timer low 1 Timer low 2	8CH 8DH CDH 8AH 8BH CCH									00H 00H 00H 00H 00H 00H
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H

*   Bit addressable
\#   SFRs are modified from or added to the 80C51 SFRs.
1.   Bits GF1, GF0, PD, and IDL of the PCON register are not implemented in the NMOS 8XC52.

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PIN DESCRIPTION

MNEMONIC	PIN NO.			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
V_{SS}	20	22	16	I	**Ground:** 0V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C52. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Pins P1.0 and P1.1 also. Port 1 also receives the low-order address byte during program memory verification. Port 1 also serves alternate functions for timer 2:
	1	2	40	I	**T2 (P1.0):** Timer/counter 2 external count input.
	2	3	41	I	**T2EX (P1.1):** Timer/counter 2 trigger input.
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**INT0 (P3.2):** External interrupt
	13	15	9	I	**INT1 (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**WR (P3.6):** External data memory write strobe
	17	19	13	O	**RD (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/PROG	30	33	27	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.
PSEN	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
EA/V_{PP}	31	35	29	I	**External Access Enable/Programming Supply Voltage:** EA must be externally held low to enable the device to fetch code from external program memory locations 0000H to 1FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

DIFFERENCES FROM THE 80C51

Special Function Registers

The special function register space is the same as the 80C51 except that the 80C32/87C52 contains the additional special function registers T2CON, RCAP2L, RCAP2H, TL2, and TH2. Since the standard 80C51 on-chip functions are identical in the 8XC52, the SFR locations, bit locations, and operation are likewise identical. The only exceptions are in the interrupt mode and interrupt priority SFRs (see Table 1).

Timer/Counters

In addition to timer/counters 0 and 1 of the 80C51, the 80C32/87C52 contains timer/counter 2. Like timers 0 and 1, timer 2 can operate as either an event timer or as an event counter. This is selected by bit C/T2 in the special function register T2CON (see Figure 1). It has three operating modes: capture, auto-load, and baud rate generator, which are selected by bits in the T2CON as shown in Table 2.

In the Capture Mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. (RCAP2L and RCAP2H are new special function registers in the 80C52.) In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt. The Capture Mode is illustrated in Figure 2.

In the auto-reload mode, there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0

transition at external input T2EX will also trigger the 16-bit reload and set EXF2. The auto-reload mode is illustrated in Figure 3.

The baud rate generation mode is selected by RCLK = 1 and/or TCLK = 1. It will be described in conjunction with the serial port.

Serial Port

The serial port of the 8XC52 is identical to that of the 80C51 except that counter/timer 2 can be used to generate baud rates.

In the 8XC52, Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (see Figure 1). Note that the baud rate for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

Now, the baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as follows:

$$\text{Modes 1, 3 Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In the most typical applications, it is configured for "timer" operation (C/T2 = 0). "Timer" operation is a little different for Timer 2 when it's being used as a baud rate generator. Normally, as a timer it would increment every machine cycle (thus at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (thus at 1/2 the oscillator frequency). In that case the baud rate is given by the formula:

$$\text{Modes 1, 3 Baud Rate} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

(MSB)							(LSB)
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T2	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).
CP/RL2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

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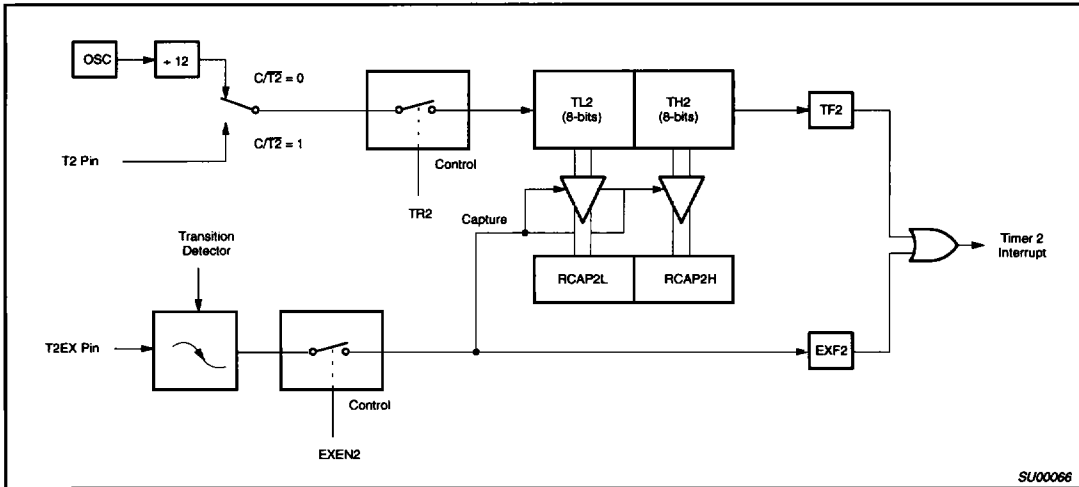**Figure 1.   Timer/Counter 2 (T2CON) Control Register**
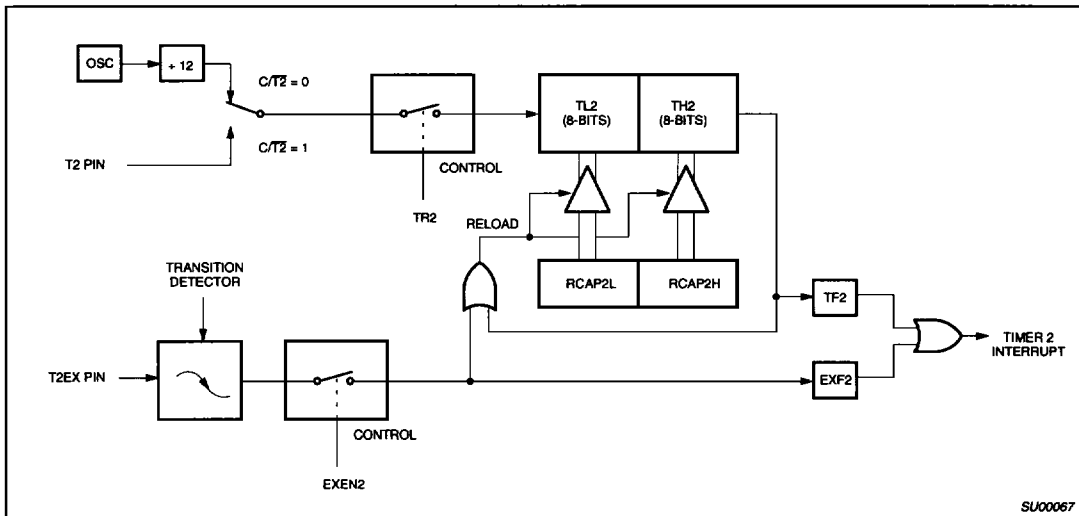
Figure 2. Timer 2 in Capture Mode

Figure 3. Timer 2 in Auto-Reload Mode
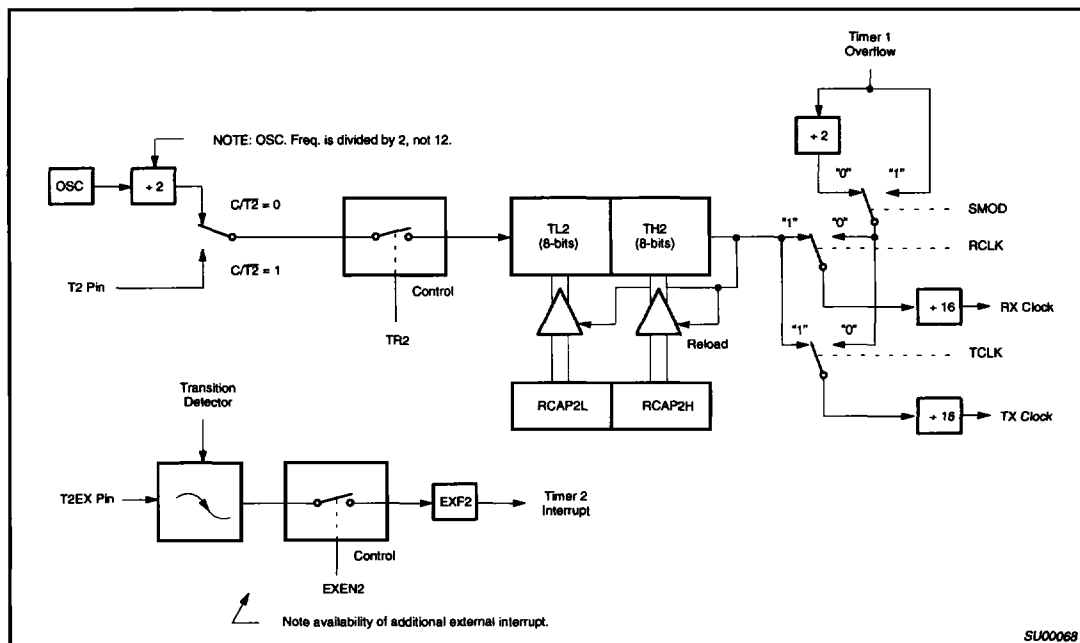
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Figure 4. Timer 2 in Baud Rate Generator Mode

Table 2.   Timer 2 Operating Modes

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK + TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Therefore, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt, if desired.

It should be noted that when Timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. Under these conditions the timer is being incremented every state time, and the results of a read or write may not be accurate. The RCAP registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. Turn the timer off (clear TR2) before accessing the Timer 2 or RCAP registers, in this case.

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. See Table 3 for set-up of timer 2 as a timer. See Table 4 for set-up of timer 2 as a counter.

Using Timer/Counter 2 to Generate Baud Rates

For this purpose, Timer 2 must be used in the baud rate generating mode. If Timer 2 is being clocked through pin T2 (P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

And if it is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

To obtain the reload value for RCAP2H and RCA02L, the above equation can be rewritten as:

$$\text{RCAP2H, RCAP2L} = 65536 - \frac{\text{Oscillator Frequency}}{32 \times \text{Baud Rate}}$$

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Interrupts

The 80C32/87C52 has 6 interrupt sources. All except TF2 and EXF2 are identical sources to those in the 80C51.

The Interrupt Enable Register and the Interrupt Priority Register are modified to include the additional 80C32/87C52 interrupt sources. The operation of these registers is identical to the 80C51.

In the 80C32/87C52, the Timer 2 Interrupt is generated by the logical OR of TF2 and EXF2. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and the bit will have to be cleared in software.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though it has been set or cleared

by hardware. That is, interrupts can be generated or pending interrupts can be canceled in software.

The interrupt vector addresses and the interrupt priority for requests in the same priority level are given in the following:

Source	Vector Address	Priority Within Level
1. IE0	0003H	(highest)
2. TF0	000BH	
3. IE1	0013H	
4. TF1	001BH	
5. RI + TI	0023H	
6. TF2 + EXF2	002BH	(lowest)

Note that they are identical to those in the 80C51 except for the addition of the Timer 2 (TF1 and EXF2) interrupt at 002BH and at the lowest priority within a level.

Table 3.   Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 4.   Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:
1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when timer 2 is used in the baud rate generator mode.

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OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the Logic Symbol, page 3-168.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all

of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. the control bits for the reduced power modes are in the special function register PCON.

DESIGN CONSIDERATIONS

At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

Table 5 shows the state of I/O ports during low current operating modes.

As a precaution to coming out of an unexpected power down, $\overline{INT0}$ and $\overline{INT1}$ should be disabled prior to entering power down.

Table 5. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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Electrical Deviations from Commercial Specifications for Extended Temperature Range (87C52)
DC and AC parameters not included here are the same as in the commercial temperature range table.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = −40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{IL}	Input low voltage, except $\overline{EA}$		−0.5	$0.2V_{CC}$−0.15	V
V_{IL1}	Input low voltage to $\overline{EA}$		0	$0.2V_{CC}$−0.35	V
V_{IH}	Input high voltage, except XTAL1, RST		$0.2V_{CC}$+1	V_{CC}+0.5	V
V_{IH1}	Input high voltage to XTAL1, RST		$0.7V_{CC}$+0.1	V_{CC}+0.5	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.45V		−75	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3	V_{IN} = 2.0V		−750	µA
I_{CC}	Power supply current: Active mode Idle mode Power-down mode	V_{CC} = 4.5–5.5V, Frequency range = 3.5 to 16MHz		32 5 50	mA mA µA

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or −40 to +85	°C
Storage temperature range	−65 to +150	°C
Voltage on $\overline{EA}$/V_{PP} pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	−0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

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DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (87C52)
T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (80C32)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
V_{IL}	Input low voltage, except $\overline{EA}$[7]		–0.5		$0.2V_{CC}$–0.1	V
V_{IL1}	Input low voltage to $\overline{EA}$[7]		0		$0.2V_{CC}$–0.3	V
V_{IH}	Input high voltage, except XTAL1, RST[7]		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST[7]		$0.7V_{CC}$		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3[9]	I_{OL} = 1.6mA[2]			0.45	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[9]	I_{OL} = 3.2mA[2]			0.45	V
V_{OH}	Output high voltage, ports 1, 2, 3, ALE, $\overline{PSEN}$[3]	I_{OH} = –60µA, I_{OH} = –25µA I_{OH} = –10µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$			V V V
V_{OH1}	Output high voltage (port 0 in external bus mode)	I_{OH} = –800µA, I_{OH} = –300µA I_{OH} = –80µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$			V V V
I_{IL}	Logical 0 input current, ports 1, 2, 3[7]	V_{IN} = 0.45V			–50	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3[7]	See note 4			–650	µA
I_{LI}	Input leakage current, port 0	V_{IN} = V_{IL} or V_{IH}			±10	µA
I_{CC}	Power supply current:[7] Active mode @ 16MHz[5] Idle mode @ 16MHz Power-down mode T_{amb} = 0 to 70°C T_{amb} = –40 to +85°C	See note 6		11.5 1.3 3	32 5 50 75	mA mA µA µA
R_{RST}	Internal reset pull-down resistor		50		300	kΩ
C_{IO}	Pin capacitance[10]				15	pF

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the *worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.* I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
5. I_{CCMAX} at other frequencies is given by: Active mode: I_{CCMAX} = 1.5 × FREQ + 8.0: Idle mode: I_{CCMAX} = 0.14 × FREQ +2.31, where FREQ is the external oscillator frequency in MHz. I_{CCMAX} is given in mA. See Figure 12.
6. See Figures 13 through 16 for I_{CC} test conditions.
7. These values apply only to T_{amb} = 0°C to +70°C. For T_{amb} = –40°C to +85°C, see table on previous page.
8. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
9. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA (*NOTE: This is 85°C specification.)
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 67mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
10. This limit is for plastic packages. For ceramic packages, the maximum limit is 20pF.

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AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (87C52)[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
1/t_{CLCL}	5	Oscillator frequency Speed versions : E			3.5	16	MHz
t_{LHLL}	5	ALE pulse width	85		$2t_{CLCL}$–40		ns
t_{AVLL}	5	Address valid to ALE low	22		t_{CLCL}–40		ns
t_{LLAX}	5	Address hold after ALE low	32		t_{CLCL}–30		ns
t_{LLIV}	5	ALE low to valid instruction in		150		$4t_{CLCL}$–100	ns
t_{LLPL}	5	ALE low to PSEN low	32		t_{CLCL}–30		ns
t_{PLPH}	5	PSEN pulse width	142		$3t_{CLCL}$–45		ns
t_{PLIV}	5	PSEN low to valid instruction in		82		$3t_{CLCL}$–105	ns
t_{PXIX}	5	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	5	Input instruction float after PSEN		37		t_{CLCL}–25	ns
t_{AVIV}	5	Address to valid instruction in		207		$5t_{CLCL}$–105	ns
t_{PLAZ}	5	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	6, 7	RD pulse width	275		$6t_{CLCL}$–100		ns
t_{WLWH}	6, 7	WR pulse width	275		$6t_{CLCL}$–100		ns
t_{RLDV}	6, 7	RD low to valid data in		147		$5t_{CLCL}$–165	ns
t_{RHDX}	6, 7	Data hold after RD	0		0		ns
t_{RHDZ}	6, 7	Data float after RD		65		$2t_{CLCL}$–60	ns
t_{LLDV}	6, 7	ALE low to valid data in		350		$8t_{CLCL}$–150	ns
t_{AVDV}	6, 7	Address to valid data in		397		$9t_{CLCL}$–165	ns
t_{LLWL}	6, 7	ALE low to RD or WR low	137	239	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	6, 7	Address valid to WR low or RD low	122		$4t_{CLCL}$–130		ns
t_{QVWX}	6, 7	Data valid to WR transition	13		t_{CLCL}–50		ns
t_{WHQX}	6, 7	Data hold after WR	13		t_{CLCL}–50		ns
t_{QVWH}	7	Data valid to WR high	287		$7t_{CLCL}$–150		ns
t_{RLAZ}	6, 7	RD low to address float		0		0	ns
t_{WHLH}	6, 7	RD or WR high to ALE high	23	103	t_{CLCL}–40	t_{CLCL}+40	ns
External Clock							
t_{CHCX}	9	High time	20		20	t_{CLCL}–t_{CLCX}	ns
t_{CLCX}	9	Low time	20		20	t_{CLCL}–t_{CHCX}	ns
t_{CLCH}	9	Rise time		20		20	ns
t_{CHCL}	9	Fall time		20		20	ns
Shift Register							
t_{XLXL}	8	Serial port clock cycle time	750		$12t_{CLCL}$		ns
t_{QVXH}	8	Output data setup to clock rising edge	492		$10t_{CLCL}$–133		ns
t_{XHQX}	8	Output data hold after clock rising edge	8		$2t_{CLCL}$–117		ns
t_{XHDX}	8	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	8	Clock rising edge to input data valid		492		$10t_{CLCL}$–133	ns

NOTES:

1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the 80C32/52 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. See application note AN457 for external memory interface.

AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0°C$ to $+70°C$ or $-40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	24MHz CLOCK		VARIABLE CLOCK		33MHz CLOCK		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	

$1/t_{CLCL}$	5	Oscillator frequency
		  Speed versions :1
		  :N
					3.5	24	3.5	33	MHz

t_{LHLL}	5	ALE pulse width	43		$2t_{CLCL}-40$		21		ns
t_{AVLL}	5	Address valid to ALE low	17		$t_{CLCL}-25$		5		ns
t_{LLAX}	5	Address hold after ALE low	17		$t_{CLCL}-25$		5		ns
t_{LLIV}	5	ALE low to valid instruction in		102		$4t_{CLCL}-65$		56	ns
t_{LLPL}	5	ALE low to $\overline{PSEN}$ low	17		$t_{CLCL}-25$		5		ns
t_{PLPH}	5	$\overline{PSEN}$ pulse width	80		$3t_{CLCL}-45$		46		ns
t_{PLIV}	5	$\overline{PSEN}$ low to valid instruction in		65		$3t_{CLCL}-60$		31	ns
t_{PXIX}	5	Input instruction hold after $\overline{PSEN}$	0		0		0		ns
t_{PXIZ}	5	Input instruction float after $\overline{PSEN}$		17		$t_{CLCL}-25$		5	ns
t_{AVIV}	5	Address to valid instruction in		128		$5t_{CLCL}-80$		72	ns
t_{PLAZ}	5	$\overline{PSEN}$ low to address float		10		10		10	ns
Data Memory									
t_{RLRH}	6, 7	$\overline{RD}$ pulse width	150		$6t_{CLCL}-100$		82		ns
t_{WLWH}	6, 7	$\overline{WR}$ pulse width	150		$6t_{CLCL}-100$		82		ns
t_{RLDV}	6, 7	$\overline{RD}$ low to valid data in		118		$5t_{CLCL}-90$		62	ns
t_{RHDX}	6, 7	Data hold after $\overline{RD}$	0		0		0		ns
t_{RHDZ}	6, 7	Data float after $\overline{RD}$		55		$2t_{CLCL}-28$		33	ns
t_{LLDV}	6, 7	ALE low to valid data in		183		$8t_{CLCL}-150$		92	ns
t_{AVDV}	6, 7	Address to valid data in		210		$9t_{CLCL}-165$		108	ns
t_{LLWL}	6, 7	ALE low to $\overline{RD}$ or $\overline{WR}$ low	75	175	$3t_{CLCL}-50$	$3t_{CLCL}+50$	41	141	ns
t_{AVWL}	6, 7	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	92		$4t_{CLCL}-75$		46		ns
t_{QVWX}	6, 7	Data valid to $\overline{WR}$ transition	12		$t_{CLCL}-30$		0.3		ns
t_{WHQX}	6, 7	Data hold after $\overline{WR}$	17		$t_{CLCL}-25$		5		ns
t_{QVWH}	7	Data valid to $\overline{WR}$ high	162		$7t_{CLCL}-130$		82		ns
t_{RLAZ}	6, 7	$\overline{RD}$ low to address float		0		0		0	ns
t_{WHLH}	6, 7	$\overline{RD}$ or $\overline{WR}$ high to ALE high	17	67	$t_{CLCL}-25$	$t_{CLCL}+25$	5	5	ns
External Clock									
t_{CHCX}	9	High time	17		17	$t_{CLCL}-t_{CLCX}$			ns
t_{CLCX}	9	Low time	17		17	$t_{CLCL}-t_{CHCX}$			ns
t_{CLCH}	9	Rise time		5		5			ns
t_{CHCL}	9	Fall time		5		5			ns
Shift Register									
t_{XLXL}	8	Serial port clock cycle time	505		$12t_{CLCL}$		363		ns
t_{QVXH}	8	Output data setup to clock rising edge	283		$10t_{CLCL}-133$		170		ns
t_{XHQX}	8	Output data hold after clock rising edge	3		$2t_{CLCL}-80$		19		ns
t_{XHDX}	8	Input data hold after clock rising edge	0		0		0		ns
t_{XHDV}	8	Clock rising edge to input data valid		283		$10t_{CLCL}-133$		170	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the 8XC52 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. Variable clock is specified for oscillator frequencies greater than 16MHz to 33MHz. For frequencies equal or less than 16MHz, see 16MHz "AC Electrial Characteristics", page 3-179.

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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE

P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float
Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{PSEN}$ low.
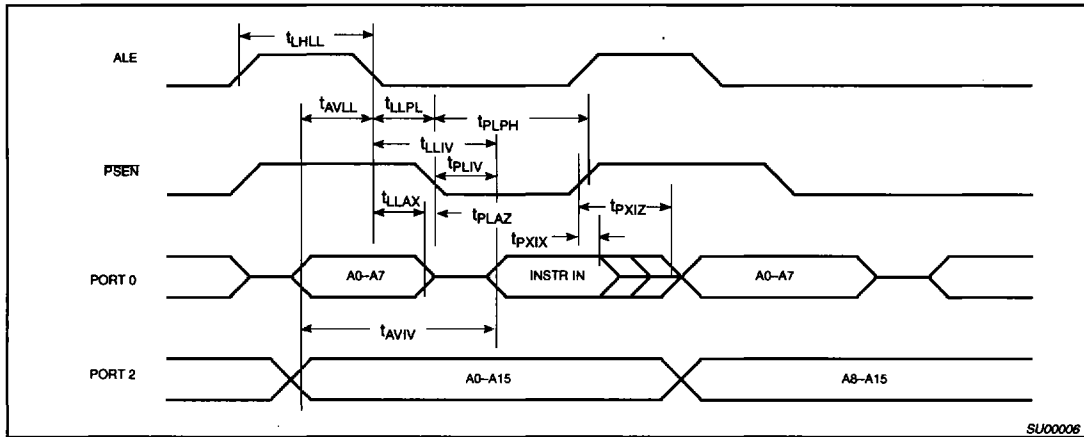
Figure 5. External Program Memory Read Cycle
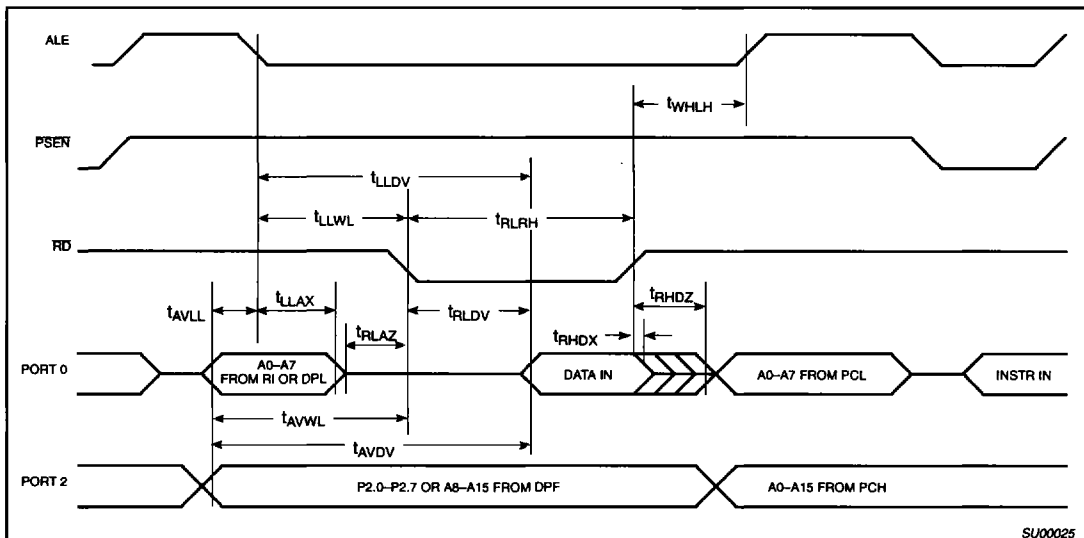
Figure 6. External Data Memory Read Cycle

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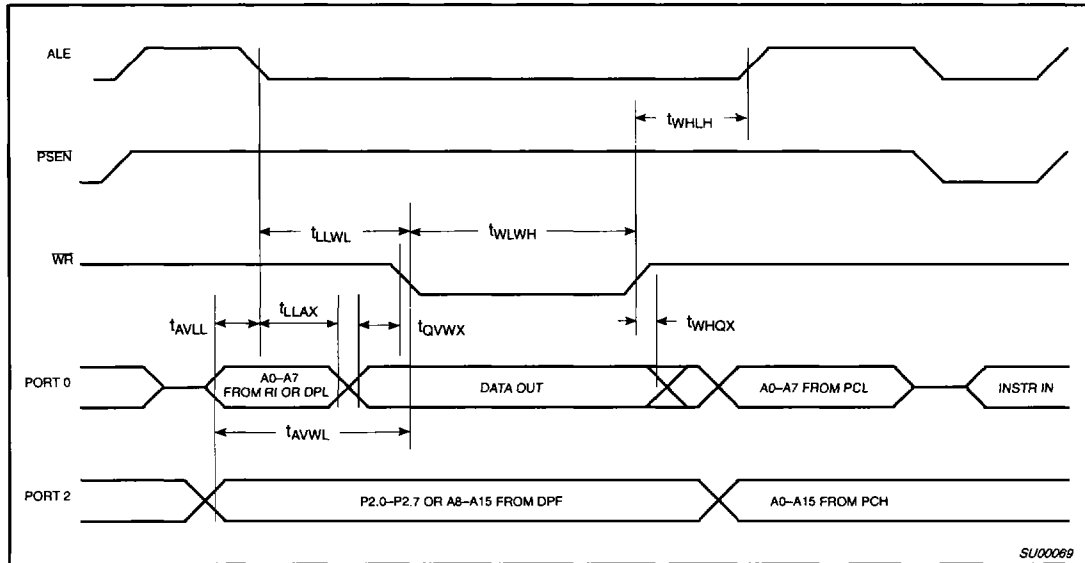
Figure 7. External Data Memory Write Cycle
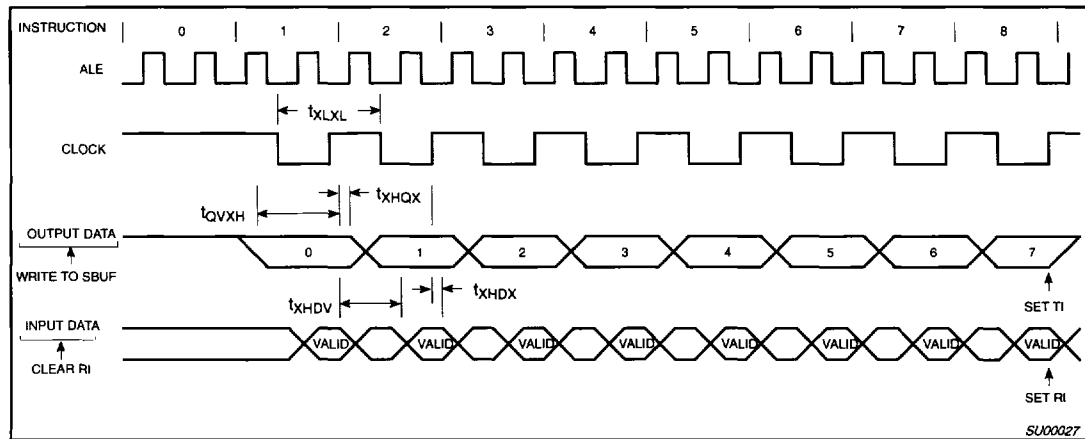
Figure 8. Shift Register Mode Timing
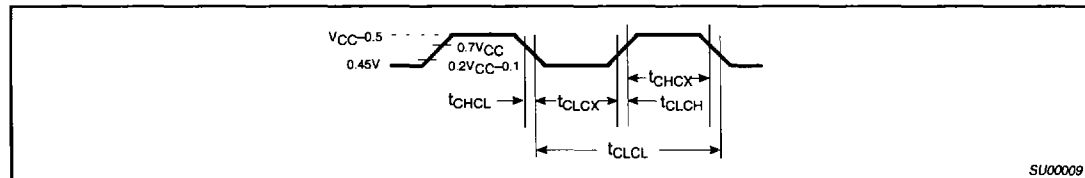
Figure 9. External Clock Drive

NOTE:
AC inputs during testing are driven at $V_{CC} -0.5$ for a logic '1' and 0.45V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

SU00010
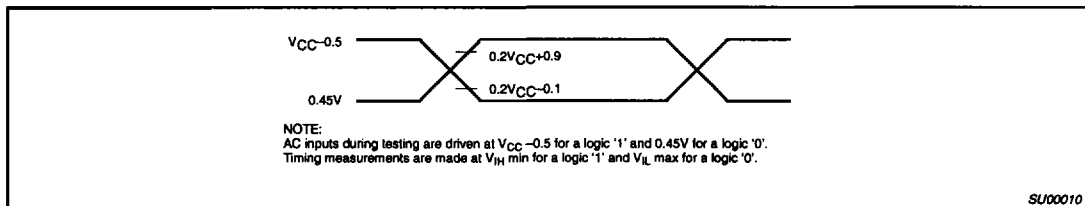
Figure 10. AC Testing Input/Output

NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs,
and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm 20mA$.

SU00011
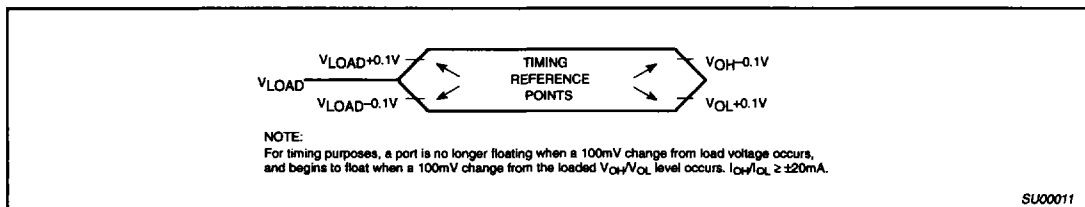
Figure 11. Float Waveform
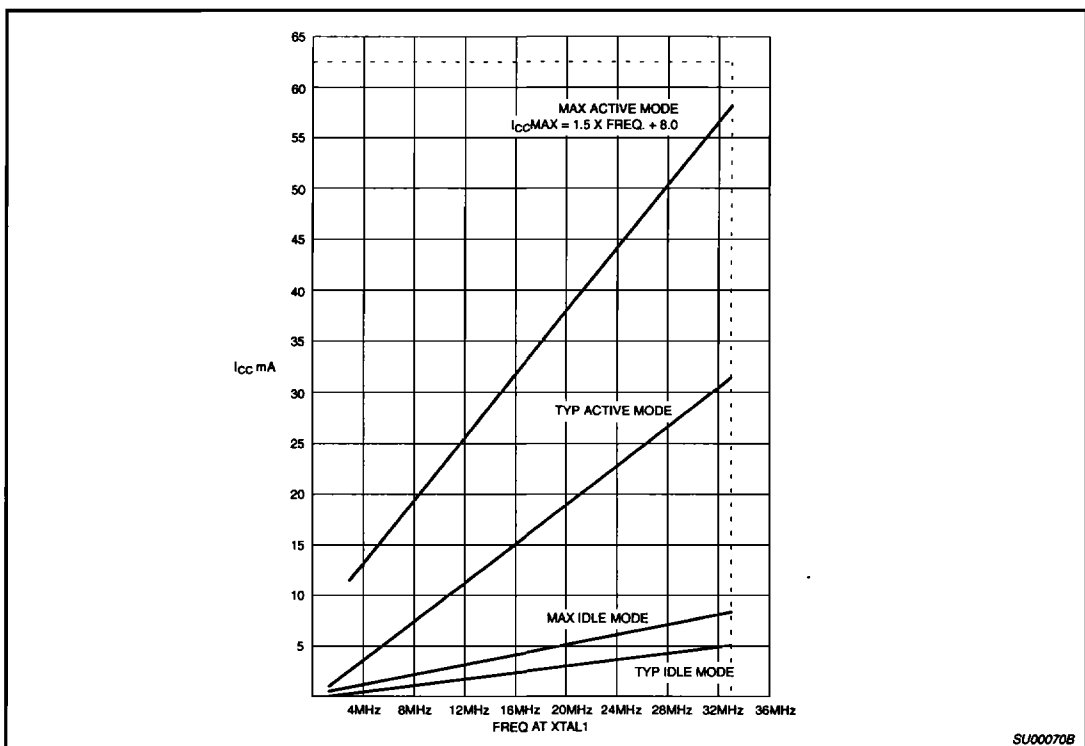
Figure 12. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test
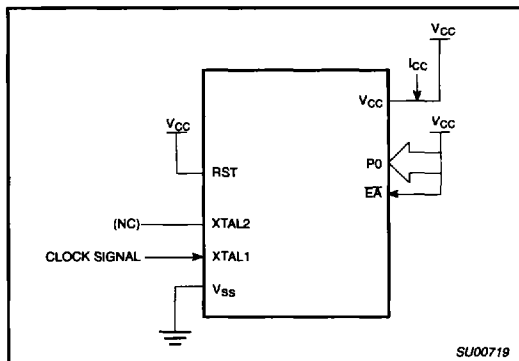
Figure 13. I_{CC} **Test Condition, Active Mode**
All other pins are disconnected
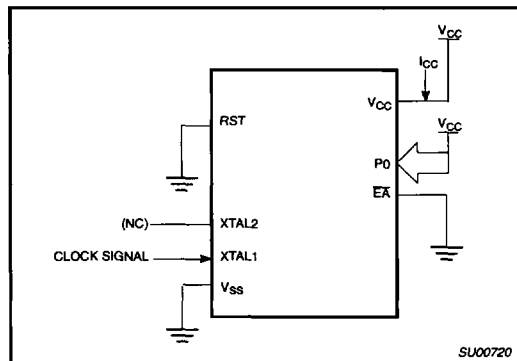
Figure 14. I_{CC} **Test Condition, Idle Mode**
All other pins are disconnected
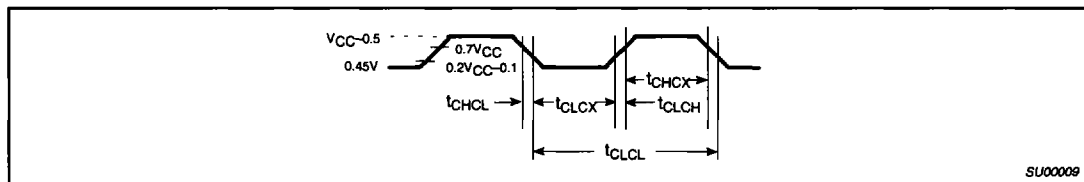
Figure 15. **Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes**
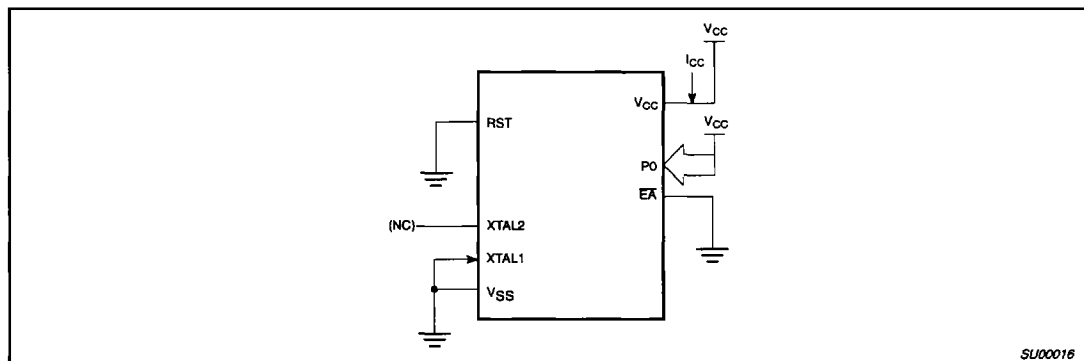$t_{CLCH} = t_{CHCL} = 5ns$

Figure 16. I_{CC} **Test Condition, Power Down Mode**
All other pins are disconnected. $V_{CC} = 2V$ to $5.5V$

EPROM CHARACTERISTICS

The 87C52 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C52 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C52 manufactured by Philips.

Table 6 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 17 and 18. Figure 19 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 17. Note that the 87C52 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 17. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 2 and 3 specified in Table 6 are held at the 'Program Code Data' levels indicated in Table 6. The ALE/PROG is pulsed low 25 times as shown in Figure 18.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 25 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the EA/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 19. The other pins are held at the 'Verify Code Data' levels indicated in Table 6. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:
(030H) = 15H indicates manufactured by Philips
(031H) = 97H indicates 87C52

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 6, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345–5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000μW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 6. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm security bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm security bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:
1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. V_{PP} = 12.75V ±0.25V.
3. V_{CC} = 5V±10% during programming and verification.
4. *ALE/PROG receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100μs (±10μs) and high for a minimum of 10μs.

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CMOS single-chip 8-bit microcontrollers

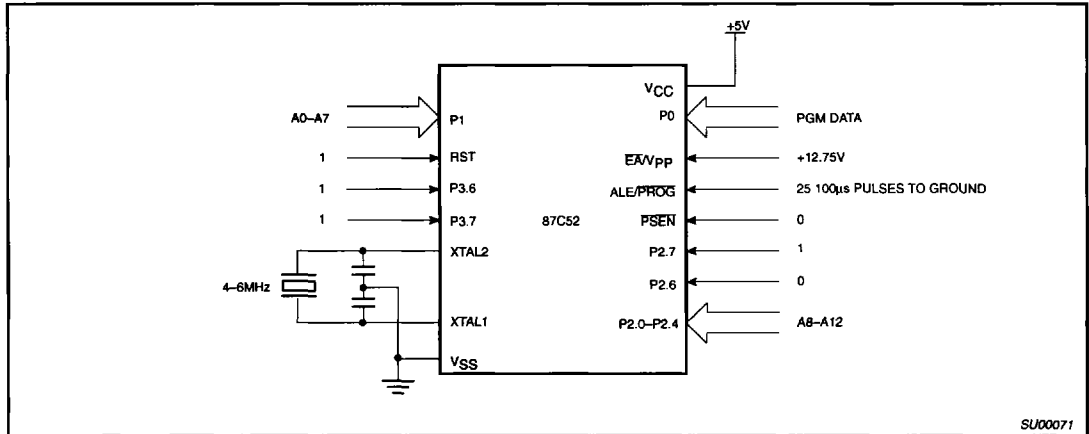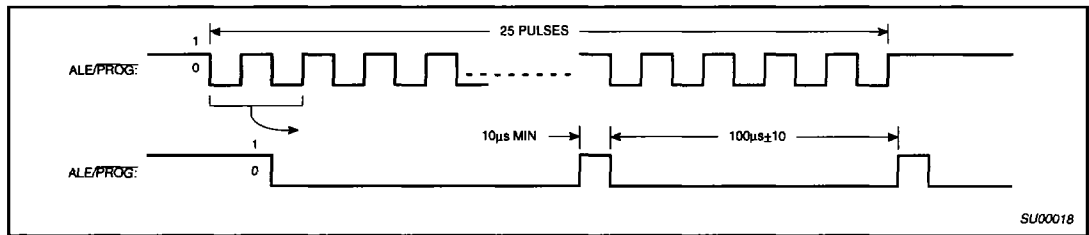**Figure 17. Programming Configuration**

Figure 18. PROG Waveform
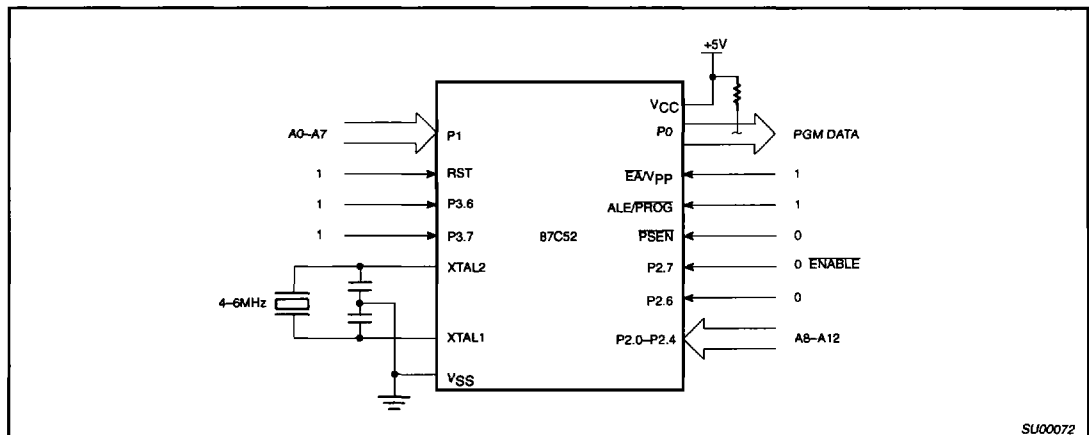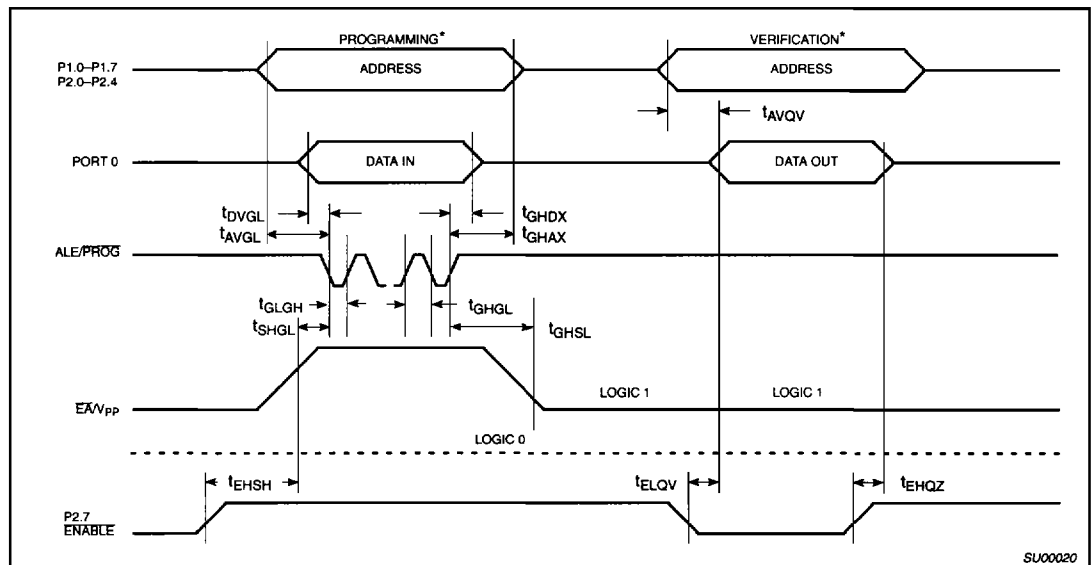

Figure 19. Program Verification

CMOS single-chip 8-bit microcontrollers

80C32/87C52

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 20)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	90	110	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		µs

NOTE:

* FOR PROGRAMMING VERIFICATION SEE FIGURE 17.
  FOR VERIFICATION CONDITIONS SEE FIGURE 19.

Figure 20. EPROM Programming and Verification