OVERVOLTAGE PROTECTION FOR ERICSSON COMPONENTS LINE INTERFACE CIRCUITS

- **Overvoltage Protector‡ for:-**

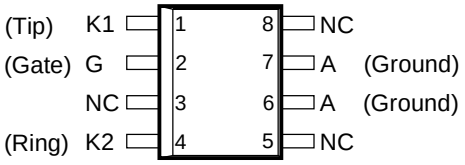
  PBL 3762A
  PBL 3764A/4, PBL 3764A/6
  PBL 3766, PBL 3766/6
  PBL 3767, PBL 3767/6
  PBL 3796, PBL 3796/2
  PBL 3798, PBL 3798/2
  PBL 3798/5
  PBL 3798/6
  PBL 3799
  PBL 3860A/1, PBL 3860A/6
  PBL 386 10/2
  PBL 386 11/2
  PBL 386 20/1
  PBL 386 21/1
  PBL 386 30/1
  PBL 386 40/1
  PBL 386 50/1
  PBL 3898/M

- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I_{TSP} A
2/10 µs	GR-1089-CORE	100
1.2/50 µs	ITU-T K22	100
0.5/700 µs	I3124	40
10/700 µs	ITU-T K20, K21	40
10/1000 µs	GR-1089-CORE	30

- **Single-Lead Line Connection Version of Feed-Through TISPPBL2D**
  - Ground Lead Creepage Distance . . > 3 mm

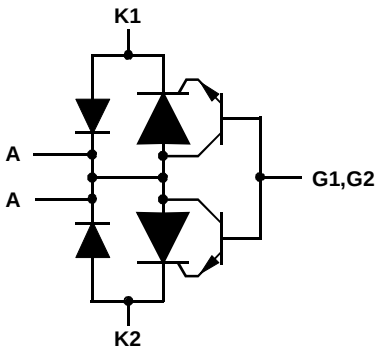
D PACKAGE
(TOP VIEW)



MD6XBA

NC - No internal connection
Terminal typical application names shown in parenthesis

device symbol



Terminals K1, K2 and A correspond to the alternative line designators of T, R and G or A, B and C. The negative protection voltage is controlled by the voltage, $V_{GG,}$ applied to the G terminal.

SD6XAP

- **Small Outline Surface Mount Package**
  - Available Ordering Options

CARRIER	ORDER #
Tube	TISPPBL2SD
Taped and reeled	TISPPBL2SDR

description

The TISPPBL2S is a dual forward-conducting buffered p-gate overvoltage protector. It is designed to protect the Ericsson Components PBL 3xxx family of SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The TISPPBL2S limits voltages that exceed the SLIC supply rail levels.

The SLIC line driver section is typically powered from 0 V (ground) and a negative voltage in the region of -10 V to -85 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimised.

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector will crowbar into a low voltage ground referenced on-state condition. As the overvoltage

‡ Customers are advised to obtain the latest version of the relevant Ericsson Components SLIC information to verify, before placing orders, that the information being relied on is current.

subsides the high holding current of the crowbar prevents d.c. latchup. The TISPPBL2S buffered gate design reduces the loading on the SLIC supply during overvoltages caused by power cross and induction.

These monolithic protection devices are fabricated in ion-implanted planar vertical power structures for high reliability and in normal system operation they are virtually transparent. The TISPPBL2S is the TISPPBL2D with a different pinout. The feed-through Ring (leads 4 — 5) and Tip (leads 1 — 8) connections have been replaced by single Ring (lead 4) and Tip (lead 1) connections. This increases package creepage distance of the biased to ground connections from about 0.7 mm to over 3 mm.

absolute maximum ratings

RATING	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, I_G = 0, -40°C ≤ T_J ≤ 85°C	V_{DRM}	-100	V
Repetitive peak gate-cathode voltage, V_{KA} = 0, -40°C ≤ T_J ≤ 85°C	V_{GKRM}	-90	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2)			
10/1000 µs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4)	I_{TSP}	30	A
0.2/310 µs (I3124, open-circuit voltage wave shape 0.5/700 µs)		40	
5/310 µs (ITU-T K20 & K21, open-circuit voltage wave shape 10/700 µs)		40	
1/20 µs (ITU-T K22, open-circuit voltage wave shape 1.2/50 µs)		100	
2/10 µs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4)		100	
Non-repetitive peak on-state current, 50/60 Hz (see Notes 1 and 2)			
100 ms	I_{TSM}	11	A
1 s		4.5	
5 s		2.4	
300 s		0.95	
900 s		0.93	
Non-repetitive peak gate current, 1/2 µs pulse, cathodes commoned (see Note 1)	I_{GSM}	40	A
Operating free-air temperature range	T_A	-40 to +85	°C
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-40 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with -40 °C ≤ T_J ≤ 85 °C. The surge may be repeated after the device returns to its initial conditions.
2. These non-repetitive rated currents are peak values for either polarirty. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of an individual terminal pair). Above 85 °C, derate linearly to zero at 150 °C lead temperature.

recommended operating conditions

		MIN	TYP	MAX	UNIT
C_G	Gate decoupling capacitor	100	220		nF
R_1	TISPPBL2S series resistor for GR-1089-CORE first-level and second-level surge survival	40			Ω
	TISPPBL2S series resistor for GR-1089-CORE first-level surge survival	25			
	TISPPBL2S series resistor for ITU-T recommendation K20/21	10			

electrical characteristics, T_{amb} = 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_D	Off-state current	V_D = V_{DRM}, V_{GK} = 0	T_J = -40 °C			-5	µA
			T_J = 85 °C			-50	µA

electrical characteristics, T_{amb} = 25 °C (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BO)}$	Breakover voltage	I_T = -20 A, 0.5/700 generator, Figure 3 test circuit (See Note 3 and Figure 2)				-70	V
$t_{(BR)}$	Breakdown time	I_T = -20 A, 0.5/700 generator, Figure 3 test circuit (See Note 3 and Figure 2)	$V_{(BR)}$ < -50 V			1	µs
V_F	Forward voltage	I_F = 5 A, t_w = 500 µs				3	V
V_{FRM}	Peak forward recovery voltage	I_F = 20 A, 0.5/700 generator, Figure 3 test circuit (See Note 4 and Figure 2)				8	V
t_{FR}	Forward recovery time	I_F = 20 A, 0.5/700 generator, Figure 3 test circuit (See Note 4 and Figure 2)	V_F > 5 V V_F > 1 V			1 10000	µs
I_H	Holding current	I_T = -1 A, di/dt = 1A/ms, V_{GG} = -50 V, -40 °C ≤ T_J ≤ 85 °C		-150			mA
I_{GAS}	Gate reverse current	V_{GG} = V_{GKRM}, V_{AK} = 0	T_J = -40 °C			-5	µA
			T_J = 85 °C			-50	µA
I_{GAT}	Gate reverse current, on state	I_T = -0.5 A, t_w = 500 µs, V_{GG} = -50 V				-1	mA
I_{GAF}	Gate reverse current, forward conducting state	I_F = 1 A, t_w = 500 µs, V_{GG} = -50 V			-10		mA
I_{GT}	Gate trigger current	I_T = -5 A, $t_{p(g)}$ ≥ 20 µs, V_{GG} = -50 V				5	mA
V_{GT}	Gate trigger voltage	I_T = -5 A, $t_{p(g)}$ ≥ 20 µs, V_{GG} = -50 V				2.5	V
C_{AK}	Anode-cathode off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, (see Note 5)	V_D = -3 V			110	pF
			V_D = -50 V			60	pF

NOTES: 3. For the required TIPX and RINGX terminal negative pulse performance refer to the respective Ericsson Components SLIC data sheet. The PBL 379x family of SLICs has ratings of -120 V for 0.25 µs, -90 V for 1 µs, -70 V for 10 ms and -70 V for d.c. The PBL 376x family together with the PBL 3860A SLIC have the same maximum ratings when the applied battery voltage is -50 V. As the FLEXI-SLIC™ PBL 386 xx family is specified in terms of current pulses, a minimum value of 2 Ω for R_P should be used. Compliance to these conditions is guaranteed by the maximum breakover voltage and the breakdown times of the TISPPBL2S.

4. For the required TIPX and RINGX terminal positive pulse performance refer to the respective Ericsson Components SLIC data sheet. The PBL 379x family of SLICs has ratings of 15 V for 0.25 µs, 10 V for 1 µs, 5 V for 10 ms and 1 V for d.c. The PBL 376x family together with the PBL 3860A SLIC have similar ratings. As the FLEXI-SLIC™ PBL 386 xx family is specified in terms of current pulses, a minimum value of 2 Ω for R_P should be used. Compliance to these conditions is guaranteed by the peak forward recovery voltage and the forward recovery times of the TISPPBL2S

5. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

thermal characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance	P_{tot} = 0.8 W, T_A = 25 °C 5 cm^2, FR4 PCB	D Package			160	°C/W

PARAMETER MEASUREMENT INFORMATION

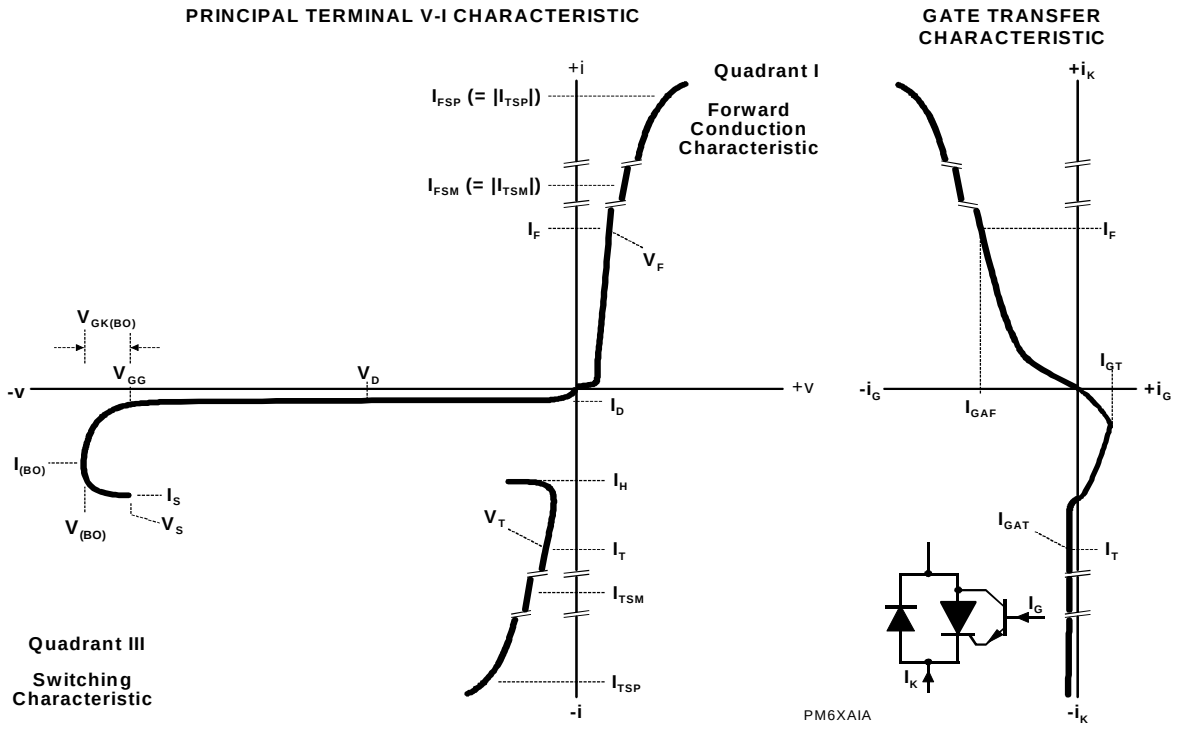


Figure 1. PRINCIPAL TERMINAL AND GATE TRANSFER CHARACTERISTICS

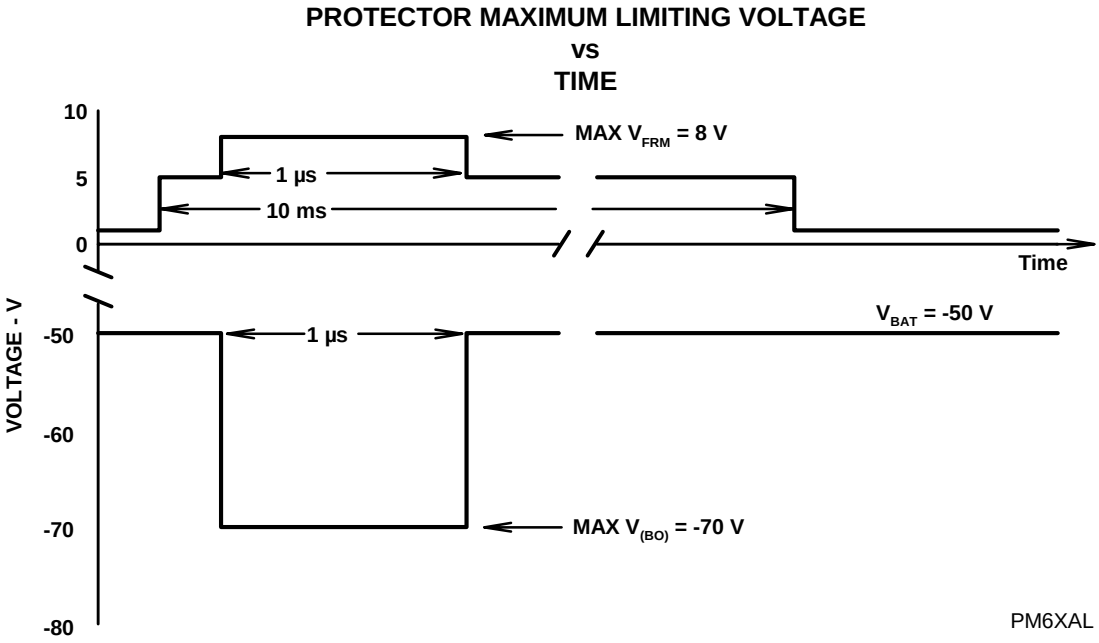


Figure 2. TRANSIENT LIMITS FOR TISPPBL2S LIMITING VOLTAGE

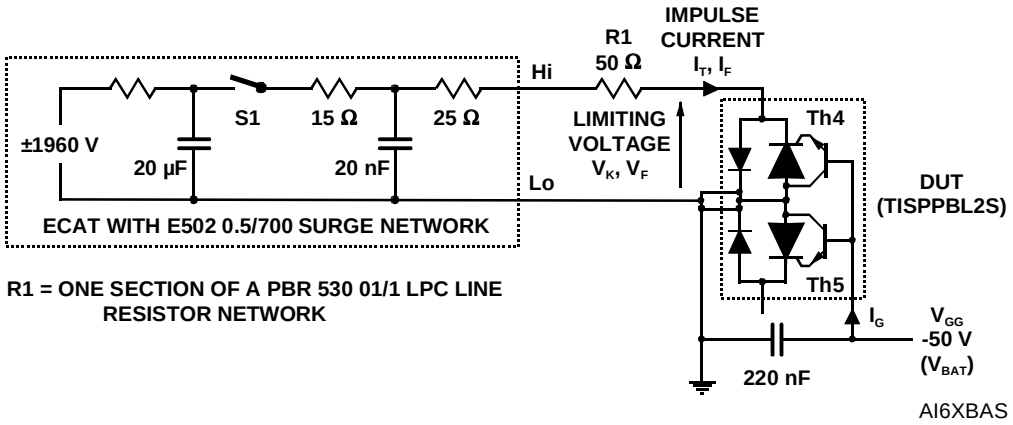


Figure 3. TEST CIRCUIT FOR MEASUREMENT OF LIMITING VOLTAGE

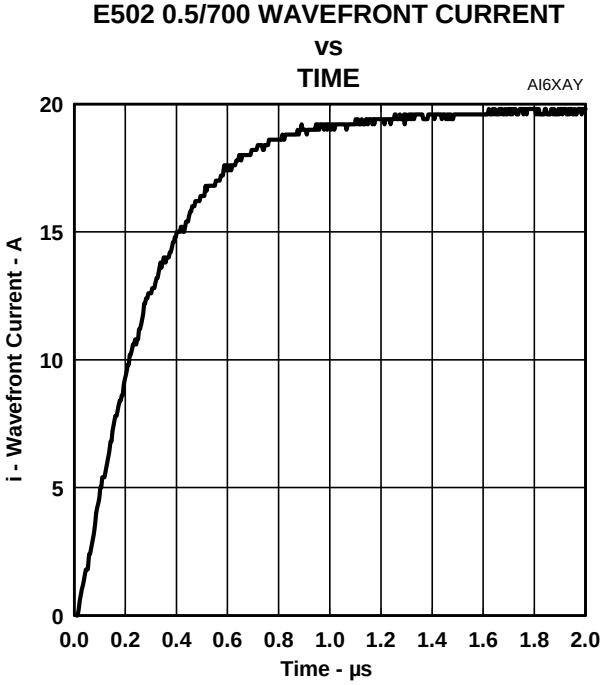


Figure 4. CURRENT WAVEFRONT

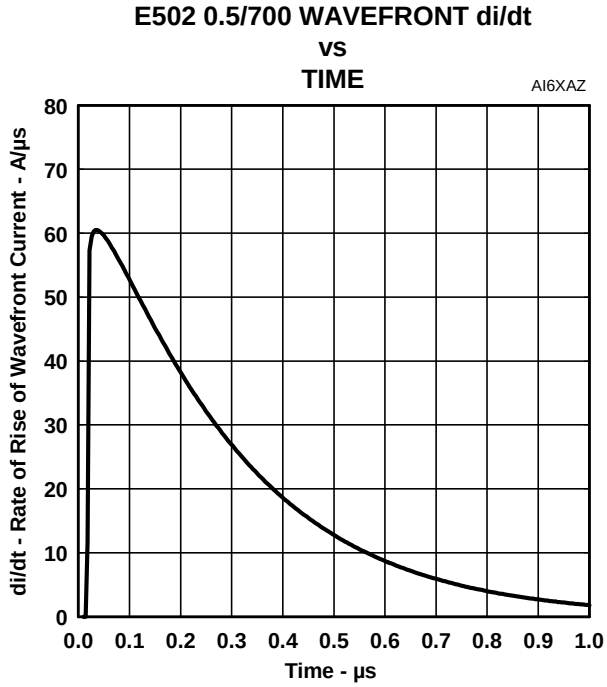


Figure 5. CURRENT WAVEFRONT di/dt

THERMAL INFORMATION

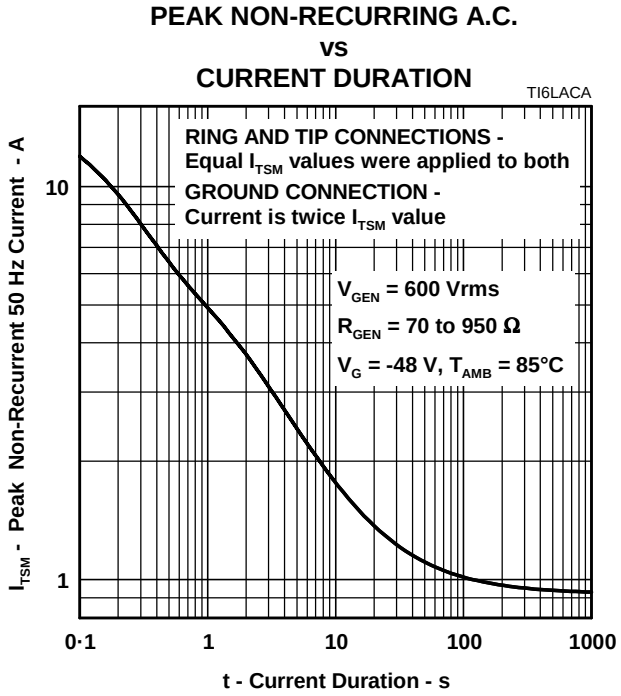


Figure 6.

TYPICAL CHARACTERISTICS

DISTRIBUTION LIMITS OF THYRISTOR LIMITING VOLTAGE vs TIME

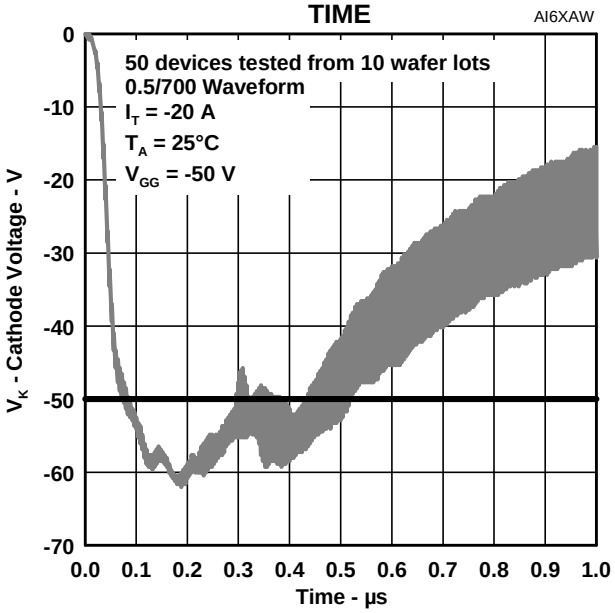


Figure 7.

DISTRIBUTION LIMITS OF DIODE FORWARD VOLTAGE vs TIME

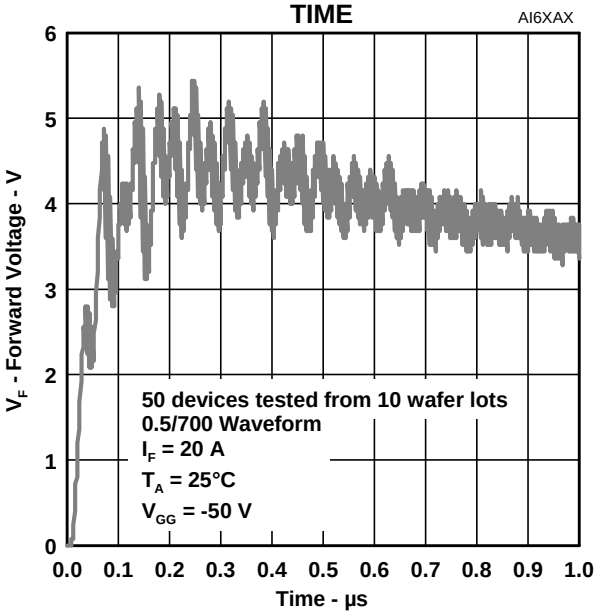


Figure 8.

CUMULATIVE POPULATION % vs PEAK LIMITING VOLTAGE

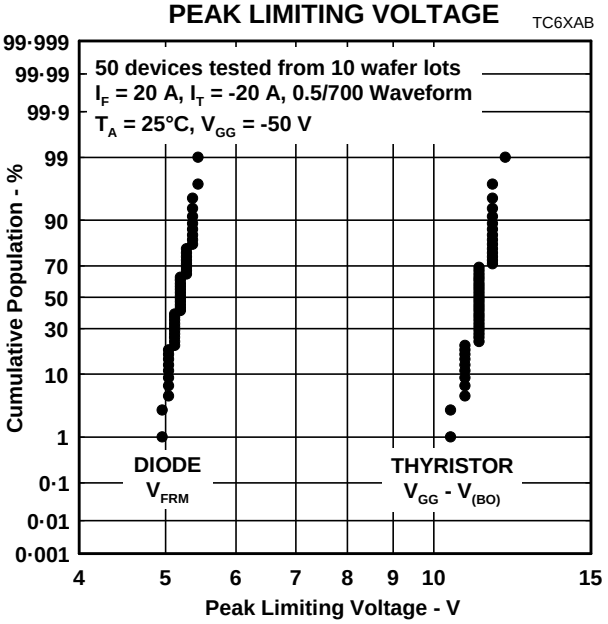


Figure 9.

DIODE FORWARD CURRENT vs FORWARD VOLTAGE

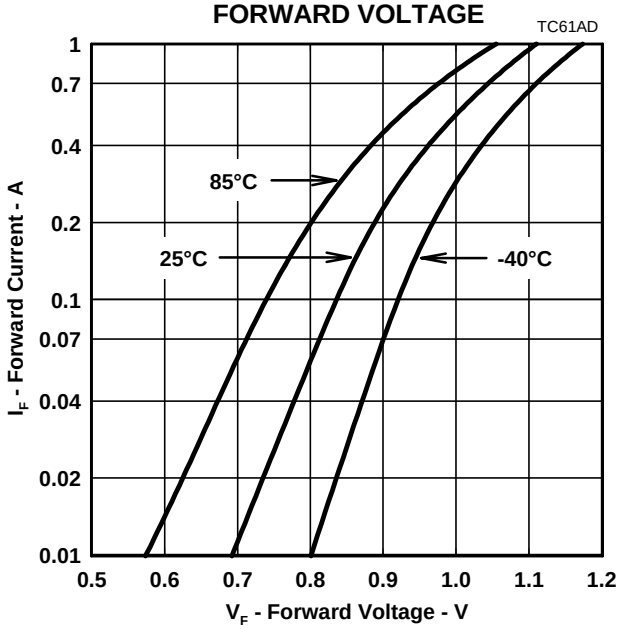


Figure 10.

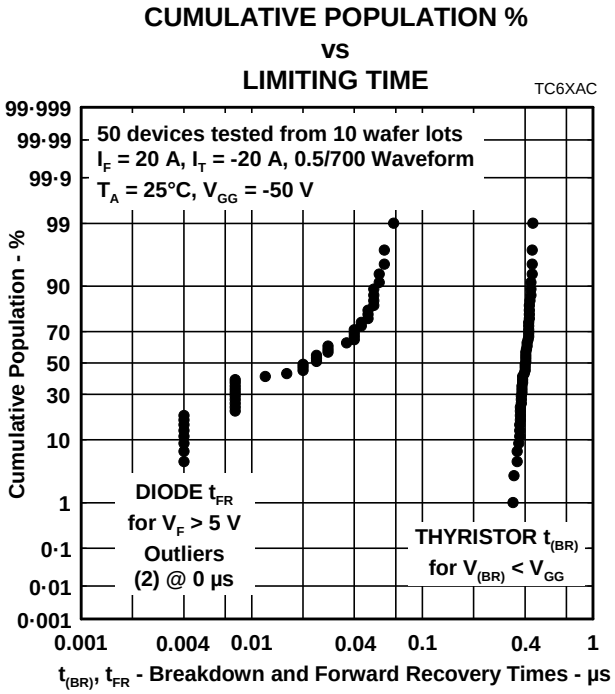


Figure 11.

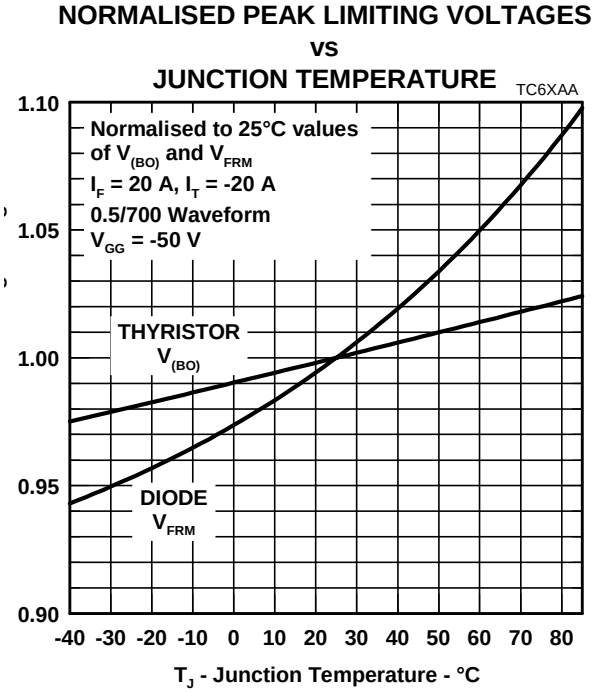


Figure 12.

APPLICATIONS INFORMATION

operation of gated protectors

Figure 13 and Figure 14 show how the TISPPBL2S limits overvoltages. The TISPPBL2S thyristor sections limit negative overvoltages and the diode sections limit positive overvoltages.

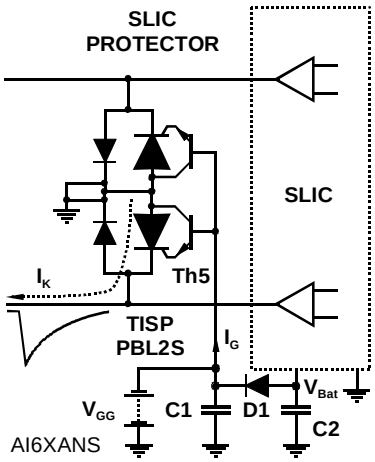


Figure 13. NEGATIVE OVERVOLTAGE CONDITION

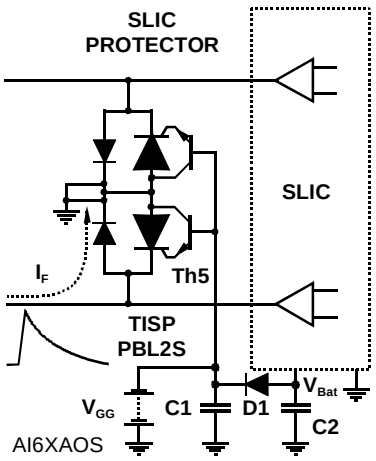


Figure 14. POSITIVE OVERVOLTAGE CONDITION

Negative overvoltages (Figure 13) are initially clipped close to the SLIC negative supply rail value (V_{BAT}) by the conduction of the transistor base-emitter and the thyristor gate-cathode junctions. If sufficient current is

available from the overvoltage, then the thyristor will crowbar into a low voltage ground referenced on-state condition. As the overvoltage subsides the high holding current of the crowbar thyristor prevents d.c. latchup.

The negative protection voltage will be the sum of the gate supply (V_{BAT}) and the peak gate(terminal)-cathode voltage ($V_{GK(BO)}$). Under a.c. overvoltage conditions $V_{GK(BO)}$ will be less than 3 V. The integrated transistor buffer in the TISPPBL2S greatly reduces protectors source and sink current loading on the V_{BAT} supply. Without the transistor, the thyristor gate current would charge the V_{BAT} supply. An electronic power supply is not usually designed to be charged like a battery. As a result, the electronic supply would switch off and the thyristor gate current would provide the SLIC supply current. Normally the SLIC current would be less than the gate current, which would cause the supply voltage to increase and destroy the SLIC by a supply overvoltage. The integrated transistor buffer removes this problem.

Fast rising impulses will cause short term overshoots in gate-cathode voltage. The negative protection voltage under impulse conditions will also be increased if there is a long connection between the gate decoupling capacitor, C1, and the gate terminal. During the initial rise of a fast impulse, the gate current (I_G) is the same as the cathode current (I_K). Rates of 60 A/µs can cause inductive voltages of 0.6 V in 2.5 cm of printed wiring track. To minimise this inductive voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimised. Inductive voltages in the protector cathode wiring can increase the protection voltage. These voltages can be minimised by routing the SLIC connection via the protector as shown in Figure 13 and Figure 14.

Positive overvoltages (Figure 14) are clipped to ground by forward conduction of the diode section in the TISPPBL2S. Fast rising impulses will cause short term overshoots in forward voltage (V_{FRM}).

TISPPBL2S limiting voltages

This clause details the TISPPBL2S voltage limiting levels under impulse conditions.

test circuit

Figure 3 shows the basic test circuit used for the measurement of impulse limiting voltage. During the impulse, the high levels of electrical energy and rapid rates of change cause electrical noise to be induced or conducted into the measurement system. It is possible for the electrical noise voltage to be many times the wanted signal voltage. Elaborate wiring and measurement techniques where used to reduce the noise voltage to less than 2 V peak to peak.

impulse generator

A Keytek ECAT E-Class series 100 with an E502 surge network was used for testing. The E502 produces a 0.5/700 voltage impulse. This particular waveform was used as it has the fastest rate of current rise (di/dt) of the commonly used lightning surge waveforms. This maximises the measured limiting voltage. Figure 4 shows the current wavefront through the DUT. To produce a peak test current level of ±20 A, the E502 charging voltage was set to ±1960 V. Figure 5 shows the DUT current di/dt. Initially the wavefront current rises at 60 A/µs, this rate then reduces as the peak current is approached. At the TISPPBL2S $V_{(BO)}$ condition the di/dt is about 50 A/µs.

limiting voltage levels

Fifty devices were measured in the test circuit of Figure 3. The 50 devices were made up from groups of 5 devices taken from 10 separately processed device lots. Figure 7 shows the total waveform variation of the thyristor limiting voltage across the 50 devices. This shows that the largest peak limiting voltage (Breakover voltage, $V_{(BO)}$) is -62 V, a 12 V overshoot beyond the -50 V gate reference supply, V_{GG}. The limiting voltage exceeds the gate reference supply voltage level for a period ($t_{(BR)}$) of about 0.4 µs.

Figure 9 and Figure 11 show these two waveform parameters in terms of device population. In Figure 9, the limiting voltage is shown in terms of the overshoot beyond the gate reference supply (V_{GG} - $V_{(BO)}$). Removing the gate reference voltage level magnifies the thyristor limiting voltage variation and shows the data stratification caused by the oscilloscope digitisation. Extrapolating the data trend indicates that the overshoot is less than 14 V at the 99.997% level (equal to 30 ppm of the population exceeding 14 V, equivalent to +4 sigma point of a normal distribution). In Figure 11, extrapolating the thyristor data trend to the 99.997% level indicates a maximum breakdown time, $t_{(BR)}$, of 0.5 µs. Figure 12 shows that increasing the temperature up to 85°C increases the thyristor peak limiting voltage by 2.4%, giving a maximum 85°C peak limiting voltage of 1.024x(-50-14) = -65.5. Over the -40°C to 85°C temperature range the TISPPBL2S is specified to have a maximum $V_{(BO)}$ value of -70 V and a breakdown time, $t_{(BR)}$, of 1 µs.

Figure 8 shows the total waveform variation of the diode limiting voltage across the 50 devices. The peak limiting voltage (Peak Forward Recovery Voltage V_{FRM}) is less than 6 V, and this value includes the 2 V of magnetically induced noise in the probe. Figure 9 shows that extrapolated 99.997% level is about 5.5 V. In Figure 11, extrapolating the diode data trend to the 99.997% level indicates a maximum forward recovery time, t_{FR}, of 0.1 µs. Figure 12 indicates that there is about a 10% uplift by increasing the temperature to 85°C. This gives a maximum 85°C peak limiting voltage of 1.1x(5.5) = 6.1 V. Over the -40°C to 85°C temperature range, the TISPPBL2S is specified to have a maximum V_{FRM} value of 8 V and a maximum forward recovery time of 1 µs.

Diodes do not switch to a much lower voltage like thyristors, so the diode limiting voltage applies for the whole impulse duration. Forward voltages of 1 V or less are normally considered safe. Figure 10 shows that the lowest current 1 V condition occurs at -40°C with a current of 0.3 A. When the TISPPBL2S is tested with the rated 10/1000 impulse it would take about 8 ms for the current to decay from 30 A to 0.3 A. Over the -40°C to 85°C temperature range, the TISPPBL2S is specified to have a V_F below 1 V within 10 ms.

SLIC protection requirements

This clause discusses the various requirements of the Ericsson Components SLICs detailed on the first page of this data sheet and compares these to the TISPPBL2S protector parameters. Some SLICs are rated for 0°C to 70°C operation, others for -40°C to 85°C operation. The TISPPBL2S protector is specified for -40°C to 85°C operation and so covers both temperature ranges.

normal operation

Depending on the SLIC type, the maximum SLIC supply voltage rating (V_{Bat}) will be -70 V, -80 V or -85 V. The -85V rating of the TISPPBL2S gate-cathode (V_{GKRM}) matches the highest SLIC voltage rating.

To restore normal operation after the TISPPBL2S has switched on, the minimum switch-off current (holding current I_H) needed is equal to the maximum SLIC short circuit current to ground (d.c. line current together with the maximum longitudinal current). For the SLICs listed on the first page of this data sheet, the TISPPBL2S minimum holding current of 140 mA will ensure switch-off after an overvoltage.

overvoltage protection

Ericsson Components specify SLIC withstand capability as a series of stress-time values. Figure 15 shows the voltage withstand limits of the PBL 3762A SLIC.

In the positive polarity, the PBL 3762A RING or TIP voltage must not exceed +15 V. For 250 ns, the PBL 3762A will be able to withstand a voltage between +10 V and +15 V. For 1 µs, the PBL 3796 will be able to withstand a voltage between +5 V and +10 V. For 10 ms, the PBL 3796 will be able to withstand a voltage between +2 V and +5 V. To protect against positive overvoltage, the TISPPBL2S positive limiting voltage must be equal to or less than these voltage values during the specified time periods.

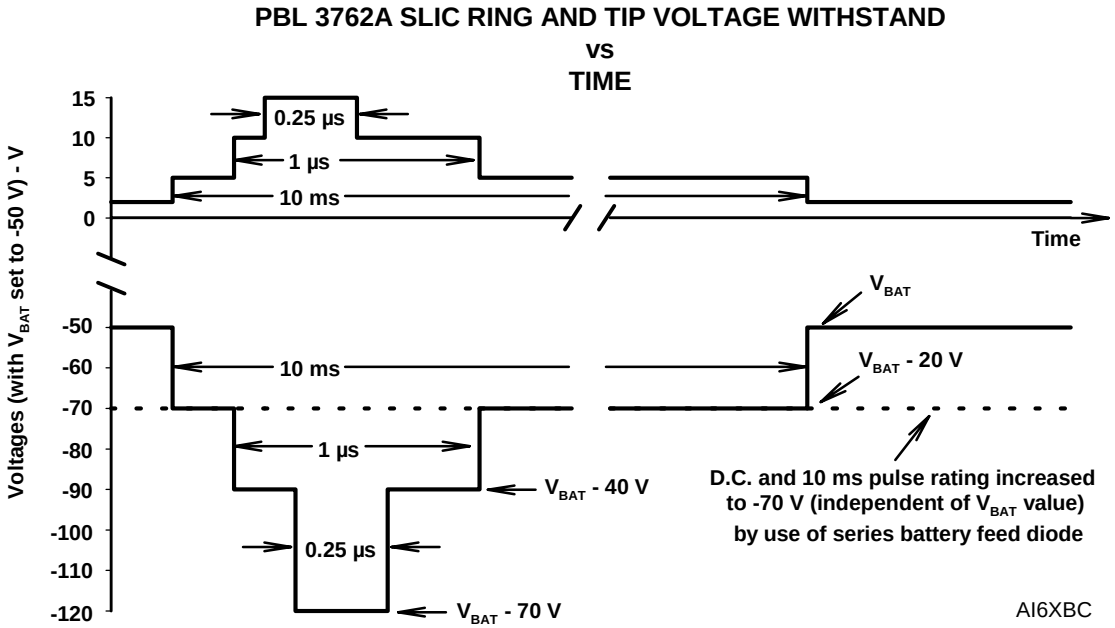


Figure 15. TRANSIENT LIMITS FOR PBL 3762A WITHSTAND VOLTAGE

In the negative polarity, the PBL 3762A RING or TIP voltage must not exceed V_{BAT} - 70. Continuously the PBL 3762A can withstand a V_{BAT} of -70 V and this implies a maximum peak voltage of -140 V. Figure 15 is drawn for a V_{BAT} of -50 V and so that the peak voltage becomes -120 V.

For 250 ns, the PBL 3762A will be able to withstand a voltage between V_{BAT} -40V and V_{BAT} -70 V or -90 V and -120 V in this case. For 1 µs, the PBL 3796 will be able to withstand a voltage between V_{BAT} -20V and V_{BAT} -40 V or -70 V and -90 V in this case. For 10 ms, the PBL 3796 will be able to withstand a voltage between V_{BAT} and V_{BAT} -20 V or -50 V and -70 V in this case. By adding a series feed diode in the battery feed the d.c. and 10 ms voltage withstands increase to -70 V, independent of the actual V_{BAT} value.To protect against negative overvoltage, the TISPPBL2S negative limiting voltage must be equal to or less than these voltage values during the specified time periods.

The following table lists the protection requirements of three selections from different SLIC families. Two, the PBL 3796 and the PBL 3762A, specify voltage withstand. The PBL 3796 specifies the negative voltages in absolute terms and the PBL 3762A specifies the negative voltages in terms of voltage relative to the battery supply voltage, V_{BAT}.

Tertiary protection is incorporated in the PBL 386 20/1 SLIC and the withstand is specified in terms of current into this protection. This type of SLIC also has more time periods specified for the current withstand values. To co-ordinate the SLIC external secondary protection (TISPPBL2S) and the internal tertiary protection, a series resistor, R_P, is required between the two. The tertiary protection will develop about 1 V and the withstand current through resistor R_P will also develop a voltage. The sum of these voltages will determine the required limiting voltage level of the TISPPBL2S. A suitable value for R_P is 2 Ω.

The negative limiting voltage of the TISPPBL2S is defined as a 1 µs, -20 V pulse below the battery voltage (Figure 2). This value does not exceed any of the voltage withstand levels listed in the SLIC withstand table. In the positive polarity the TISPBL2S limits the maximum voltage to 8 V in a 1 µs period and between 1 V and 5 V for a 10 ms period. These values do not exceed the values listed in the SLIC withstand table.

SLIC withstand comparison

SLIC	PBL 3796		PBL 3762A		PBL 386 20/1	
CONDITION	V	V	V	V	A	A
continuous	-70 Note 1	+1 Note 1	V_{Bat} (-70 V) Note 3	+2	-0.1 Note 6	+0.1
pulse < 10 ms	-70 Note 1	+5 Note 1	V_{Bat} - 20 Note 3	+5	-2 Note 5	+2 Note 5
pulse < 1 ms					-5 Note 5	+5 Note 5
pulse < 10 µs					-15 Note 5	+15 Note 5
pulse < 1 µs	-90 Note 1	+10 Note 1	V_{Bat} - 40 Note 3	+10	-20 Note 5	+20 Note 5
pulse < 250 ns	-120 Note 1, 2	+15 Note 1, 2	V_{Bat} - 70 Note 4	+15	-20 Note 5	+20 Note 5

Notes:
1. These voltage rating require a diode to be installed in series with the V_{Bat} pin.
2. R_{F1}, $R_{F2} \geq 20\ \Omega$ is also required. Pulse supplied to TIP and RING outside R_{F1}, R_{F2}
3. A diode in series with the V_{Bat} input increases the permitted continuous voltage and pulse < 10 ms to -70 V. A pulse ≤ 1 µs is increased to the greater of |-70 V| or |V_{Bat} - 40 V|
4. R_{F1}, $R_{F2} \geq 20\ \Omega$ is also required. Pulse supplied to TIP and RING outside R_{F1}, R_{F2}
5. Pulse is applied to TIP and RING outside R_{P1} and R_{P2}
6. Permitted continuous voltage for V_{Bat} is -75 V

A graphical representation is shown in Figure 16. In the positive polarity, the three line types correspond to the three SLIC types discussed (R_P is 2 Ω for the PBL 386 20/1). The two shaded areas represent the positive and negative maximum limiting voltage levels of the TISPPBL2S as per Figure 2. The negative voltage withstand capability of the three SLICs is shown relative to their maximum rated battery supply voltage, V_{BATM}. Figure 16 shows that the TISPPBL2S maximum limiting voltage levels do not exceed the SLIC voltage withstand ratings.

application circuit

Figure 17 shows a typical TISPPBL2S SLIC card protection circuit. The incoming line conductors, R and T, connect to the relay matrix via the series over-current protection. Fusible resistors, fuses and positive temperature coefficient (PTC) resistors can be used for over-current protection. Resistors will reduce the prospective current from the surge generator for both the TISPPBL2S and the ring/test protector. The TISP7xxxF3 protector has the same protection voltage for any terminal pair. This protector is used when the ring generator configuration may be ground or battery-backed. For dedicated ground-backed ringing generators, the TISP3xxxF3 gives better protection as its inter-conductor protection voltage is twice the conductor to ground value.

Relay contacts 3a and 3b connect the line conductors to the SLIC via the TISPPBL2S protector. Closing contacts 3a and 3b connects the TISPPBL2S protector in parallel with the ring/test protector. As the ring/test protector requires much higher voltages than the TISPPBL2S to operate, it will only operate when the contacts 3a and 3b are open. Both protectors will divert the same levels of peak surge current and their

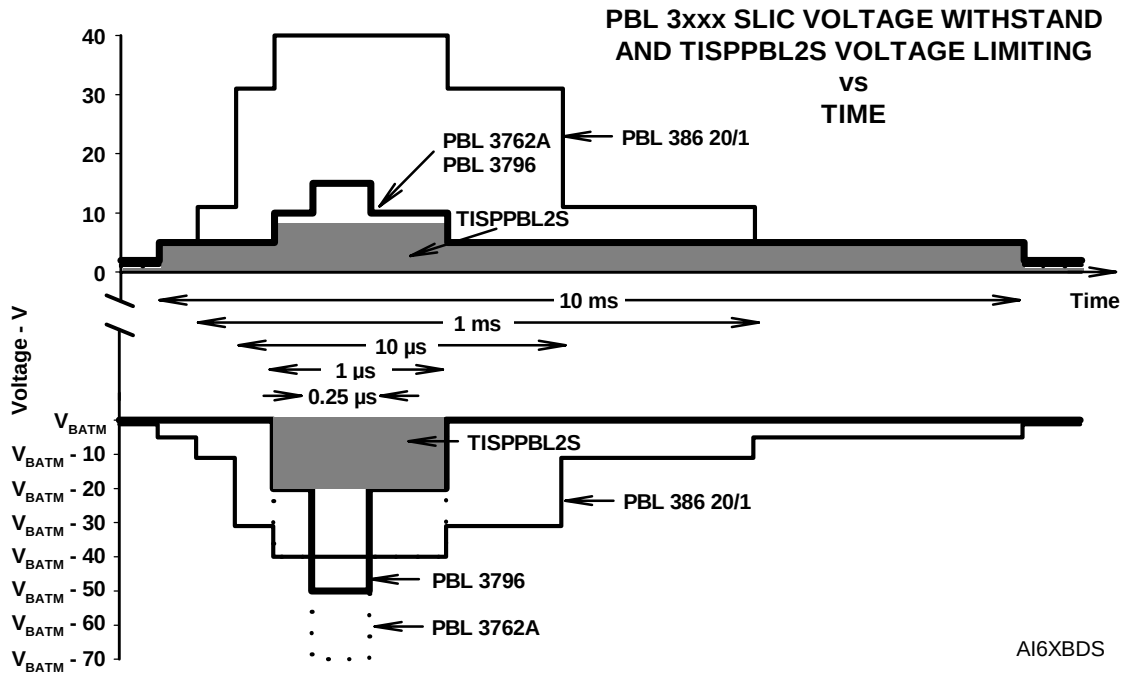


Figure 16. SLIC VOLTAGE WITHSTAND AND TISPPBL2S PROTECTION LEVELS

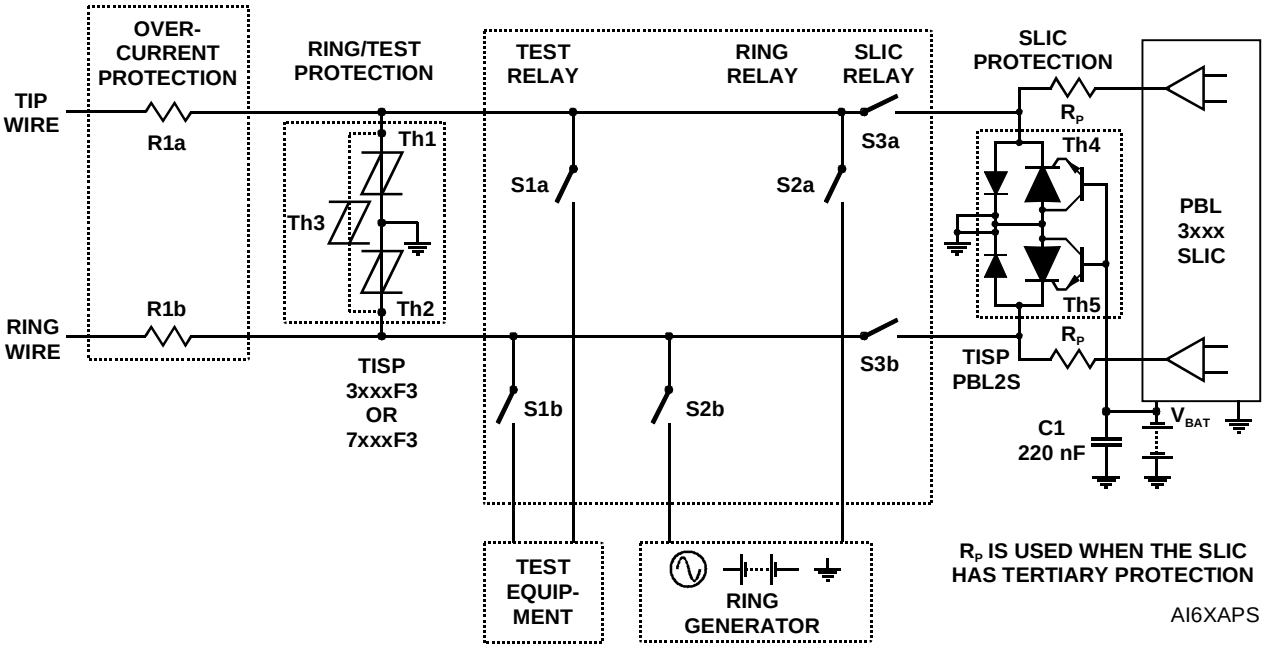


Figure 17. TYPICAL APPLICATION CIRCUIT

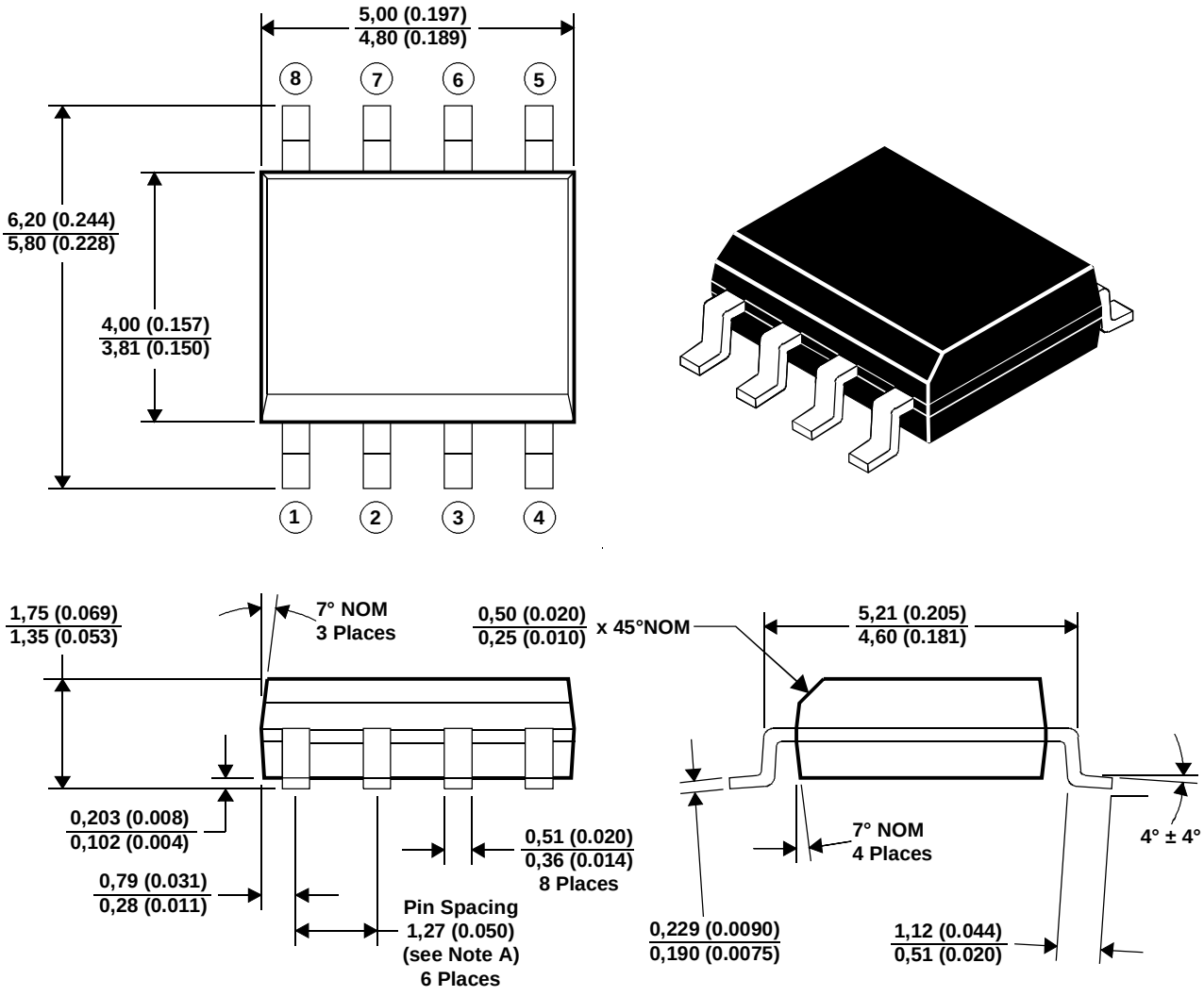
required current ratings should be similar. The TISPPBL2S protector gate reference voltage comes from the SLIC negative supply (V_{BAT}). A 220 nF gate capacitor sources the high gate current pulses caused by fast rising impulses. When the SLIC has internal tertiary protection (e.g. PBL 386 21/1), then the two R_P resistors need to be added for protection co-ordination.

MECHANICAL DATA

D008

plastic small-outline package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



MDXXAA

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002).

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