PRELIMINARY **VT20C71 • VT20C72**

4,096 x 4 SEPARATE I/O SRAM

FEATURES

- High-speed access and cycle times: 20, 25, 35 ns
- Automatic power-down at deselect
- Pin-compatible with standard 4K x 4 separate I/O SRAMs
- Low-power CMOS process: 600 mW active (typical) 35 mW standby (typical)
- High-reliability six-transistor memory cell
- Capable of withstanding greater than 2000 V ESD
- 300-mil, 24-pin plastic dual in-line packages
- 24-pin SOIC and SOJ packages

DESCRIPTION

The VT20C71 and VT20C72 are high-speed static RAMs organized as 4,096 words by 4 bits. They were developed in conjunction with VISIC Inc., and are fabricated using an advanced 1.5 micron CMOS process. These devices offer very high performance and reliability as well as low power, making them suitable for use in high-performance cache memory, writeable control store, and high-speed data buffer applications.

The VT20C71 and VT20C72 feature an automatic power-down that offers a standby current of only 7 mA (typical) when deselected.

For easy memory expansion, both devices have active-LOW Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) signals, as well as three-state outputs. The outputs may be placed in the high-impedance state with the Write Enable signal LOW (VT20C72 only) or with the Chip Enable HIGH.

The VT20C71 and VT20C72 are packaged in 300-mil dual in-line packages with industry-standard pinouts, and in 24-pin small-outline packages. They are compatible with other static RAMs, yet offer higher speeds for increased system performance.

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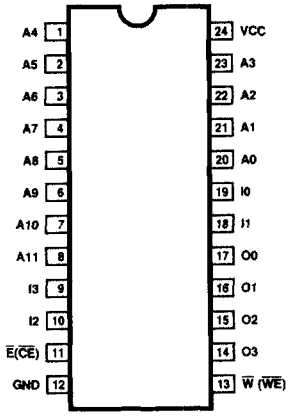
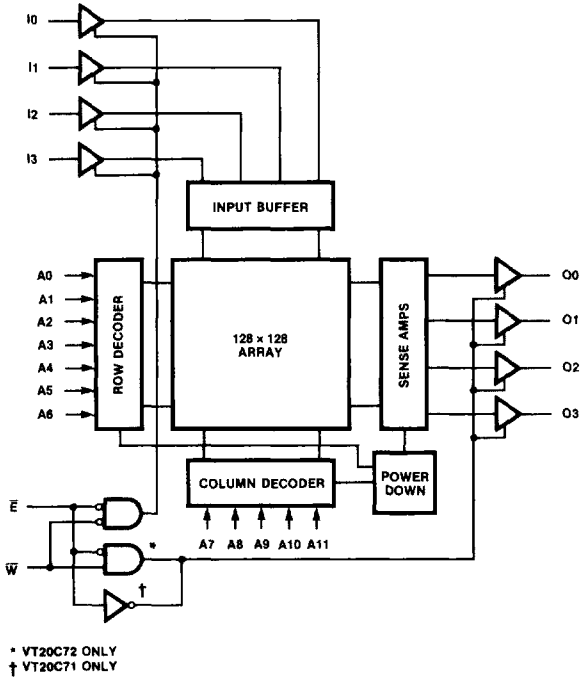
PIN DIAGRAM

VT20C71 • VT20C72



BLOCK DIAGRAM



* VT20C72 ONLY
† VT20C71 ONLY

PIN NAMES

A0 – A11	Address Inputs
I0 – I3	Data Input
O0 – O3	Data Output
E ($\overline{CE}$)	Chip Enable
W ($\overline{WE}$)	Write Enable
VCC	Power (5 V)
GND	Ground (0 V)

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature (TA)	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Voltage on Any Terminal Relative to Ground	−1.5 V to +7.0 V
Short Circuit Current	30 mA
Static Discharge Voltage	>2000 V
Latch-Up Current (TA = 0°C to +70°C)	>200 mA

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of this device under these or any conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±10%, Note 1

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input LOW Voltage	−1.0		0.8	V	Note 2
VIH	Input HIGH Voltage	2.2		VCC + 1.0	V	Note 3
IIL	Input Leakage Current	−10		10	uA	VIN = VCC to GND
IOL	Output Leakage Current	−10		10	uA	
VOH	Output HIGH Voltage	2.4			V	IOUT = −4 mA
VOL	Output LOW Voltage			0.4	V	IOUT = 8 mA
ICC	Power Supply Current 20 ns 25 ns 35 ns			 150 135 120	 mA mA mA	$\overline{E}$ = VIL, outputs open-load
ISB	Standby Current			10	mA	$\overline{E} \geq$ VIH

CAPACITANCE TA = 25°C, f = 1 MHz

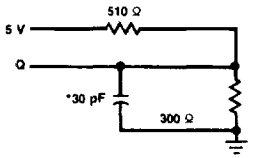
Symbol	Parameter	Typ	Max	Unit	Condition
CI	Input Capacitance	7	10	pF	
CO	Output Capacitance	7	10	pF	

AC TEST CONDITIONS

Input Voltage Levels	0 V to 3 V
Input Transition Times	5 ns
Input Reference Level	1.5 V
Output Reference Level	1.5 V
Output Load	Figures 1a and 1b

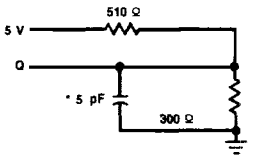
AC TESTING LOAD CIRCUIT

FIGURE 1a. OUTPUT LOAD CIRCUIT A



*INCLUDES SCOPE AND TEST JIG.

FIGURE 1b. OUTPUT LOAD CIRCUIT B



*INCLUDES SCOPE AND TEST JIG.

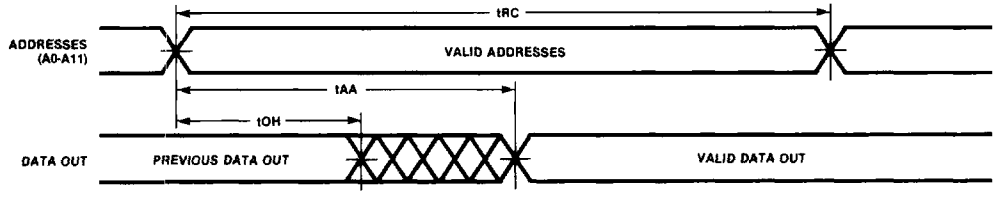
Notes:
1. Operation across the temperature range is guaranteed with 400 linear feet per minute of air flow.
2. VIL min is −2.0 V for pulse widths of less than 20 ns.
3. All input pins are diode-clamped to VCC. Some testers may not have enough drive capability to reach the maximum input voltage.

READ CYCLE TIMING CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±10%

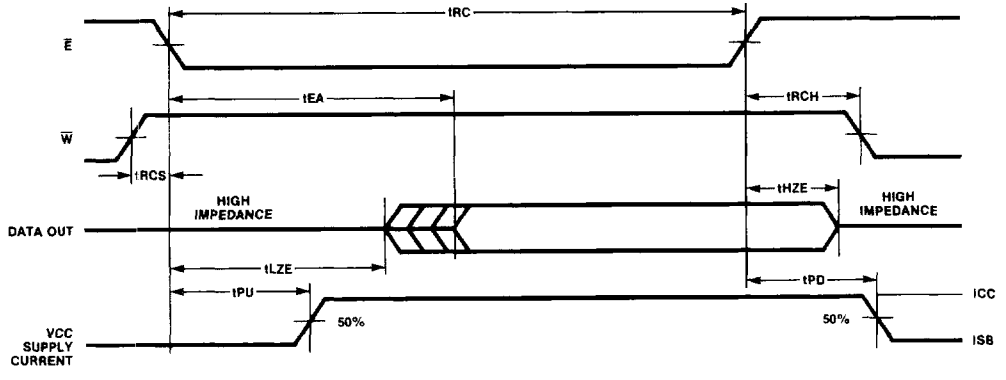
Symbol	Parameter	VT20C71-20 VT20C72-20		VT20C71-25 VT20C72-25		VT20C71-35 VT20C72-35		Unit	Condition
		Min	Max	Min	Max	Min	Max		
tRC	Read Cycle	20		25		35		ns	
tAA	Address Access		20		25		35	ns	
tOH	Output Hold from Address Change	5		5		5		ns	
tEA	$\overline{E}$ LOW to Output Valid		20		25		35	ns	
tLZE	$\overline{E}$ LOW to Output Low-Impedance	3		3		3		ns	Output Load Figure 1b
tHZE	$\overline{E}$ HIGH to Output High-Impedance		10		15		15	ns	Output Load Figure 1b
tPU	$\overline{E}$ LOW to Power-Up	0		0		0		ns	
tPD	$\overline{E}$ HIGH to Power-Down		15		15		15	ns	
tRCS	Read Command Set-Up	0		0		0		ns	
tRCH	Read Command Hold	0		0		0		ns	

TIMING DIAGRAMS

READ CYCLE NO. 1 ($\overline{W}$ = VIH, $\overline{E}$ = VIL)



READ CYCLE NO. 2, Note 1



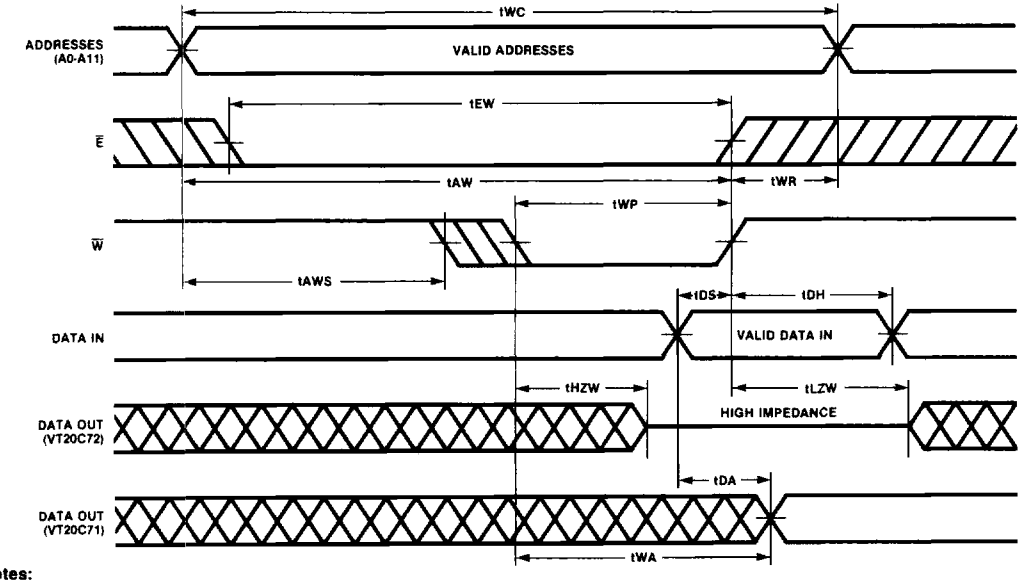
Note:
1. Address valid prior to or coincident with $\overline{E}$ transition LOW.

WRITE CYCLE TIMING CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±10%

Symbol	Parameter	VT20C71-20 VT20C72-20		VT20C71-25 VT20C72-25		VT20C71-35 VT20C72-35		Unit	Condition
		Min	Max	Min	Max	Min	Max		
tWC	Write Cycle	20		25		35		ns	
tEW	Enable LOW to End of Write	20		25		35		ns	
tAW	Address Set-Up to End of Write	15		20		30		ns	
tWR	Address Hold from End of Write	0		0		0		ns	
tAWS	Address Set-Up to Beginning of Write	0		0		0		ns	
tWP	Write Pulse Width	15		20		25		ns	
tDS	Data In Set-Up to End of Write	10		12		15		ns	
tDH	Data In Hold after End of Write	0		0		0		ns	
tHZW	Write LOW to Output High-Impedance (VT20C72)		10		10		15	ns	Output Load Figure 1b
tLZW	Write HIGH to Output Low-Impedance (VT20C72)	0		0		0		ns	Output Load Figure 1b
tWA	Write LOW to Output Valid (VT20C71)	20		25		35		ns	
tDA	Data In Valid to Output Valid (VT20C71)	20		25		35		ns	

TIMING DIAGRAM

WRITE CYCLE NO. 1, Notes 1 and 2

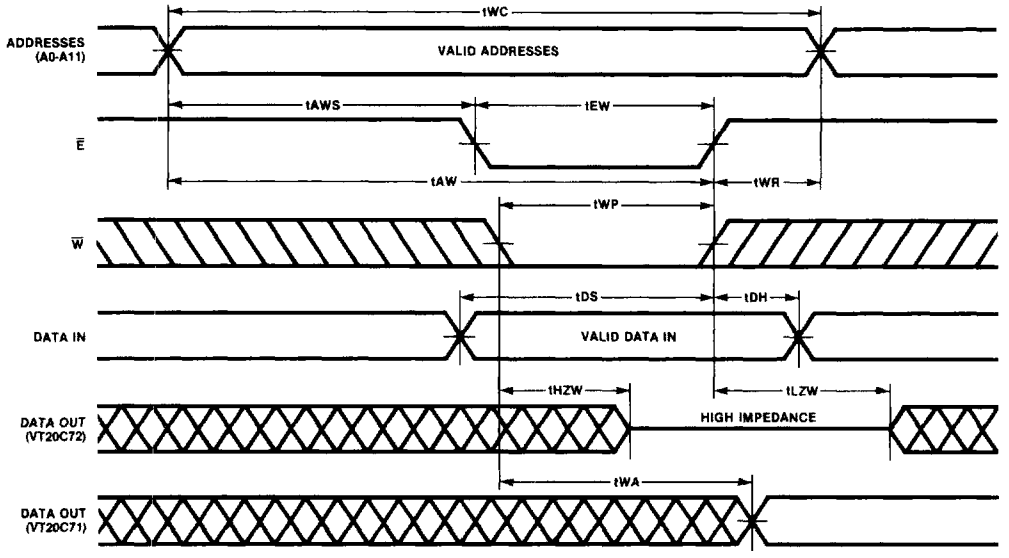


Notes:

1. W̄-controlled write cycle.
2. Both Ē and W̄ must be LOW to initiate a write. Either signal can terminate a write by going HIGH; thus, data set-up and hold are referenced to the rising edge of Ē or W̄, whichever occurs first.

TIMING DIAGRAM (Cont).

WRITE CYCLE NO. 2, Notes 1 - 3



POWER DISTRIBUTION AND TRACE LINE TERMINATION CONSIDERATIONS

To achieve full compatibility with TTL-based devices, CMOS memories are typically designed to convert TTL input levels to the CMOS levels required for internal operation. Greater power efficiency is achieved, however, when an entire design takes advantage of the lower consumption capabilities of CMOS technology. When CMOS levels are used throughout a design and not only in the memory, lower current specifications can be achieved, resulting in a lower overall power requirement.

The operating margins of all devices on a board using very-high-speed memory can best be maintained by providing a quiet environment that is free of noise spikes, undershoot, and excessive ringing. Key elements in creating such an atmosphere are observing proper power distribution techniques and proper termination of TTL drive lines.

POWER DISTRIBUTION

A power distribution scheme that effectively maintains wide operating margins combines power trace layout with decoupling capacitor placement to minimize the series impedance in the decoupling path. This path runs from the power pin of a memory device through its decoupling capacitor to the ground pin.

The total impedance of this path is established by the power line impedance and the impedance of the capacitor itself. In practice, the capacitive effects of the decoupling path are minimal because of the very-high-frequency components of the current transients associated with memory operation. This makes the line inductance the dominant impedance factor.

The preferred technique for reducing power line impedance and improving the quality of VCC and ground is to use separate power and ground planes.

A somewhat-less-effective approach is to grid the power and ground traces. If this is done, the ground grid should extend the TTL driver peripheral circuitry, providing a solid ground reference for the TTL drivers.

The decoupling capacitor, which provides energy for the high-frequency transients, should be placed as near the memory device as possible in order to have the shortest practical lead lengths. This capacitor should be of a low-inductance type and,

Notes:

1. $\overline{E}$-controlled write cycle.
2. Both $\overline{E}$ and $\overline{W}$ must be LOW to initiate a write. Either signal can terminate a write by going HIGH; thus, data set-up and hold are referenced to the rising edge of $\overline{E}$ or $\overline{W}$, whichever occurs first.
3. If $\overline{E}$ goes HIGH simultaneously with $\overline{W}$ high, the output remains in a high-impedance state (VT20C72 only).

at a minimum, be 0.1 uF. For the greatest efficiency, it should be placed between the power supply and ground pins of each device.

Low-frequency current transients can be handled by larger tantalum capacitors placed near the memory board edge connector, where the power traces meet the backplane power distribution system. Such large capacitors provide bulk energy storage that prevents voltage drops caused by the long inductive path between the memory board and the power supply.

TRACE TERMINATION

On a memory board, trace lines have the appearance of shorted transmission lines to TTL-level driver signals. This can cause reflections of TTL signals propagating down the lines, particularly LOW-going signals. These reflections can be reduced or eliminated by proper line termination. Proper termination also reduces RFI emissions.

Trace line termination can be either series or parallel, although series termination is recommended. This type of termination has the advantage of drawing no dc current, and also requires the smallest number of components to implement. It simply calls for placing a series resistor in the signal line to dampen reflections. The resistor is placed at the output of the TTL driver, as close as possible to the driver package. The driver/termination combination should be placed close to the memory array to minimize lead length.

In most applications, a series resistor of between 10 ohms and 33 ohms is sufficient to dampen reflections. However, because the characteristic impedance of each layout is different, some experimentation may be necessary to determine the optimum value for a specific configuration.

SIGNAL FIDELITY

When the layout is complete and the power distribution and line termination requirements have been met, it is good procedure to verify signal fidelity by observation with a wide-band (300 MHz or faster) oscilloscope and probe.