AN6363, AN6363S

VTR Color AFC Circuit

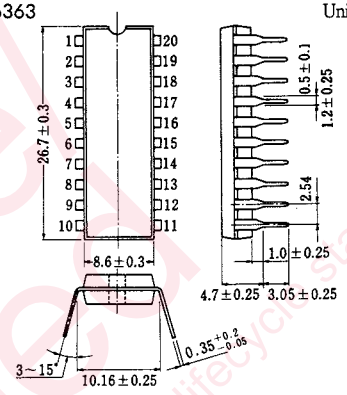
■ Outline

The AN6363 and the AN6363S are integrated circuits designed for VTR color AFC and constitute a PAL-system color signal processing circuit for VTR by combining with the AN6360, the AN6360S, the AN6371 or the AN6371S.

■ Features

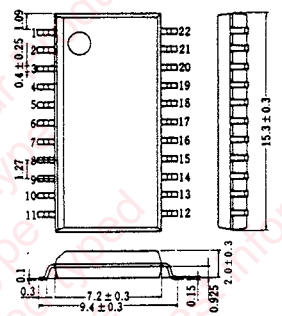
- The functions consist of:
  - AFC circuit
  - Synchro separation circuit
  - 90° rotary circuit
- Supply voltage either 9V or 12V

AN6363 Unit: mm



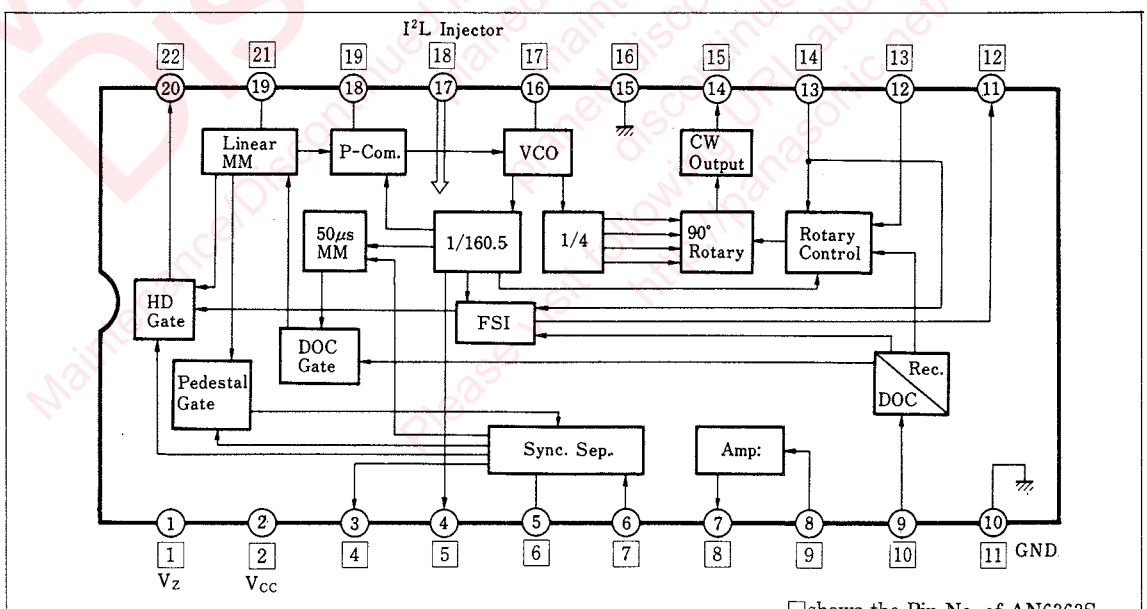
20-Lead DIL Plastic Package

AN6363S



22-Lead PANAFALAT Package (SO-22D)

■ Block Diagram



□shows the Pin No. of AN6363S

Maintenance/Discontinued

■ Pin

( ) shows the Pin No. of AN6363S

Pin No.	Pin Name	Pin No.	Pin Name
1 (1)	Zener Voltage	11 (12)	2nd FSI Output
2 (2)	V_{CC}	12 (13)	ID Input
3 (4)	V_{CC} Output for V Sync.	13 (14)	PG (Head SW) Input
4 (5)	Sync Front Pulse Output	14 (15)	CW (627kHz) Output
5 (6)	Low Pass Filter	15 (16)	GND
6 (7)	Sync. Sep. Input	16 (17)	VCO Control
7 (8)	White Clip Output	17 (18)	I^2L Injector
8 (9)	Video Input	18 (19)	P-Com. Filter
9 (10)	Rec./DOC Select	19 (21)	Linear Mono. Multi.
10 (11)	GND	20 (22)	HD Output for Burst Gate

In case of AN6363S, Pin No.③,⑳ are NC.

■ Absolute Maximum Ratings (Ta=25℃)

Item		Symbol	Rating	Unit
Supply voltage		V_{CC}	13	V
Power dissipation (Ta=70℃)	AN6363	P_D	550	mW
	AN6363S		270*	
Operating ambient temperature		T_{opr}	−20~+70	℃
Storage temperature	AN6363	T_{stg}	−40~+150	℃
	AN6363S		−40~+125	

*Indicates a package capability.

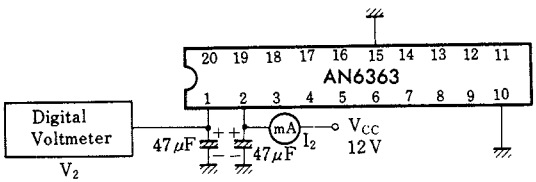
■ Electrical Characteristics ($V_{CC}=V_{2-15}=12V$, Ta=25℃±2℃)

Item		Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit current		I_2	1		18		37	mA
Zener voltage		V_Z	1		6.1		7.2	V
VCO frequency control sensitivity	AN6363	β_{14}	3	I_{17}=28mA	270		490	kHz/V
	AN6363S	β_{15}						
HSS input sensitivity	AN6363	S_8	4	I_{17}=28mA	0.5			V_{P-P}
	AN6363S	S_9						
VSS output amplitude	AN6363	v_{O3}	2	I_{17}=28mA	5		6.4	V
	AN6363S	v_{O4}						
HD output amplitude	AN6363	v_{O20}	2	I_{17}=28mA	5		6.4	V
	AN6363S	v_{O22}						
Sync. Front pulse output amplitude	AN6363	v_{O4}	2	I_{17}=28mA	5		6.4	V
	AN6363S	v_{O5}						
Sync. Front pulse width	AN6363	t_4	2	I_{17}=28mA		10.7		μs
	AN6363S	t_5						
627 kHz CW output amplitude	AN6363	v_{O14}	2	I_{17}=28mA	1.3		2.3	V
	AN6363S	v_{O15}						
627 kHz 2nd harmonic	AN6363	$2f_{14}$	5	I_{17}=28mA, Z_{I17}=6.8kΩ			−20	dB
	AN6363S	$2f_{15}$						
PG input "H" voltage	AN6363	S_{13-H}	6	I_{17}=28mA, Z_{I17}=6.8kΩ	4		7	V
	AN6363S	S_{14-H}						
PG input "L" voltage	AN6363	S_{13-L}	6	I_{17}=28mA, Z_{I17}=6.8kΩ			0.8	V
	AN6363S	S_{14-L}						
2nd FSI output amplitude	AN6363	v_{O11}	7	I_{17}=28mA	5		6.4	V
	AN6363S	v_{O12}						
Rec./PB select sensitivity	AN6363	S_{9-1}	7	I_{17}=28mA	0.5			mA
	AN6363S	S_{10-1}						
DOC input sensitivity	AN6363	S_{9-2}	7	I_{17}=28mA			2	V
	AN6363S	S_{10-2}						
VCO oscillation frequency	AN6363	f_{OSC14}	8	I_{17}=28mA	2.3		4.1	MHz
	AN6363S	f_{OSC15}						
ID input sensitivity	AN6363	S_{12}	9	I_{17}=28mA			0.2	V
	AN6363S	S_{13}						

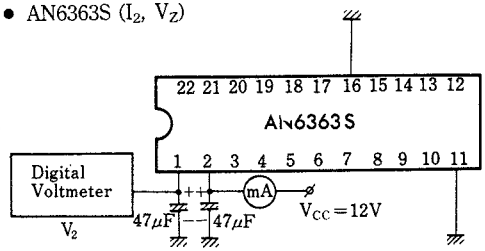
Note) Operating supply voltage range $V_{CC(opr)}$=8.5~12.5V

Test Circuit 1

- AN6363 (I_2, V_Z)

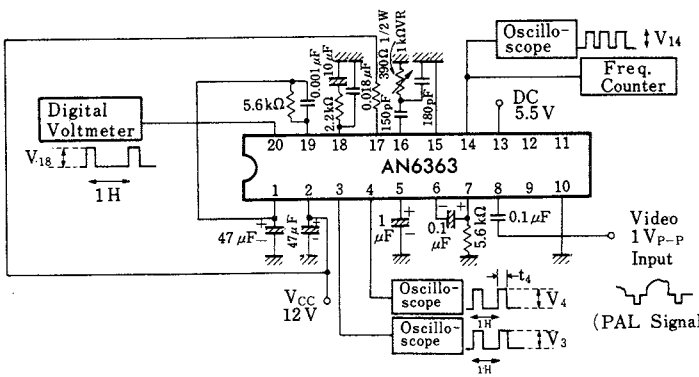


- AN6363S (I_2, V_Z)



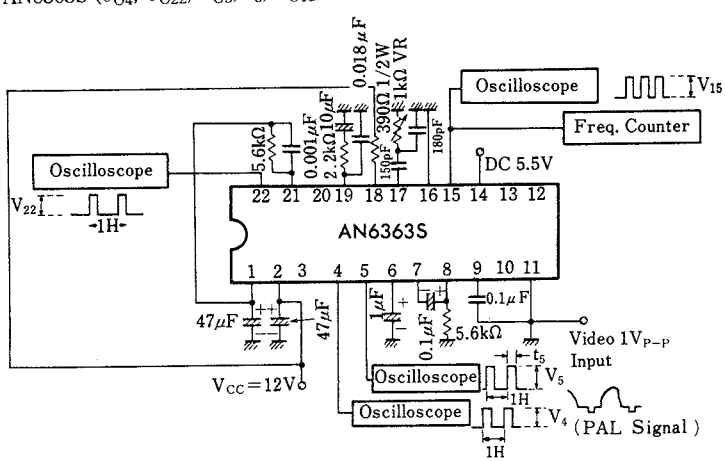
Test Circuit 2

- AN6363 (v_{O3}, v_{O20}, v_{O4}, t_4, v_{O14})



Variable resistor setting
Note 1) Set to V_{18} a Pin⑱ DC voltage when Pin⑧ input is OFF.
Note 2) Adjust the 1kΩ VR for the Pin⑯ so that a Pin⑱ voltage will be V_{18} when input is made to the Pin⑧.
This setting becomes a basic condition here after.

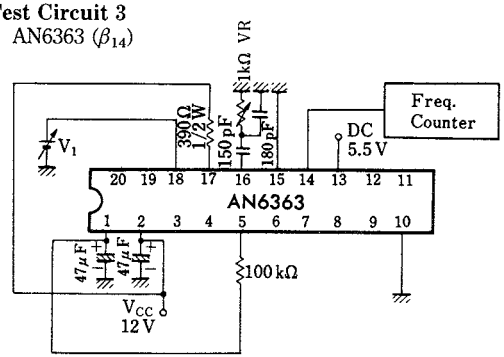
- AN6363S (v_{O4}, v_{O22}, v_{O5}, t_5, v_{O15})



Variable resistor setting
Note 1) Set to V_{19} a Pin⑲ DC voltage when Pin⑨ input is OFF.
Note 2) Adjust the 1kΩ VR for the Pin⑰ so that a Pin⑲ voltage will be V_{19} when input is made to the Pin⑨.
This setting becomes a basic condition here after.

Test Circuit 3

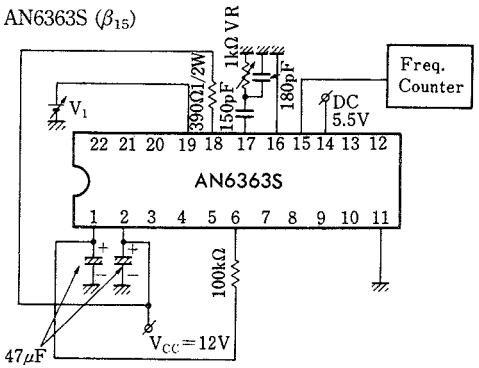
- AN6363 (β_{14})



Note) Determine a four−fold Pin⑭ output frequency change as β_{14} when a V_{18} DC voltage is changed by ±0.5V without changing the Pin⑱ variable resistor set in Test Circuit 2.

$\beta_{14} = 4 \times (f_{14(V18+0.5)} - f_{14(V18-0.5)})$

- AN6363S (β_{15})

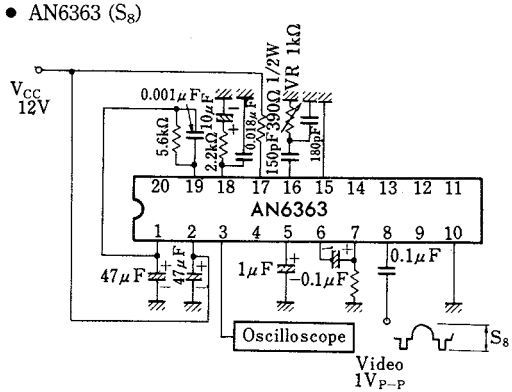


Note) Determine a four−fold Pin⑮ output frequency change as β_{15} when a V_{19} DC voltage is changed by ±0.5V without changing the Pin⑰ variable resistor set in Test Circuit 2.

$\beta_{15} = 4 \times (f_{15(V19+0.5)} - f_{15(V19-0.5)})$

Test Circuit 4

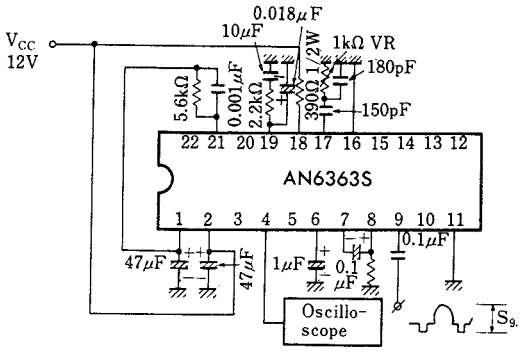
- AN6363 (S_8)



Note 1) Pin⑧ input signal amplitude when Pin③ output is normally made by increasing Pin⑧ input from 0

Note 2) Do not change the Pin⑯ variable resistor. (same as Test Circuit 2)

- AN6363S (S_9)

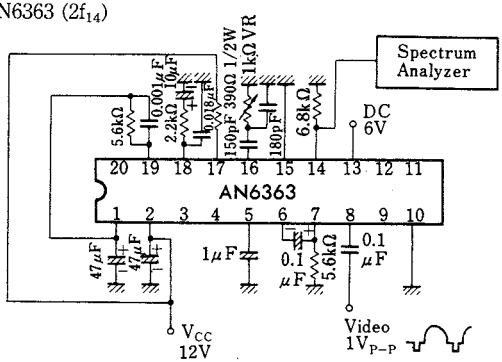


Note 1) Pin⑨ input signal amplitude when Pin④ output is normally made by increasing Pin⑨ input from 0

Note 2) Do not change the Pin⑰ variable resistor. (same as Test Circuit 2)

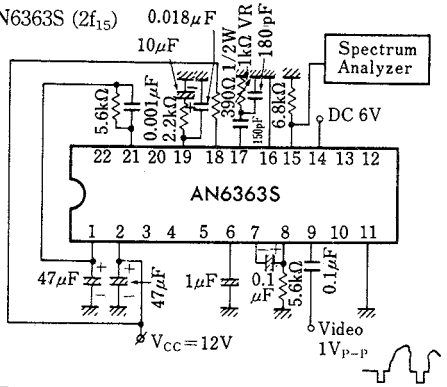
Test Circuit 5

- AN6363 ($2f_{14}$)



Note) Do not change the Pin⑯ variable resistor. (same as Test Circuit 2)

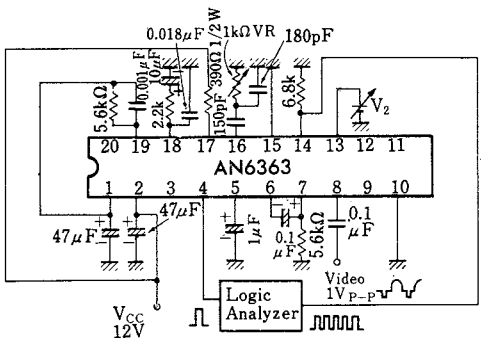
- AN6363S ($2f_{15}$)



Note) Do not change the Pin⑰ variable resistor. (same as Test Circuit 2)

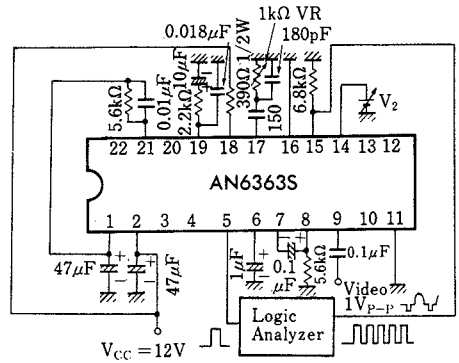
Test Circuit 6

- AN6363 (S_{13-H}, S_{13-L})



Note 1) Pin⑬ DC voltages at which Pin⑭ output changes a phase by 90° at an intermediate timing of Pin④ output "H", and when it does not.
Note 2) Do not change the Pin⑭ variable resistor. (same as Test Circuit 2)

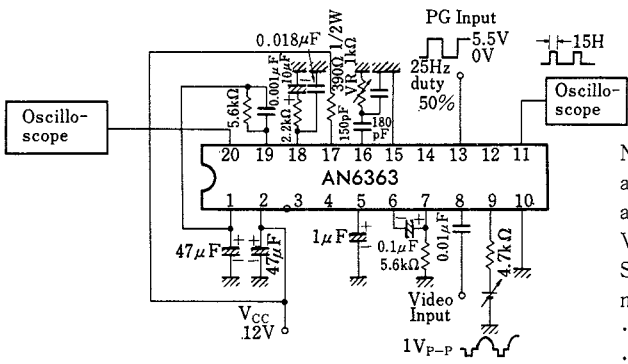
- AN6363S (S_{14-H}, S_{14-L})



Note 1) Pin⑭ DC voltages at which Pin⑮ output changes a phase by 90° at an intermediate timing of Pin⑤ output "H", and when it does not.
Note 2) Do not change the Pin⑰ variable resistor. (same as Test Circuit 2)

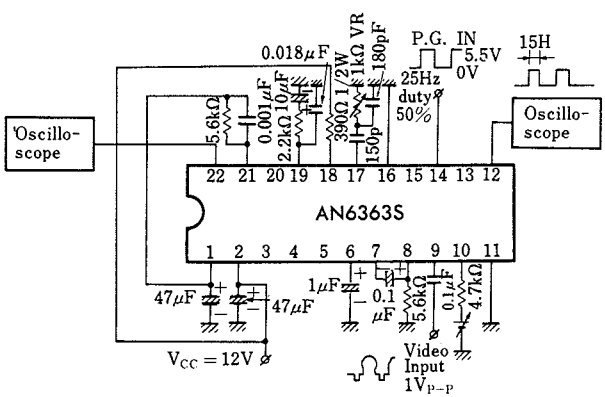
Test Circuit 7

- AN6363 (v_{O11}, S_{9-1}, S_{9-2})



Note) S_{9-1}: Pin⑨ inflow current which does not allow Pin⑪ output to be made as pulse output for about 15H after a rise/fall of Pin⑬ PG input
V_{11}: Pin⑪ output under the condition above
S_{9-2}: Pin⑨ DC voltage at which Pin⑳ output is not made at all.
· The PB mode is a Pin⑨ Open state.
· Do not change the Pin⑯ variable resistor. (same as Test Circuit 2)

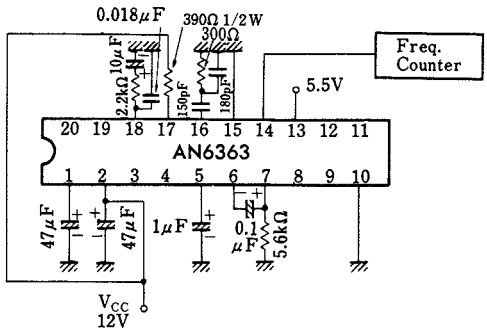
- AN6363S (v_{O12}, S_{10-1}, S_{10-2})



Note) S_{10-1}: Pin⑩ inflow current which does not allow Pin⑫ output to be made as pulse output for about 15H after a rise/fall of Pin⑭ PG input
V_{12}: Pin⑫ output under the condition above
S_{10-2}: Pin⑩ DC voltage at which Pin㉒ output is not made at all.
· The PB mode is a Pin⑩ Open state.
· Do not change the Pin⑰ variable resistor. (same as Test Circuit 2)

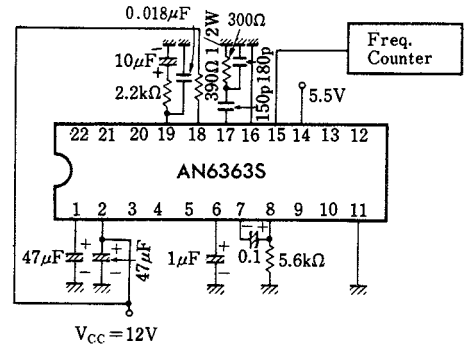
Test Circuit 8

- AN6363 (f_{OSC14})



Note) Assume a four−fold Pin⑭ output frequency as f_{14}.
f_{14}= 4 × (Pin⑭ output frequency)

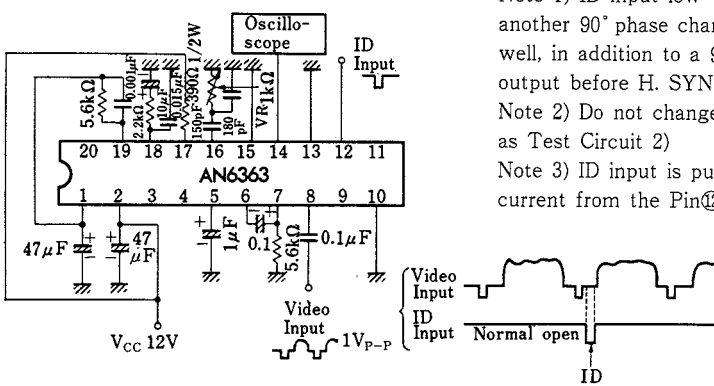
- AN6363S (f_{OSC15})



Note) Assume a four−fold Pin⑮ output frequency as f_{15}. f_{15}= 4 × (Pin⑮ output frequency)

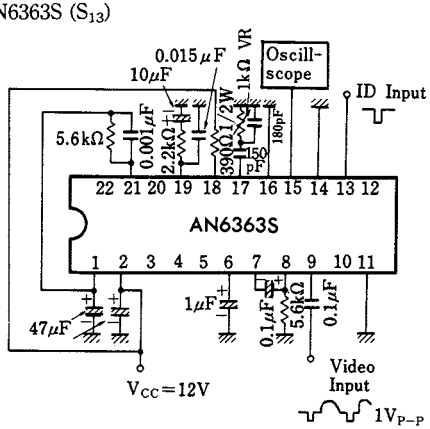
Test Circuit 9

- AN6363 (S_{12})

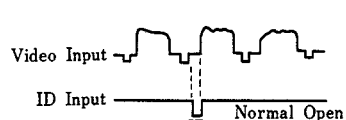


Note 1) ID input low−level voltage which causes another 90° phase change at an ID input timing as well, in addition to a 90° phase change of Pin⑭ output before H. SYNC.
Note 2) Do not change the Pin⑯ variable resistor. (same as Test Circuit 2)
Note 3) ID input is pules input which draws out a current from the Pin⑫ at a burst timing.

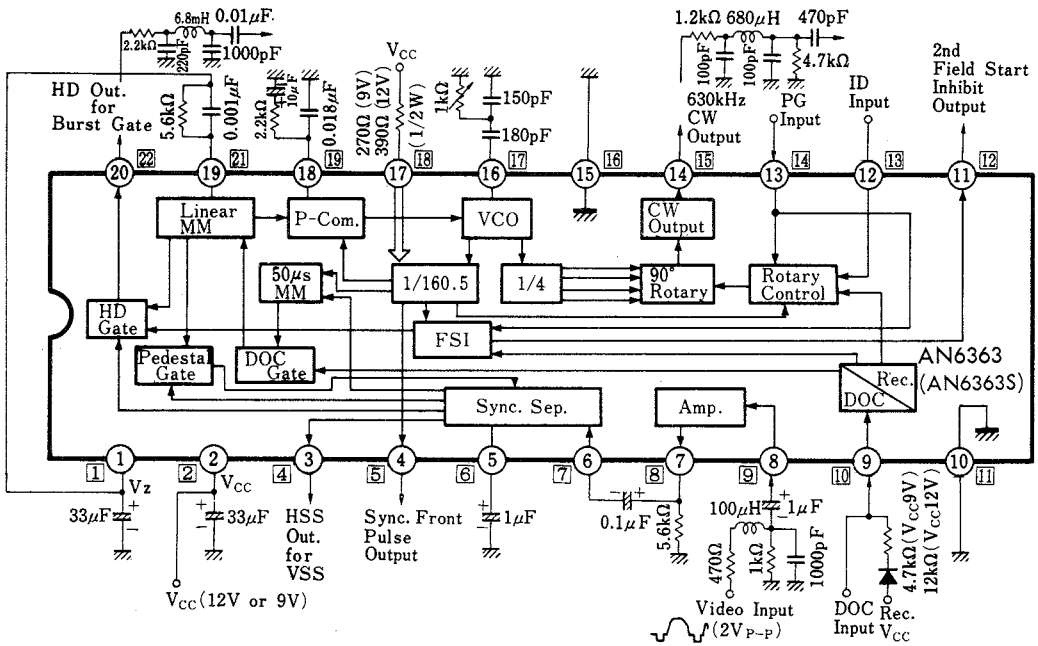
- AN6363S (S_{13})



Note 1) ID input low−level voltage which causes another 90° phase change at an ID input timing as well, in addition to a 90° phase change of Pin⑮ output before H. SYNC.
Note 2) Do not change the Pin⑰ variable resistor. (same as Test Circuit 2)
Note 3) ID input is pules input which draws out a current from the Pin⑬ at a burst timing.



■ Application Circuit



□shows the Pin No. of AN6371S

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