K4D623237M 64M DDR SGRAM

512K x 32Bit x 4 Banks Double Data Rate Synchronous Graphic RAM with Bi-directional Data Strobe

FEATURES

- 3.3V ±5% power supply for device operation
- 2.5V ±5% power supply for I/O interface
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
  - -. Read latency 2, 3 (clock)
  - -. Burst length (2, 4, 8 and Full page)
  - -. Burst type (sequential & interleave)
- Full page burst length for sequential burst type only
- Start address of the full page burst should be even
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- Data I/O transactions on both edges of Data strobe
- Data input & output & DM are synchronized with DQS
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 16ms refresh period (2K cycle)
- 100pin TQFP package
- Maximum clock frequency up to 166MHz
- Maximum data rate up to 333Mbps/pin

Graphics Features

- SMRS cycle.
  - -. Load color register
- 16 Columns Block Write.
- Byte Masking with DM for Block Write operation is supported.

ORDERING INFORMATION

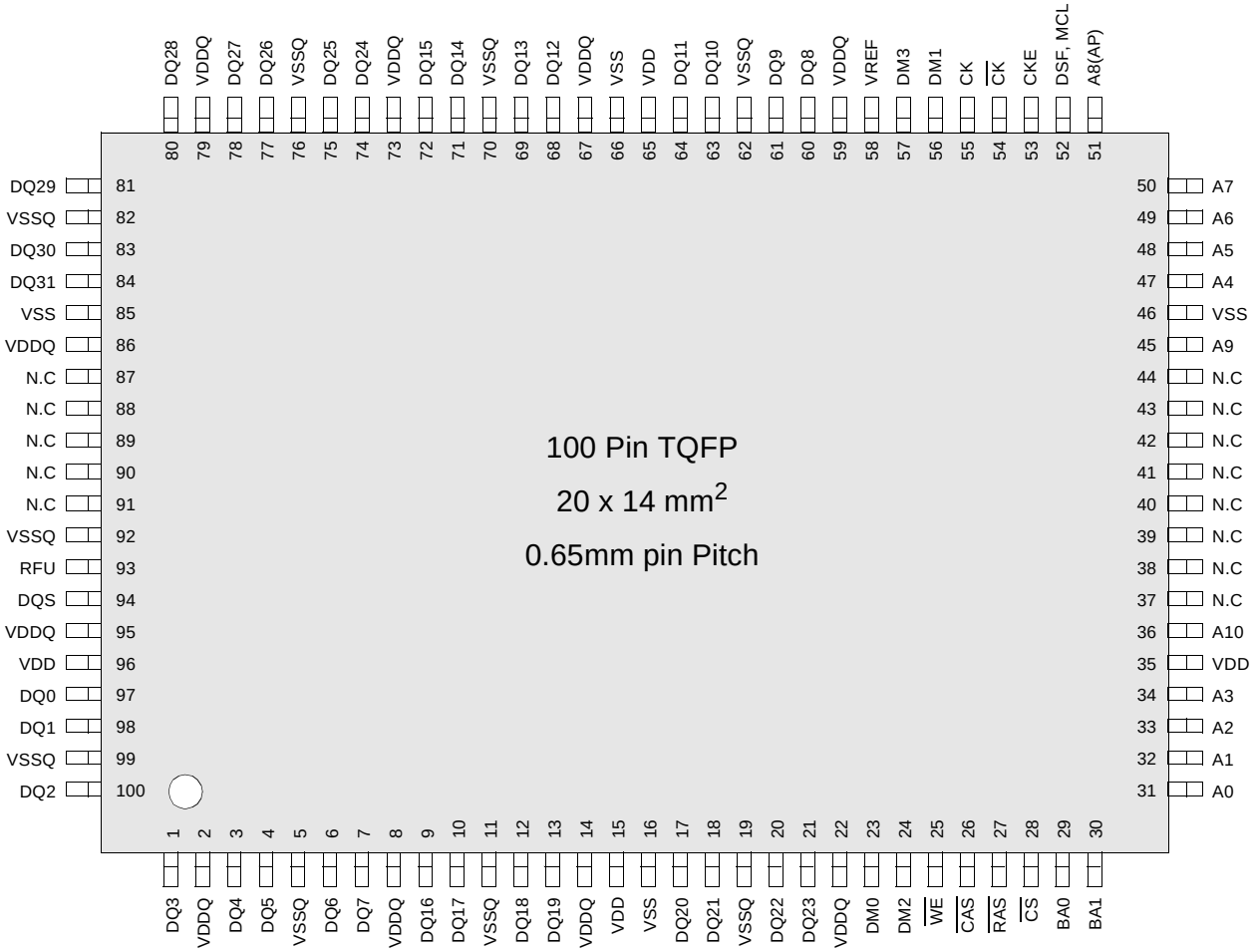
Part NO.	Max Freq.	Max Data Rate	Interface	Package
K4D623237M-QC60	166MHz	333Mbps/pin	SSTL_2	100 TQFP
K4D623237M-QC70	143MHz	286Mbps/pin		
K4D623237M-QC80	125MHz	250Mbps/pin		
K4D623237M-QC10	100MHz	200Mbps/pin		

GENERAL DESCRIPTION

FOR 512K x 32Bit x 4 Bank DDR SGRAM

The K4D623237 is 67,108,864 bits of hyper synchronous data rate Dynamic GRAM organized as 4 x 524,288 words by 32 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 1.328GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

PIN CONFIGURATION (Top View)



PIN DESCRIPTION

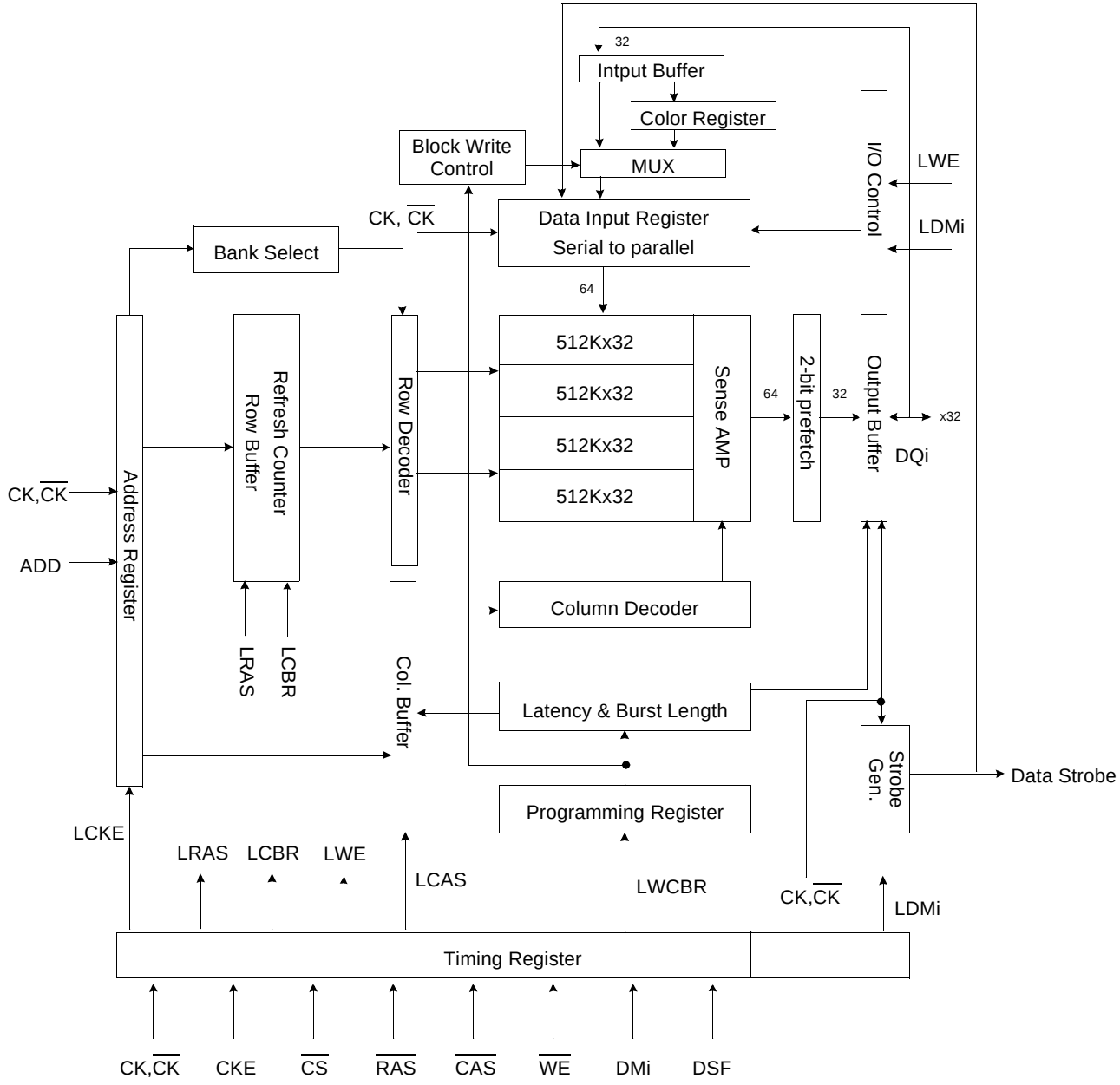
CK,$\overline{CK}$	Differential Clock Input	BA_0, BA_1	Bank Select Address
CKE	Clock Enable	A_0 ~A_{10}	Address Input
$\overline{CS}$	Chip Select	DQ_0 ~ DQ_{31}	Data Input/Output
$\overline{RAS}$	Row Address Strobe	V_{DD}	Power
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE}$	Write Enable	V_{DDQ}	Power for DQ′s
DQS	Data Strobe	V_{SSQ}	Ground for DQ′s
DMi	Data Mask	DSF	Define Special Function
RFU	Reserved for Future Use	MCL	Must Connect Low

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, $\overline{CK}$*1	Input	The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ′s and DM′s that are sampled on both edges of the DQS.
CKE	Input	Activates the CK signal when high and deactivates the CK signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode.
$\overline{CS}$	Input	$\overline{CS}$ enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$	Input	Latches row addresses on the positive going edge of the CK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Input	Latches column addresses on the positive going edge of the CK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Input	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQS	Input/Output	Data input and output are synchronized with both edge of DQS.
DM_0 ~ DM_3	Input	Data In mask. Data In is masked by DM Latency=0 when DM is high in burst write. DM_0 for DQ_0 ~ DQ_7, DM_1 for DQ_8 ~ DQ_{15}, DM_2 for DQ_{16} ~ DQ_{23}, DM_3 for DQ_{24} ~ DQ_{31}.
DQ_0 ~ DQ_{31}	Input/Output	Data inputs/Outputs are multiplexed on the same pins.
BA_0, BA_1	Input	Selects which bank is to be active.
A_0 ~ A_{10}	Input	Row/Column addresses are multiplexed on the same pins. Row addresses : RA_0 ~ RA_{10}, Column addresses : CA_0 ~ CA_7. Column address CA_8 is used for auto precharge.
V_{DD}/V_{SS}	Power Supply	Power and ground for the input buffers and core logic.
V_{DDQ}/V_{SSQ}	Power Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	Power Supply	Reference voltage for inputs, used for SSTL interface.
DSF, MCL	Define Special Function	Enables block write and special mode register set and must be connected low to disable these special functions.

*1 : The timing reference point for the differential clocking is the cross point of CK and $\overline{CK}$.
For any applications using the single ended clocking, apply V_{REF} to $\overline{CK}$ pin.

BLOCK DIAGRAM (512Kbit x 32I/O x 4 Bank)



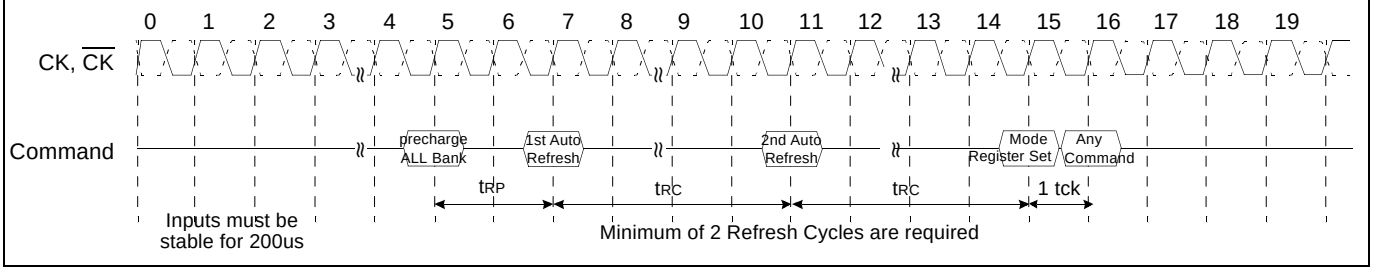
FUNCTIONAL DESCRIPTION

• Power-Up Sequence

DDR SGRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

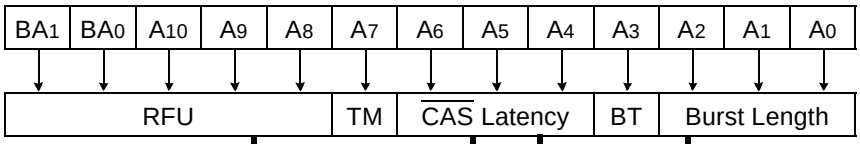
1. Apply power and keep CKE at low state (All other inputs may be undefined)
   - Apply VDD before VDDQ .
   - Apply VDDQ before VREF & VTT
2. Start clock and maintain stable condition for a minimum of 200us.
3. The minimum of 200us after stable power and clock(CK,$\overline{CK}$), apply NOP and take CKE to be high .
4. Issue precharge command for all banks of the device.
5. Issue at least 2 or more auto-refresh commands.
6. Issue a mode register set command to initialize the mode register.
   cf) Sequence of 4 & 5 is regardless of the order.

Power up Sequence & Auto Refresh(CBR)



MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of DDR SGRAM. It programs CAS latency, addressing mode, burst length, test mode and various vendor specific options to make DDR SGRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the DDR SGRAM. The mode register is written by asserting low on CS, RAS, CAS and WE(The DDR SGRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A_0 ~ A_{10} and BA_0, BA_1 in the same cycle as CS, RAS, CAS and WE going low is written in the mode register. One clock cycle is requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A_0 ~ A_2, addressing mode uses A_3, CAS latency(read latency from column address) uses A_4 ~ A_6. A_7 is used for test mode. A_7, A_8, BA_0 and BA_1 must be set to low for normal DDR SGRAM operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



A_7	mode
0	Normal
1	Test

Burst Type

A_3	Type
0	Sequential
1	Interleave

CAS Latency

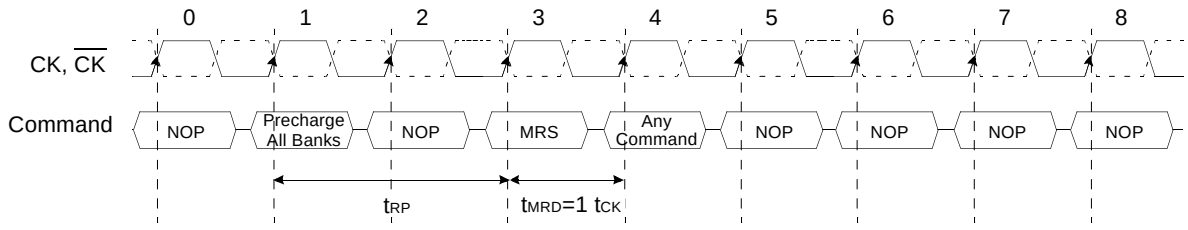
A_6	A_5	A_4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	2
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

Burst Length

A_2	A_1	A_0	Burst Type	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full page	Reserve

* RFU(Reserved for future use) should stay "0" during MRS cycle.

MRS Cycle



*1 : MRS can be issued only at all banks precharge state.
*2 : Minimum t_{RP} is required to issue MRS command.

DEFINE SPECIAL FUNCTION(DSF)

The DSF controls the graphic applications of SGRAM. If DSF is tied to low, SGRAM functions are the same as SDRAM functions. SGRAM can be used as an unified memory by the appropriate DSF command. All the graphic function mode can be entered only by setting DSF high when issuing commands which otherwise would be normal SDRAM commands.

See the sessions below for the graphic functions that DSF control.

SPECIAL MODE REGISTER SET(SMRS)

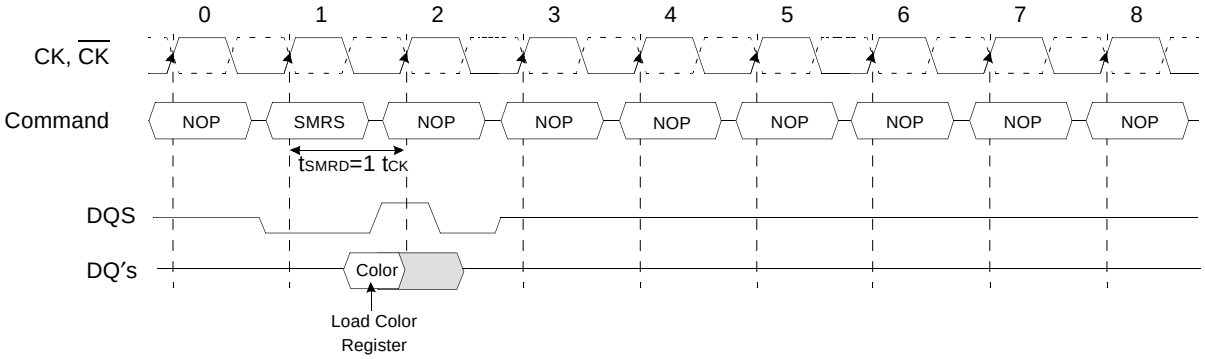
There is a special mode register in DDR SGRAM. It is color register. This usage will be explained at "BLOCK WRITE" session. When A6 and DSF goes high in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low, load color register(LCR) process is executed and the color register is filled with color data for associated DQ′s through the DQ pins. At the next clock of LCR, a new commands can be issued. SMRS, compared with MRS, can be issued at the active state under the condition that DQ′s are idle.

Special Mode Register Programmed with SMRS

Address	BA_1	BA_0	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	X						LC	X					

Load Color Register	
A_6	Function
0	Disable
1	Enable

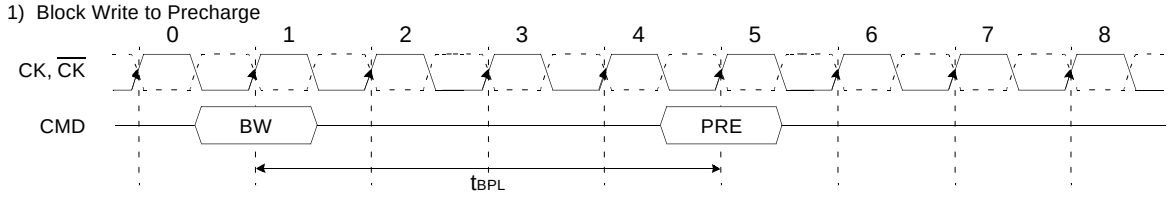
SMRS Cycle



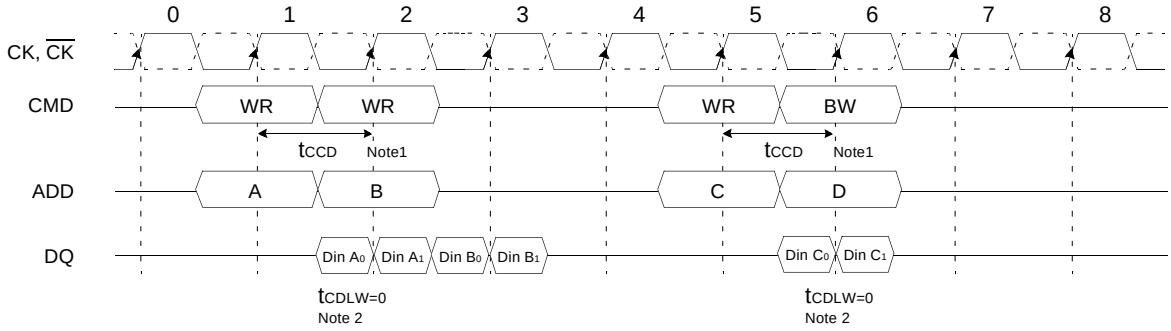
BLOCK WRITE

Block write is a feature allowing the simultaneous writing of consecutive 16 columns of data within a RAM device during a single access cycle. During block write the data to be written comes from an internal "color" register. The block of column to be written is aligned on 16 column boundaries and is defined by the column address with the 4 LSB′s ignored. Write command with DSF=High enables block write for the associated bank. A write command with DSF=Low enables normal write for the associated bank. The block width is 16 column where column="n" bits for by "n" part. The color register is the same width as the data port of the chip. The color register provides the data without column masking. So DQ states are don′t cared. And Null Column Mask command with high state on DQs make no problem. DQS should toggle once for valid data mask(DM) input. Block writes are always non-burst, independent of the burst length that has been programmed into the mode register. Back to back block writes are allowed provided that the specified block write cycle time(tBWC) is satisfied.

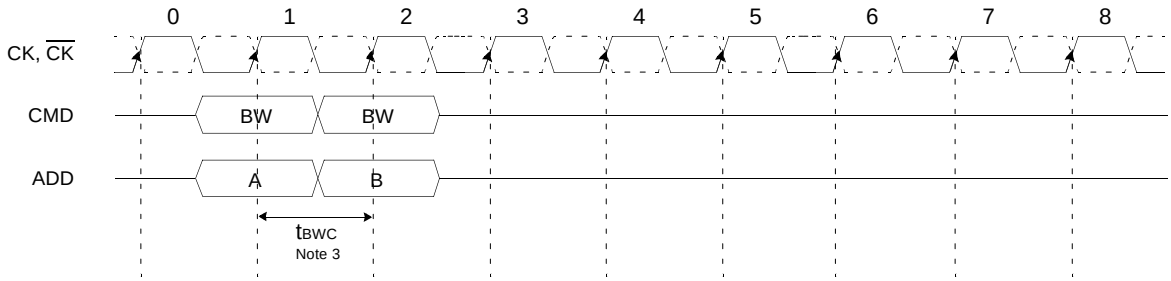
1) Block Write to Precharge



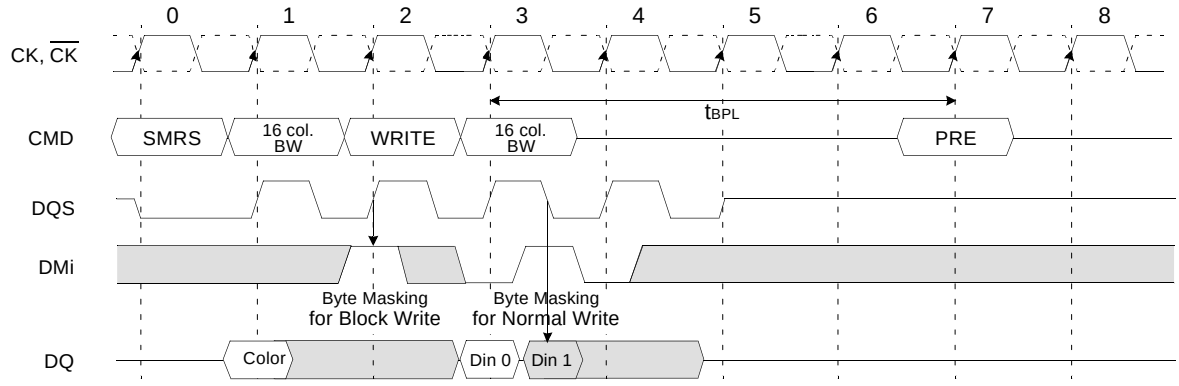
2) Write interrupted by Block Write (BL=2)



3) Block Write to Block Write



4) Byte Masking for Block Write



***Note :** 1. t_{CCD} : $\overline{CAS}$ to $\overline{CAS}$ delay. (=1 tCK)
2. t_{CDLW} : Last data in to new column address delay. (=0 tCK)
3. t_{BWC} : Block write minimum cycle time. (=1 tCK)

BURST MODE OPERATION

Burst mode operation is used to provide a constant flow of data to memory locations(write cycle), or from memory locations(read cycle). There are two parameters that define how the burst mode operates. These parameters including burst sequence and burst length are programmable and determined by address bits A_0 ~ A_3 during the Mode Register Set command. The burst type is used to define the sequence in which the burst data will be delivered or stored to the SGRAM. Two types of burst sequences are supported, sequential and interleaved. See the below table. The burst length controls the number of bits that will be output after a read command, or the number of bits to be input after a write command. The burst length can be programmed to have values of 2, 4, 8 or Full page. For the full page operation, the starting address must be an even number.

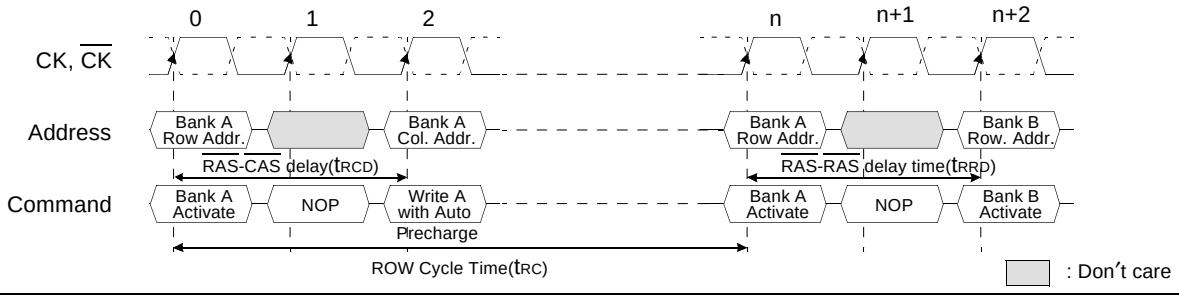
BURST LENGTH AND SEQUENCE

Burst Length	Starting Address(A_2, A_1, A_0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

BANK ACTIVATION COMMAND

The Bank Activation command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The DDR SGRAM has four independent Banks, so two Bank Select addresses(BA_0, BA_1) are supported. The Bank Activation command must be applied before any Read or Write operation is executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time(t_{RCD} min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to Bank B and vice versa) is the Bank to Bank delay time(t_{RRD} min).

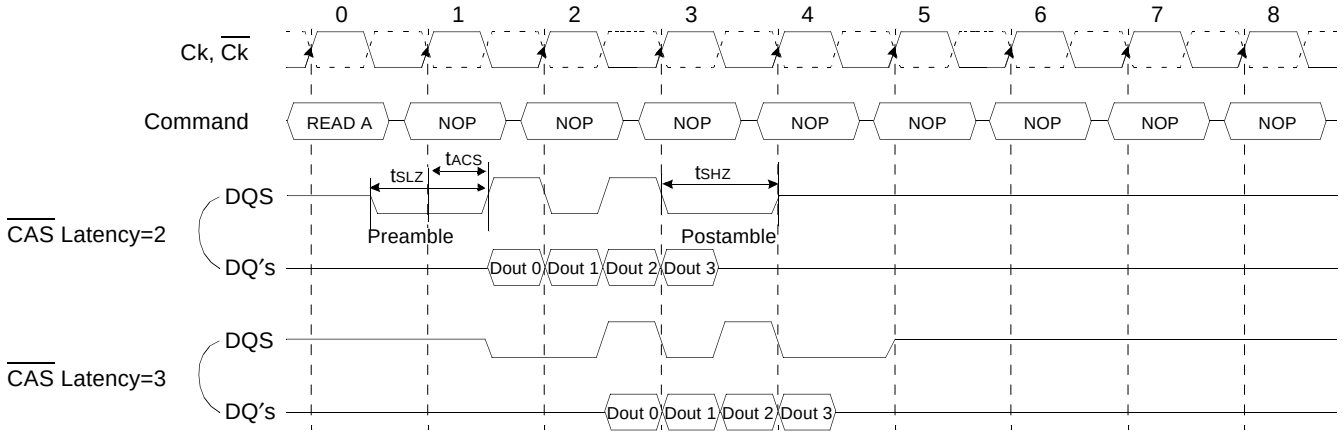
Bank Activation Command Cycle ($\overline{CAS}$ Latency = 2)



BURST READ OPERATION

Burst Read operation in DDR SGRAM is in the same manner as the current SDRAM such that the Burst read command is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock after t_{RCD} from the bank activation. The address inputs (A_0~A_7) determine the starting address for the Burst. The Mode Register sets type of burst(sequential or interleave) and burst length(2, 4, 8, Full page). The first output data is available after the $\overline{CAS}$ Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe adopted by DDR SGRAM until the burst length is completed.

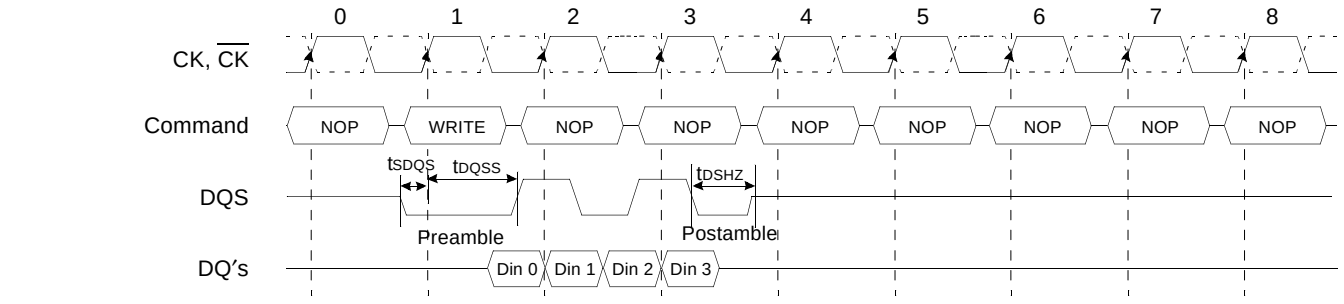
< Burst Length=4, $\overline{CAS}$ Latency=2, 3 >



BURST WRITE OPERATION

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. There is no real write latency required for burst write cycle. The first data for burst write cycle must be applied at the first rising edge of the data strobe enabled after t_{DQSS} from the rising edge of the clock that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

< Burst Length=4 >

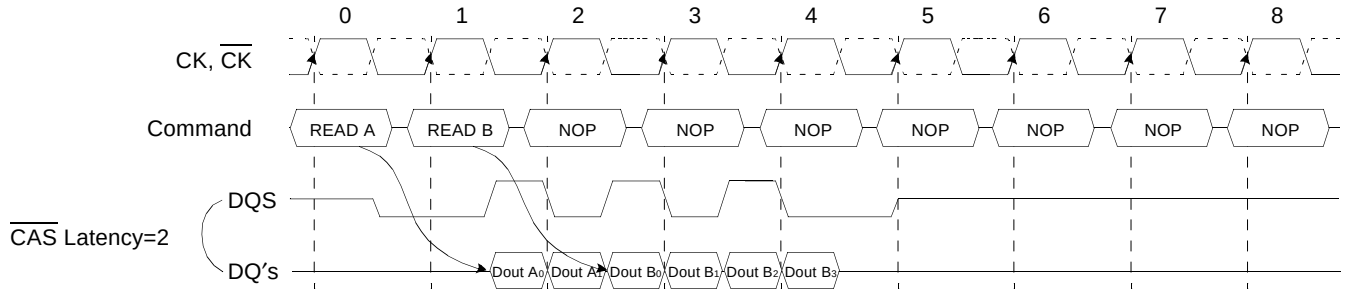


BURST INTERRUPTION

Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is minimum 1 tck.

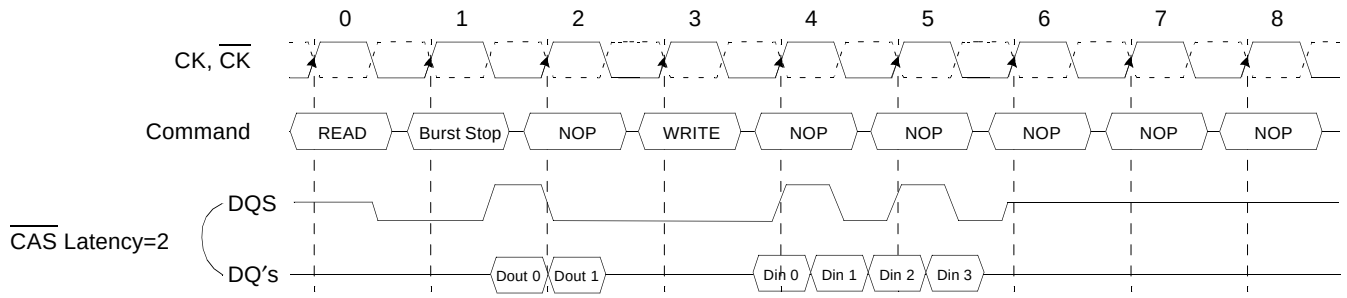
< Burst Length=4, $\overline{CAS}$ Latency=2 >



Read Interrupted by Burst stop & a Write

To interrupt a burst read with a write command, Burst stop command must be asserted to avoid data contention on the I/O bus by placing the DQ's(Output drivers) in a high impedance state at least one clock cycle before the Write Command is initiated.

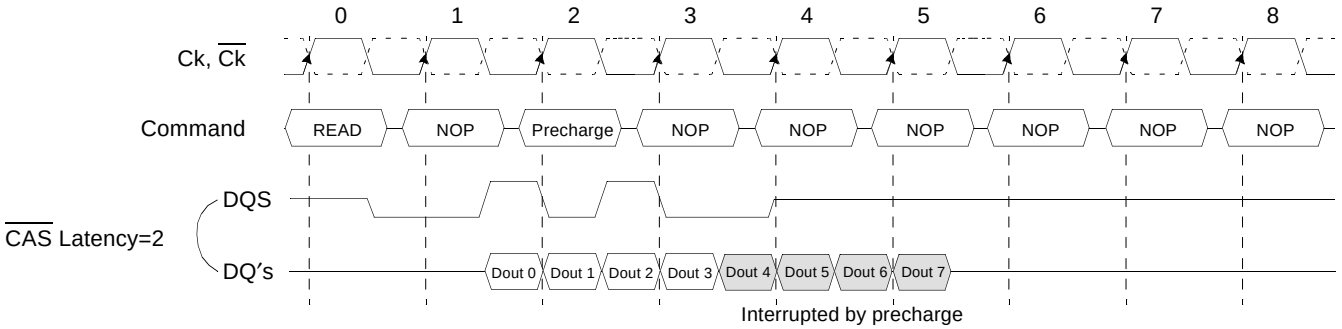
< Burst Length=4, $\overline{CAS}$ Latency=2 >



Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the Read to precharge intervals without interrupting a Read burst. A precharge command to output disable latency is equivalent to the CAS latency.

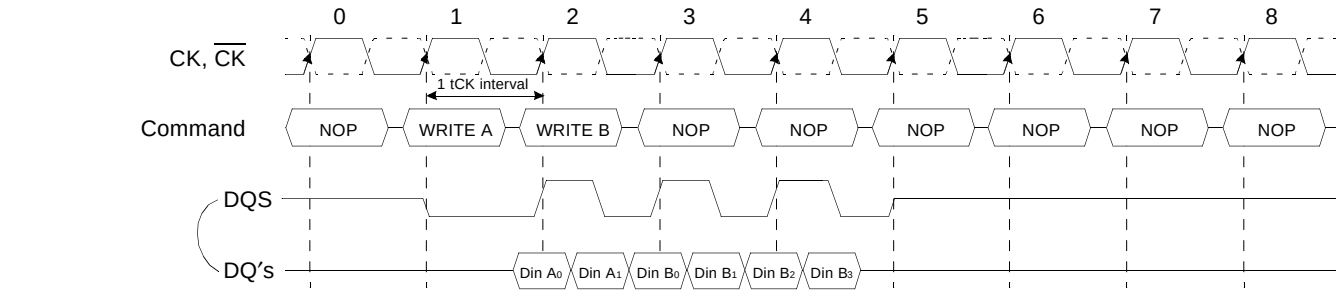
< Burst Length=8, CAS Latency=2 >



Write Interrupted by a Write

A Burst Write can be interrupted before completion of the burst by the new Write Command, with the only restriction being that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

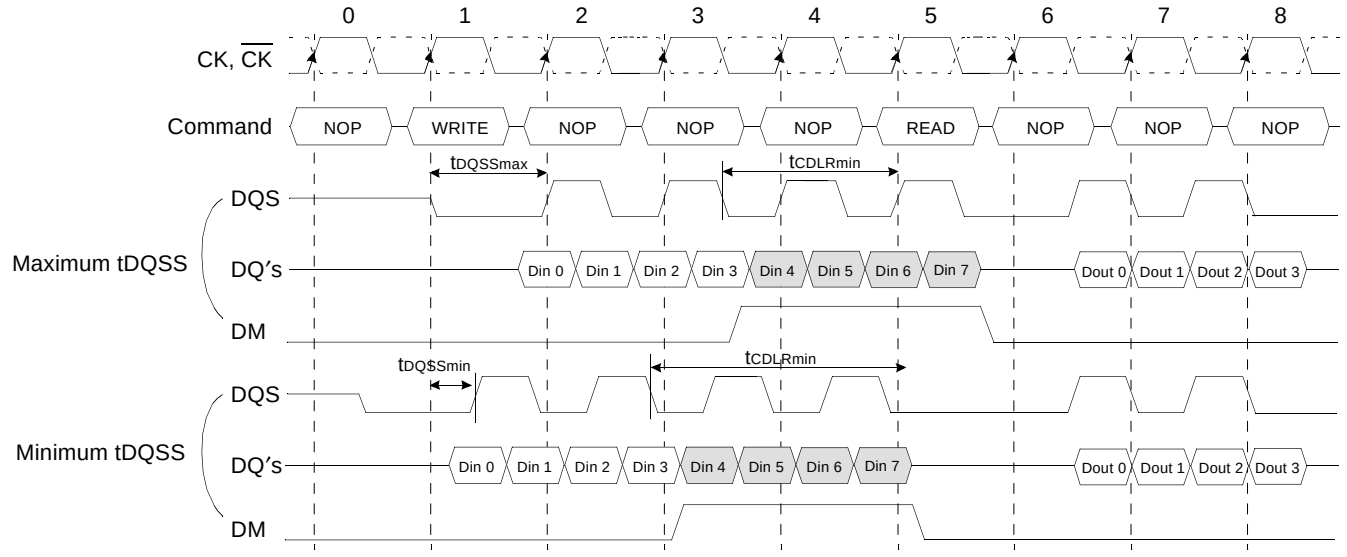
< Burst Length=4 >



Write Interrupted by a Read & DM

A Burst Write can be interrupted by a Read command to any bank. The DQ′s must be in the high impedance state at least one clock cycle before interrupting read data appears on the outputs to avoid data contention. When the Read Command is registered, any residual data from the burst write cycle will be masked by DM. The delay from the last data to Read command (tCDLR) is required to avoid the data contention DRAM inside.

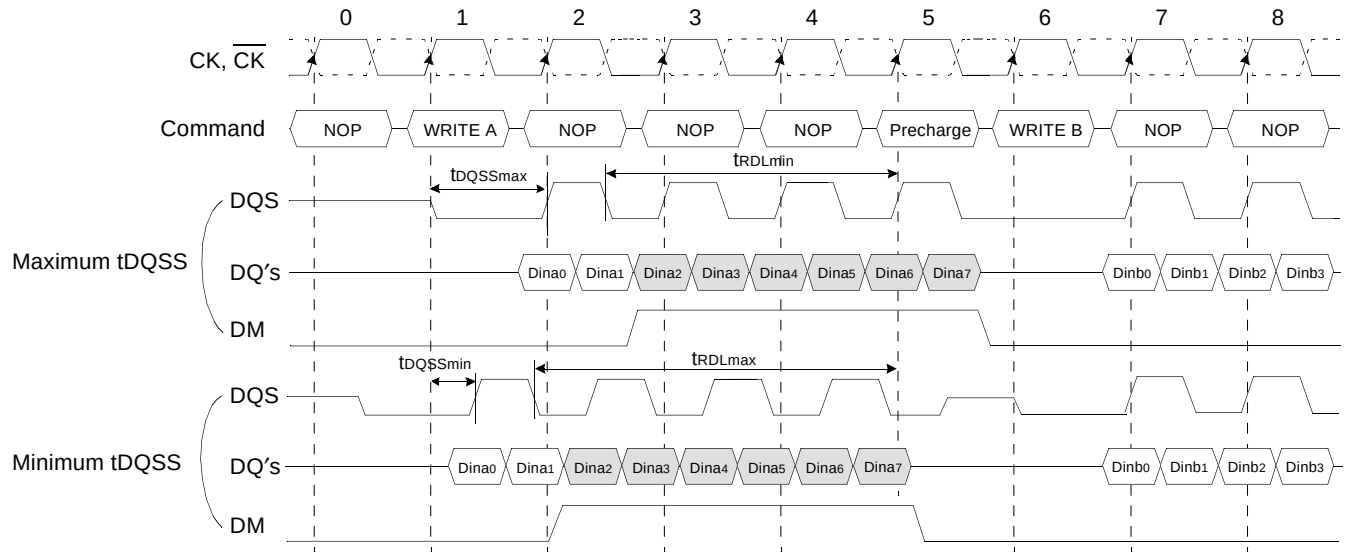
< Burst Length=8, $\overline{\text{CAS}}$ Latency=2 >



Write Interrupted by a Precharge & DM

A Burst Write operation can be interrupted before completion of the burst by a precharge of the same bank. A Write Recovery time(tRDL) is required before a Precharge command to finish the Write operation. When Precharge command is asserted, any residual data from the burst write cycle must be masked by DM.

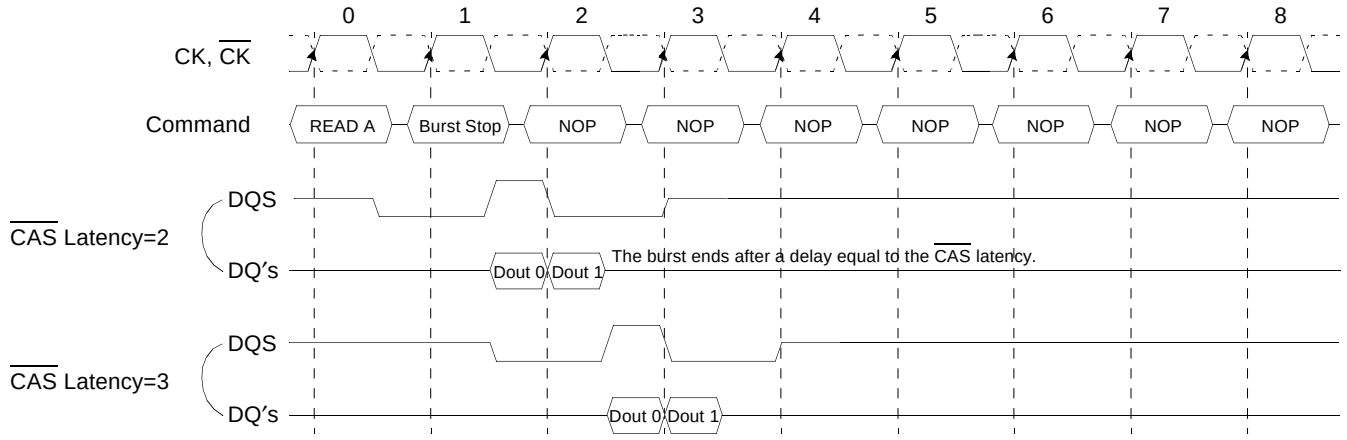
< Burst Length=8 >



BURST STOP COMMAND

The Burst stop command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock only . The Burst Stop command has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. When the Burst Stop command is issued during a burst read cycle, both the data and DQS(Data Strobe) go to a high impedance state after a delay which is equal to the $\overline{CAS}$ Latency set in the Mode Register. The Burst Stop command, however, is not supported during a write burst operation.

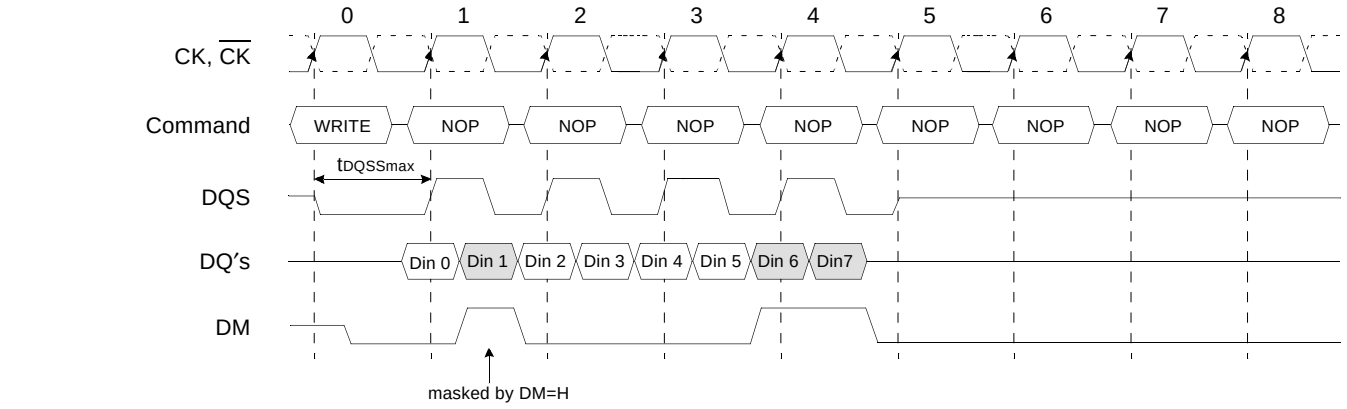
< Burst Length=4, $\overline{CAS}$ Latency=2, 3 >



DM FUNCTION

The DDR SGRAM has a Data mask function that can be used in conjunction with data Write cycle only, not Read cycle. When the Data Mask is activated (DM high) during write operation the write data is masked immediately(DM to Data-mask Latency is zero).
DM must be issued at the rising edge or the falling edge of Data Strobe instead of a clock edge.

< Burst Length=8 >

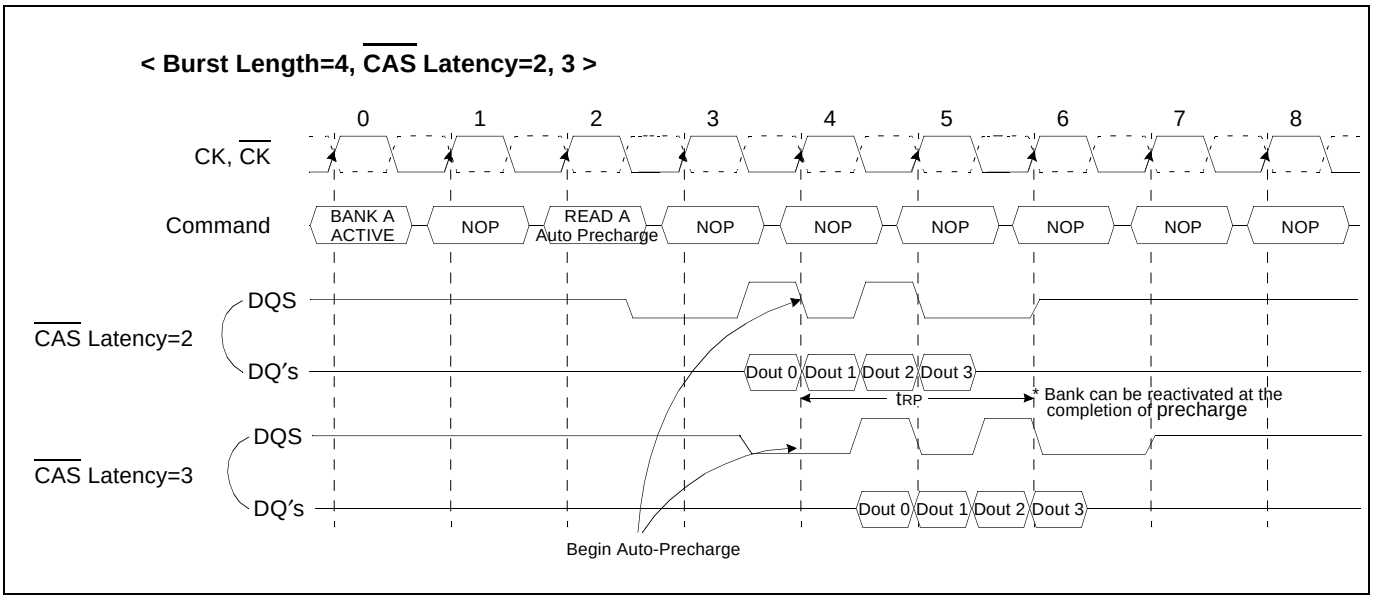


AUTO-PRECHARGE OPERATION

The Auto precharge command can be issued by having column address A_8 High when a Read or a Write command is asserted into the DDR SGRAM. If A_8 is low when Read or Write command is issued, then normal Read or Write burst operation is asserted and the bank remains active after the completion of the burst sequence. When the Auto precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during read or write cycle after t_{RAS}(min) is satisfied.

Read with Auto Precharge

If a Read with Auto-precharge command is initiated, the DDR SGRAM automatically starts the precharge operation on BL/2 clock later from a Read with Auto-Precharge command when t_{RAS}(min) is satisfied. If not, the start point of precharge operation will be delayed until t_{RAS}(min) is satisfied. Once the precharge operation has started the bank cannot be reactivated and the new command can not be asserted until the Precharge time(t_{RP}) has been satisfied.



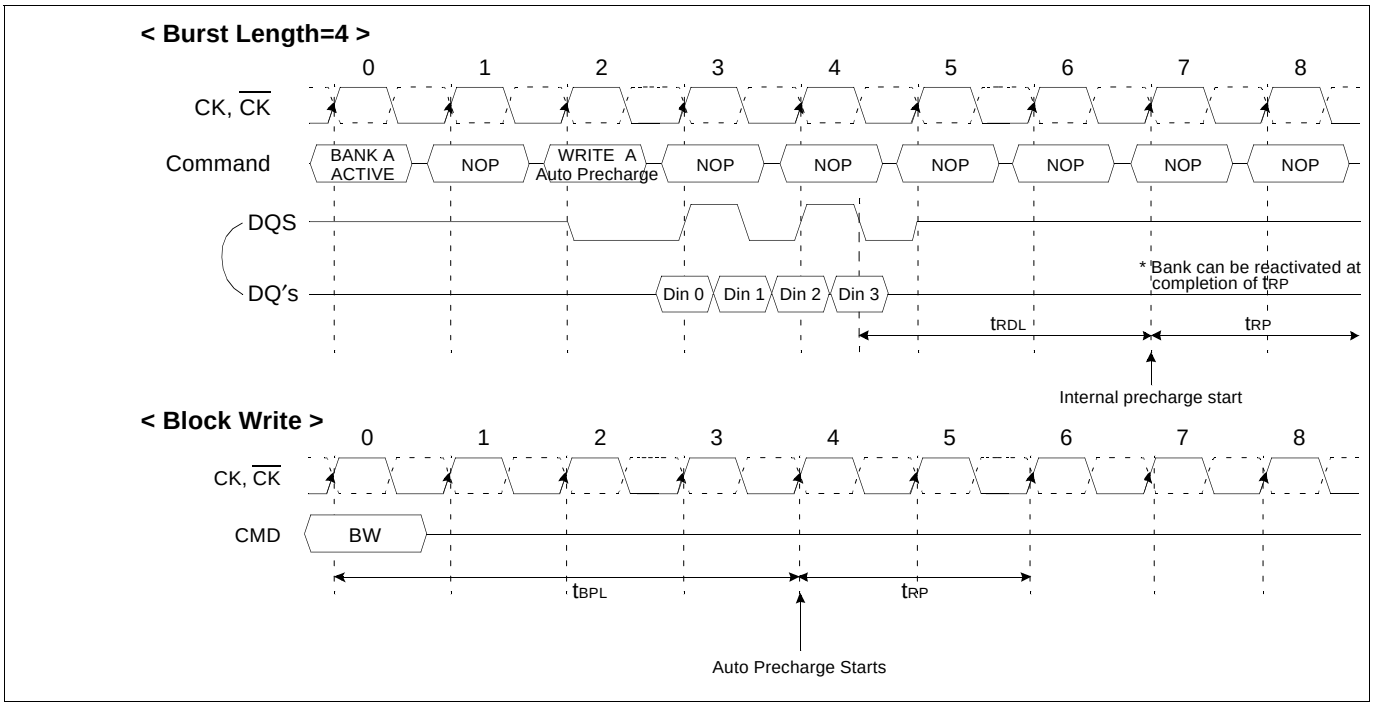
When the Read with Auto precharge command is issued, new command can be asserted at T3,T4 and T5 respectively as follows, even the new command for the same bank is illigal.

Asserted command	For same Bank			For Different Bank		
	3	4	5	3	4	5
Read Interrupt	READ + NO AP*1	READ+ NO AP	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Fail	Legal	Legal	Legal
Precharge	Illegal	Illegal	Fail	Legal	Legal	Legal

*1 : AP = Auto Precharge

Write with Auto Precharge

If A_8 is high when Write command is issued , the write with Auto-Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping t_{RDL}(min).



PRECHARGE COMMAND

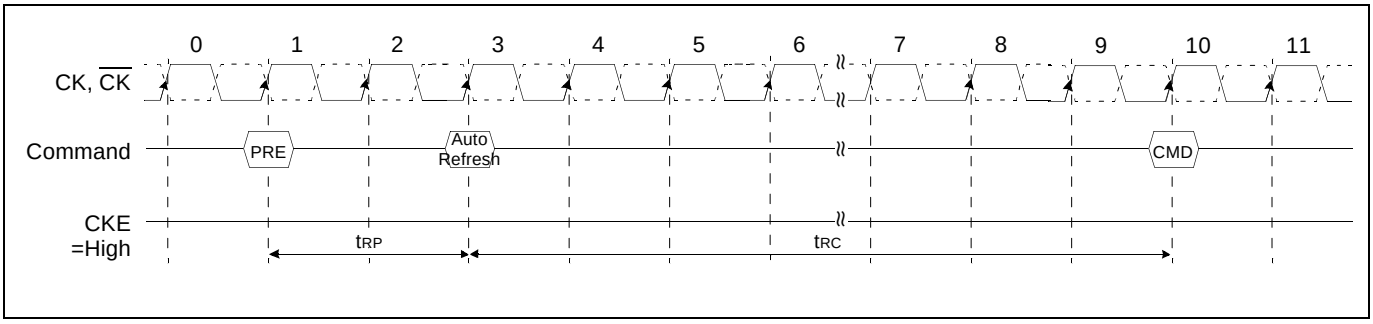
The precharge command is used to precharge or close a bank that has been activated. The precharge command is issued when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock, CK. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The Bank select addresses(BA_0, BA_1) are used to define which bank is precharged when the command is initiated. For write cycle, t_{RDL}(min.) must be satisfied from the start of the last burst write cycle until the precharge command can be issued. After t_{RP} from the precharge, an active command to the same bank can be initiated.

< Bank Selection for Precharge by Bank address bits >

A_8/AP	BA1	BA_0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

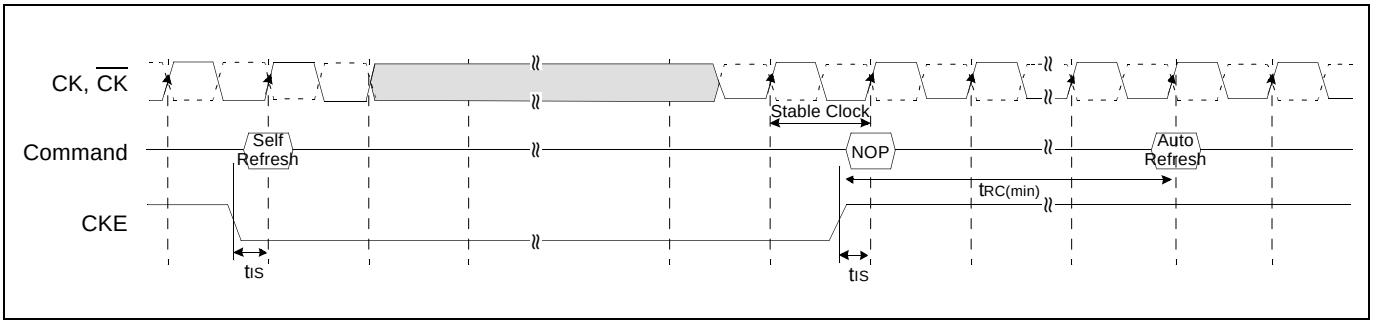
AUTO REFRESH

An Auto Refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock, CK. All banks must be precharged and idle for a t_{RP}(min) before the Auto Refresh command is applied. No control of the external address pins is required once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the t_{RFC}(min).



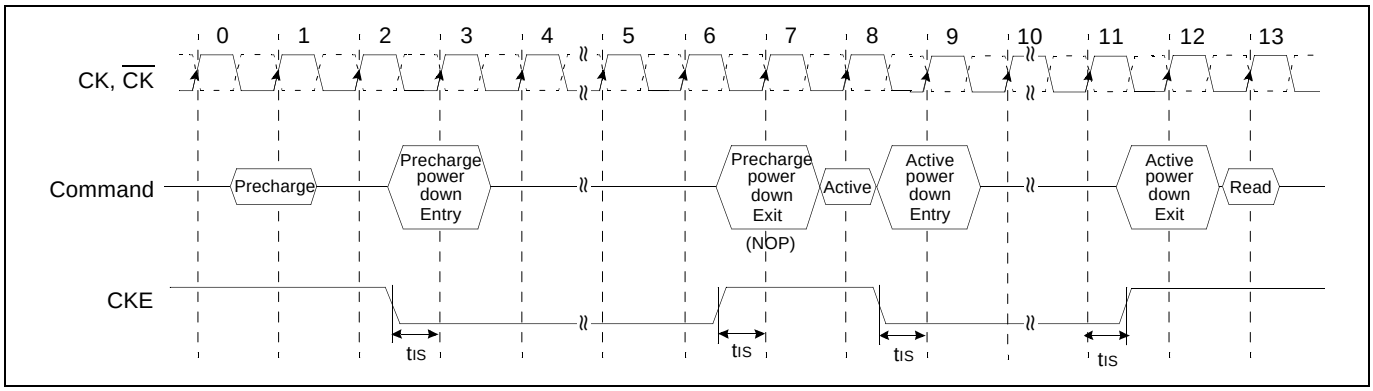
SELF REFRESH

A Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. After 1 clock cycle from the self refresh command, all of the external control signals including system clock(CK, $\overline{CK}$) can be disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. To exit the Self Refresh mode, supply stable clock input before returning CKE high, assert deselect or NOP command and then assert CKE high. The Auto Refresh is required before self refresh entry and after self refresh exit.



POWER DOWN MODE

The power down is entered when CKE Low,and exited when CKE High. Once the power down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. The both bank should be in idle state prior to entering the precharge power down mode and CKE should be set high at least 1 tCK+tIS prior to Row active command. During power down mode, refresh operations cannot be performed, therefore the device cannot remain in power down mode longer than the refresh period(tREF) of the device.



SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DM	$BA_{0,1}$	A_8/AP	A_{10},A_9,A_7~A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	L	X	OP CODE			1, 2
	Special Mode Register Set								H					
Refresh	Auto Refresh		H	H	L	L	L	H	X	X	X			3
	Self Refresh	Entry		L										3
		Exit	L	H	L	H	H	H	X	X	X			3
					H	X	X	X						3
Bank Active & Row Addr.			H	X	L	L	H	H	X	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	X	V	L	Column Address	4
	Auto Precharge Enable											H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	L	X	V	L	Column Address	4
	Auto Precharge Enable											H		4, 6
Block Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	H	X	V	L	Column Address	4, 5
	Auto Precharge Enable											H		4,5,6,9
Burst Stop			H	X	L	H	H	L	X	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	X	X	V	L	X	
	All Banks										X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X	X	X			
					L	V	V	V						
		Exit	L	H	X	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X	X			
					L	H	H	H						
		Exit	L	H	H	X	X	X	X	X				
					L	H	H	H	X					
DM			H	X						V	X			8
No Operation Command			H	X	H	X	X	X	X	X	X			
					L	H	H	H						

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{10} & BA_0 ~ BA_1 : Program keys. (@MRS)
A_6 : LCR @ SMRS/Color register exists only one per DQi which all banks share.
Color is loaded into chip through DQ pin
2. MRS can be issued only at all banks precharge state.
SMRS can be issued only if DQ's are idle.
A new command can be issued after 1 clock cycle of MRS/SMRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_8/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. Graphic features are added to SDRAM′s original features.
   If DSF is tied to low, graphic functions are disabled and chip operates as a 64M SDRAM with 32 DQ′s.

FUNCTION TRUTH TABLE

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Action
IDLE	H	X	X	X	X	X	DESEL	NOP
	L	H	H	H	X	X	NOP	NOP
	L	H	H	L	X	X	TERM	NOP
	L	H	L	X	X	BA, CA, A_8	READ/WRITE/BW	ILLEGAL*2
	L	L	H	H	X	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	X	BA, A_8	PRE/PREA	NOP*4
	L	L	L	H	X	X	REFA	AUTO-Refresh*5
	L	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
					H		SMRS	Special Mode Register Set
ROW ACTIVE	H	X	X	X	X	X	DESEL	NOP
	L	H	H	H	X	X	NOP	NOP
	L	H	H	L	X	X	TERM	NOP
	L	H	L	H	X	BA, CA, A_8	READ/READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	L	BA, CA, A_8	WRITE/WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	H	L	L	H	BA, CA, A_8	BW/BWA	Begin Block Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	X	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	X	BA, A_8	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	X	REFA	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
					H		SMRS	Special Mode Register Set
READ	H	X	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	X	TERM	Terminate Burst
	L	H	L	H	L	BA, CA, A_8	READ/READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	X	BA, CA, A_8	WRITE/WRITEA BW/BWA	ILLEGAL
	L	L	H	H	L	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	L	BA, A_8	PRE/PREA	Terminate Burst, Precharge
	L	L	L	H	X	X	REFA	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
					H		SMRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Action
WRITE	H	X	X	X	X	X	DESEL	NOP(Continue Burst END)
	L	H	H	H	X	X	NOP	NOP(Continue Burst END)
	L	H	H	L	X	X	TERM	ILLEGAL
	L	H	L	H	X	BA, CA, A_8	READ/READA	Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Precharge*3
	L	H	L	L	L	BA, CA, A_8	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge*3
	L	H	L	L	H	BA, CA, A_8	BW/BWA	Terminate Burst , Latch CA, New Block Write, Determine AP.
	L	L	H	H	X	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	X	BA, A_8	PRE/PREA	Terminate Burst With DM=High, Precharge
	L	L	L	H	X	X	REFA	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
					H		SMRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	X	DESEL	NOP(Continue Burst END)
	L	H	H	H	X	X	NOP	NOP(Continue Burst END)
	L	H	H	L	X	X	TERM	ILLEGAL
	L	H	L	X	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	X	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	X	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	X	REFA	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
					H		SMRS	ILLEGAL
WRITE with AUTO RECHARGE	H	X	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	X	TERM	ILLEGAL
	L	H	L	X	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	X	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	X	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	X	REFA	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
					H		SMRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Action
BLOCK WRITE RECOVERING	H	X	X	X	X	X	DESEL	NOP(Continue Block Write)
	L	H	H	H	X	X	NOP	NOP(Continue Block Write)
	L	H	H	L	X	X	TERM	NOP
	L	H	L	X	X	BA, CA, A_8	READ/READA WRITE/ WRITEA	ILLEGAL
	L	L	H	H	X	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	X	BA, A_8	PRE/PREA	Terminate Block Write, Pre-charge
	L	L	L	H	X	X	REFA	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
					H		SMRS	ILLEGAL
PRE-CHARGING	H	X	X	X	X	X	DESEL	NOP(Idle after t_{RP})
	L	H	H	H	X	X	NOP	NOP(Idle after t_{RP})
	L	H	H	L	X	X	TERM	NOP
	L	H	L	X	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	X	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	X	BA, A_8	PRE/PREA	NOP*4(Idle after t_{RP})
	L	L	L	H	X	X	REFA	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
					H		SMRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	X	DESEL	NOP(ROW Active after t_{RCD})
	L	H	H	H	X	X	NOP	NOP(ROW Active after t_{RCD})
	L	H	H	L	X	X	TERM	NOP
	L	H	L	X	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	X	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	X	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	X	REFA	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
					H		SMRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Action
WRITE RECOVERING	H	X	X	X	X	X	DESEL	NOP
	L	H	H	H	X	X	NOP	NOP
	L	H	H	L	X	X	TERM	NOP
	L	H	L	H	X	BA, CA, A_8	READ	ILLEGAL*2
	L	H	L	L	L	BA, CA, A_8	WRITE/WRITEA	New Write, Determine AP.
	L	H	L	L	H	BA, CA, A_8	BW/BWA	New BW, Determine AP.
	L	L	H	H	X	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	X	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	X	REFA	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
					H		SMRS	ILLEGAL
RE-FRESHING	H	X	X	X	X	X	DESEL	NOP(Idle after t_{RP})
	L	H	H	H	X	X	NOP	NOP(Idle after t_{RP})
	L	H	H	L	X	X	TERM	NOP
	L	H	L	X	X	BA, CA, A_8	READ/WRITE	ILLEGAL
	L	L	H	H	X	BA, RA	ACT	ILLEGAL
	L	L	H	L	X	BA, A_8	PRE/PREA	ILLEGAL
	L	L	L	H	X	X	REFA	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
					H		SMRS	ILLEGAL

ABBREVIATIONS :

H=High Level, L=Low level, V=Valid, X=Don′t Care

BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

Note :

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state ; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle sate. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.
6. Same Bank′s previous Auto precharge will not be performed. But if Bank is different, previous Auto precharge will be performed.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

FUNCTION TRUTH TABLE for CKE

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Add	Action
SELF-REFRESHING	H	X	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	X	Exit Self-Refresh*1
	L	H	L	H	H	H	X	X	Exit Self-Refresh*1
	L	H	L	H	H	L	X	X	ILLEGAL
	L	H	L	H	L	X	X	X	ILLEGAL
	L	H	L	L	X	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	X	NOP(Maintain Self-Refresh)
Both Bank Precharge POWER DOWN	H	X	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	X	Exit Power Down*2
	L	H	L	H	H	H	X	X	Exit Power Down*2
	L	H	L	H	H	L	X	X	ILLEGAL
	L	H	L	H	L	X	X	X	ILLEGAL
	L	H	L	L	X	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	X	NOP(Maintain Power Down)
ALL BANKS IDLE	H	H	X	X	X	X	X	X	Refer to Function True Table
	H	L	H	X	X	X	X	X	Enter Power Down*3
	H	L	L	H	H	H	X	X	Enter Power Down*3
	H	L	L	H	H	L	X	X	ILLEGAL
	H	L	L	H	L	X	X	X	ILLEGAL
	H	L	L	L	H	H	L	RA	Row (& Bank) Active
	H	L	L	L	L	H	L	X	Enter Self-Refresh*3
	H	L	L	L	L	L	L	OP Code	Mode Register Access
	H	L	L	L	L	L	H	OP Code	Special Mode Register Access
	L	X	X	X	X	X	X	X	Refer to Current State=Power Down
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to Function True Table
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle*4
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle*4
	L	L	X	X	X	X	X	X	Maintain Clock Suspend

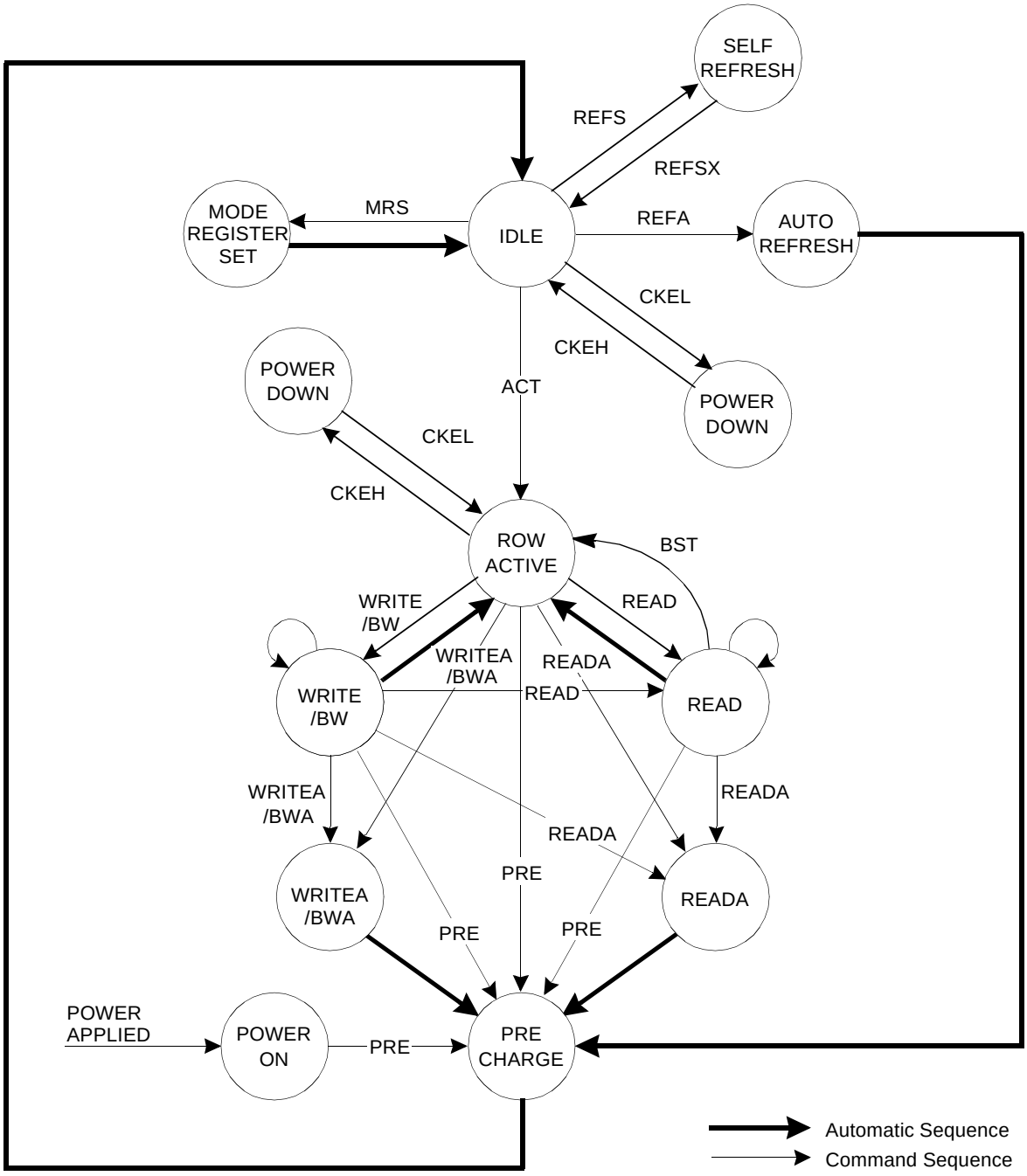
ABBREVIATIONS :

H=High Level, L=Low level, X=Don't Care

Note :

1. After CKE's low to high transition to exist self refresh mode. And a time of tRC(min) has to be elapse after CKE's low to high transition to issue a new command.
2. CKE low to high transition is asynchronous as if restarts internal clock.
   A minimum setup time "tSS + one clock" must be satisfied before any command other than exit.
3. Power-down and self refresh can be entered only from the all banks idle state.
4. Must be a legal command.

SIMPLIFIED STATE DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.6	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS(SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 65°C)

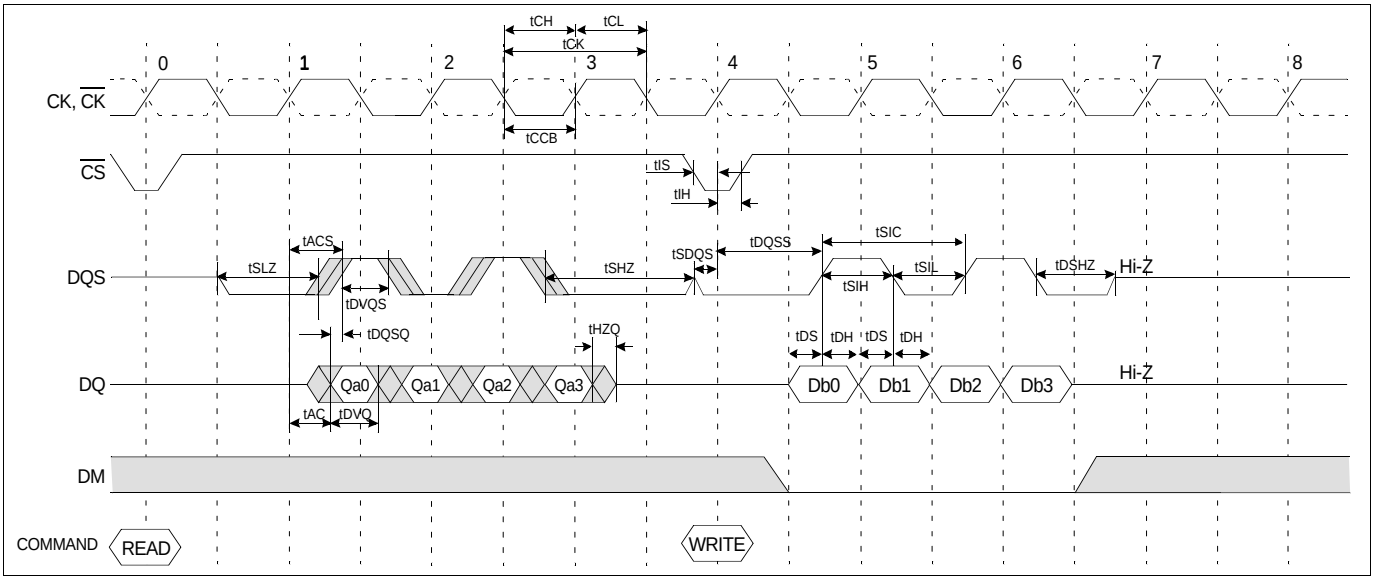
Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	V_{DD}	3.135	3.3	3.465	V	1
Output Supply voltage	V_{DDQ}	2.375	2.50	2.625	V	1
Reference voltage	V_{REF}	1.15	1.25	1.35	V	2, 3
Termination voltage	Vtt	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	4
Input logic high voltage	V_{IH}	V_{REF}+0.18	-	V_{DDQ}+0.30	V	
Input logic low voltage	V_{IL}	-0.30	-	V_{REF}-0.18	V	5
Output logic high voltage	V_{OH}	Vtt+0.76	-	-	V	I_{OH}=-15.2mA
Output logic low voltage	V_{OL}	-	-	Vtt-0.76	V	I_{OL}=+15.2mA
Input leakage current	I_{IL}	-5	-	5	uA	6
Output leakage current	I_{OL}	-5	-	5	uA	6

Note :
1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. Typically, the value of V_{REF} is expected to be about 0.50*V_{DDQ} of the transmitting device. V_{REF} is expected to track variation in V_{DDQ}.
3. Peak to peak AC noise on V_{REF} may not exceed 2% V_{REF}(DC).
4. V_{tt} of the transmitting device must track V_{REF} of the receiving device.
5. V_{IL}(min.)= -1.5V AC(pulse width ≤ 5ns).
6. For any pin under test input of 0V ≤ V_{IN} ≤ V_{DD}+0.3V is acceptable. For all other pins that are not under test V_{IN}=0V.

AC CHARACTERISTICS

Parameter		Symbol	-60		-70		-80		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CK cycle time	CL=2	tCK	12	1000	12	1000	12	1000	13	1000	ns	
	CL=3		6		7		8		10		ns	
CK high level width		tCH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK low level width		tCL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK rising edge to $\overline{CK}$ rising edge Delay		tCCB	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK Edge to Data Strobe Edge		tACS	2.5	5.5	2.5	5.5	2.5	6.0	2.5	6.0	ns	
CK Edge to Output Data Edge		tAC	2.5	5.5	2.5	5.5	2.5	6.0	2.5	6.0	ns	
Data Strobe Edge to Ouput Data Edge		tDQSQ	-0.4	+0.4	-0.5	+0.5	-0.5	+0.5	-0.6	+0.6	ns	
Data valid widow		tDVQ	1.9		2.1		2.6		3.3		ns	
Data strobe valid window		tDVQS	1.9		2.1		2.6		3.3		ns	
DQS Low-Z to 1st valid DQS(Preamble) @ Read		tSLZ	4	8	5	9	6	10	8	12	ns	
Last valid DQS to DQS Hi-Z(Postamble) @ Read		tSHZ	4	8	5	9	6	10	8	12	ns	
Last valid DQS to DQS Hi-Z(Postamble) @ Write		tDSHZ	2		2.5		3		4		ns	
Data out active to Hi-Z		tHZQ	3		3		3		3		ns	
DQS Write Preamble setup time		tSDQS	0		0		0		0		ns	
CK to valid DQS-in		tDQSS	3.5	1 tCK	4	1 tCK	4	1 tCK	4.5	1 tCK	ns	
DQS-in high level width		tSIH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-in low level width		tSIL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-in cycle time		tSIC	1		1		1		1		tCK	
Input setup time		tIS	1.5		1.75		2		2.5		ns	
Input hold time		tIH	1		1		1		1		ns	
Data in & DM set-up time		tDS	0.4		0.4		0.4		0.6		ns	
Data in & DM hold time		tDH	0.7		0.7		0.8		1		ns	
CK transition time		tT	0.5	1.5	0.5	1.7	0.5	2	0.5	2.5	ns	

Simplified Timing(1) @ BL=4, CL=2

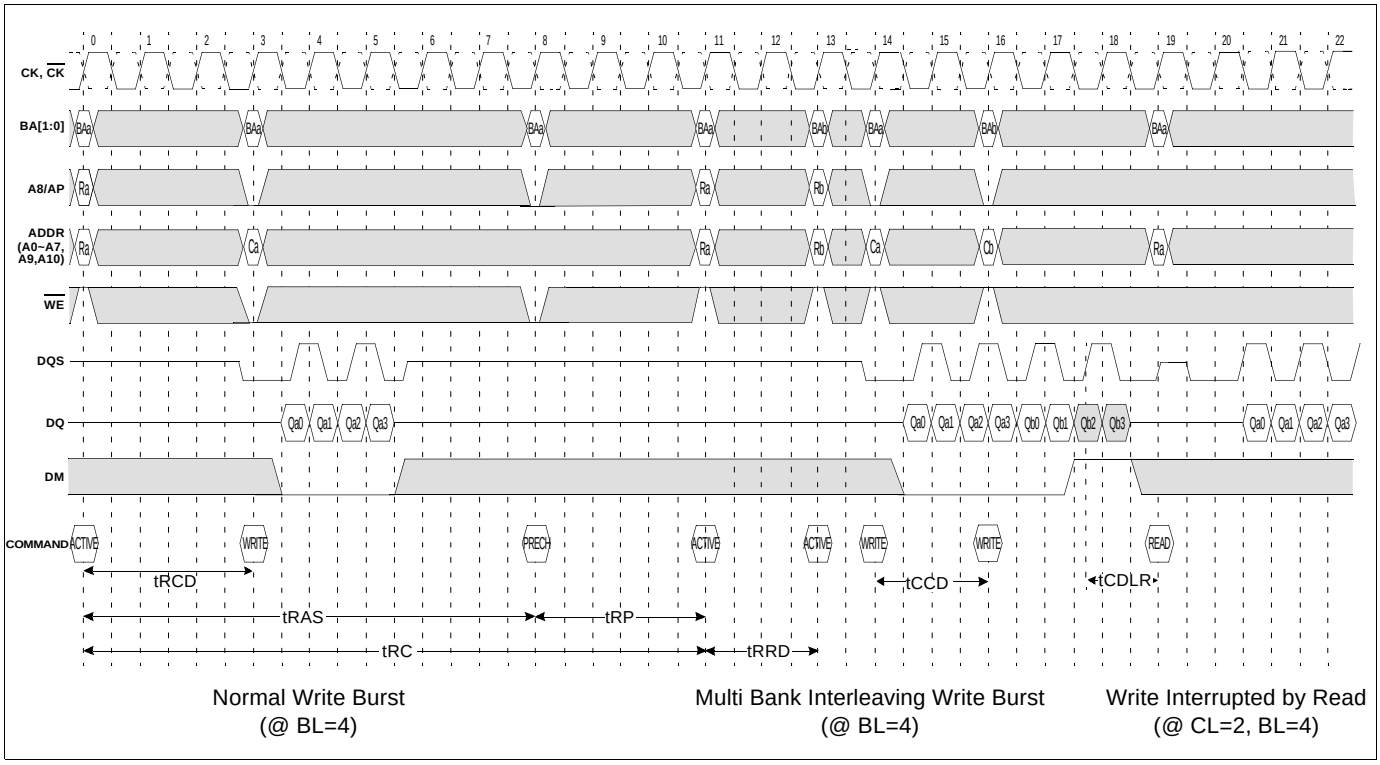


AC CHARACTERISTICS

Parameter	Symbol	-60		-70		-80		-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Row cycle time	tRC	70		70		70		70		ns	
Row active time	tRAS	48	100K	49	100K	48	100K	50	100K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	tRCD	18		20		20		20		ns	
Row precharge time	tRP	18		21		20		20		ns	
Row active to Row active delay	tRRD	12		14		16		20		ns	
Last data in to Row precharge	tRDL	3.5 tCK -tDQSS		3.5 tCK -tDQSS		3.5 tCK -tDQSS		3.5 tCK -tDQSS		ns	1
Last data in to Read command delay	tCDLR	2.5 tCK -tDQSS		2.5 tCK -tDQSS		2.5 tCK -tDQSS		2.5 tCK -tDQSS		ns	1
Last data in to Write command delay	tCDLW	0		0		0		0		tCK	
Col. address to Col. address delay	tCCD	1		1		1		1		tCK	
Mode register set cycle time	tMRD	1		1		1		1		tCK	
Special Mode register set cycle time	tSMRD	1		1		1		1		tCK	
Block write cycle	tBWC	1		1		1		1		tCK	
Block write to precharge	tBPL	4		4		4		4		tCK	

1. Note : When tDQSS is close to the minimum value, tCDLR and tRDL are 2 tck ,3 tck, respectively.
When tDQSS is close to the maximum value, tCDLR and tRDL are 1.5 tck, 2.5 tck respectively.
For normal write operation, even numbers of Din are to be written inside DRAM.

Simplified Timing(2) @ BL=4, CL=2



Normal Write Burst (@ BL=4)

Multi Bank Interleaving Write Burst (@ BL=4)

Write Interrupted by Read (@ CL=2, BL=4)

DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, T_A=0 to 65°C)

Parameter	Symbol	Test Condition	$\overline{CAS}$ Latency	Version				Unit	Note
				-60	-70	-80	-10		
Operating Current (One Bank Active)	I_{CC1}	Burst Lenth=2 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA		260	240	220	200	mA	1
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC}=10ns		2				mA	
	I_{CC2PS}	CKE ≤ V_{IL}(max), CK ≤ V_{IL}(min), t_{CC}=∞		2					
Precharge Standby Current in Non Power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC}=10ns Input signals are changed once		65				mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min),CK ≤ V_{IL}(max), t_{CC}=∞		20					
Active Standby Current power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC}=10ns		4				mA	
	I_{CC3PS}	CKE ≤ VIL(max),CK ≤ VIL(max), t_{CC}=∞		4					
Active Standby Current in in Non Power-down mode	I_{CC3N}	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), t_{CC}=10ns Input signals are changed once		65				mA	
	I_{CC3NS}	CKE ≥ VIH(min),CK ≤ VIL(max), t_{CC}=∞ Input signals are stable.		40					
Operating Current (Burst Mode)	I_{CC4}	I_{OL}=0mA Page Burst All Banks activated t_{CCD}=2 tck	3	400	360	320	280	mA	1
			2	300	300	300	280		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		300	290	280	270	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		2				mA	
Operating Current (One Bank Block Write)	I_{CC7}	$t_{CC} \geq t_{CC}$(min), I_{OL}=0mA, t_{BWC}(min)		420	380	340	300	mA	3

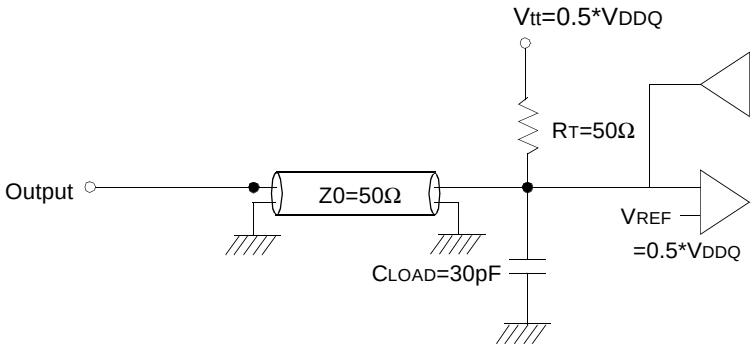
Note : 1. Measured with outputs open.

2. Refresh period is 16ms.

3. Assumes minimum column address update cycle t_{BWC}(min).

AC OPERATING TEST CONDITIONS (V_{DD}=3.3V±0.15V, T_A= 0 to 65°C)

Parameter	Value	Unit	Note
Input reference voltage for CK(for single ended)	0.50*V_{DDQ}	V	
CK signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.35/V_{REF}-0.35	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Fig.1		



(Fig. 1) Output Load Circuit

CAPACITANCE (V_{DD}=3.3V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A_0~A_{10}, BA_0~BA_1)	C_{IN1}	2.5	4.5	pF
Input capacitance (CK, CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN2}	2.5	5.0	pF
Data & DQS input/output capacitance(DQ_0~DQ_{31})	C_{OUT}	2.5	5.5	pF
Input capacitance(DM)	C_{IN3}	2.5	5.5	pF

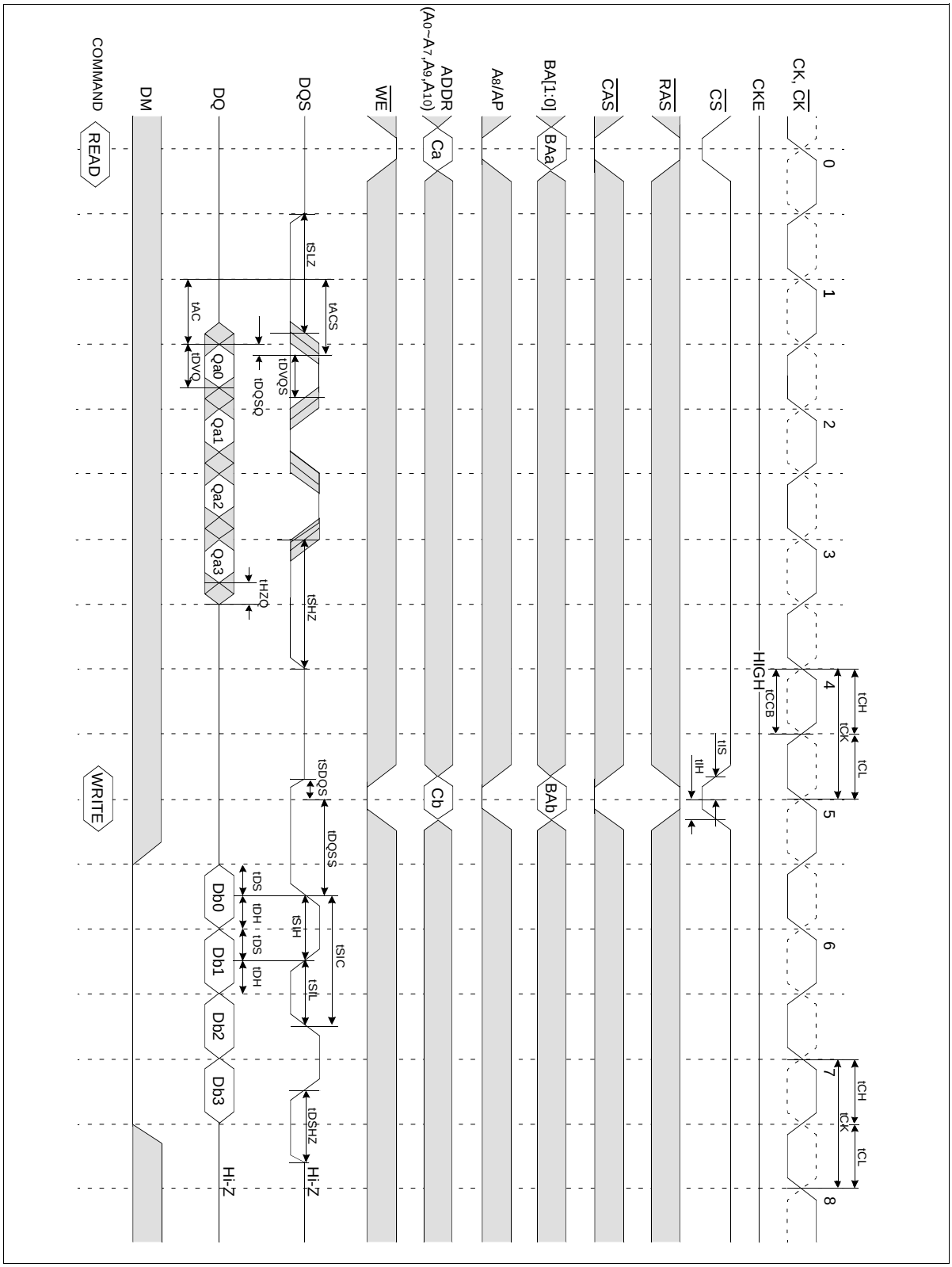
DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

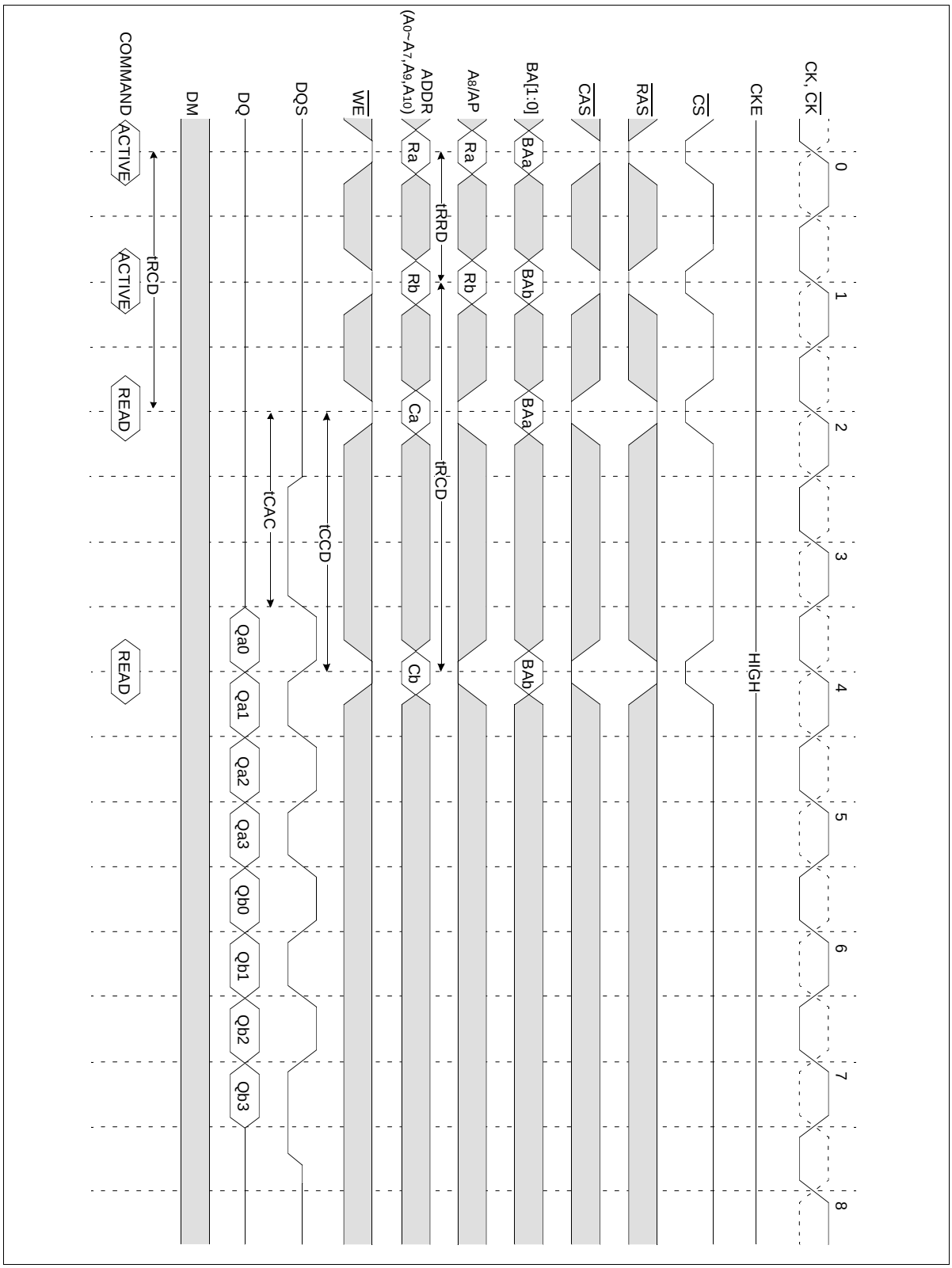
Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and V_{SS}	C_{DC1}	0.1 + 0.01	uF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1 + 0.01	uF

Note : 1. V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
2. V_{SS} and V_{SSQ} pins are separated each other
All V_{SS} pins are connected in chip. All V_{SSQ} pins are connected in chip.

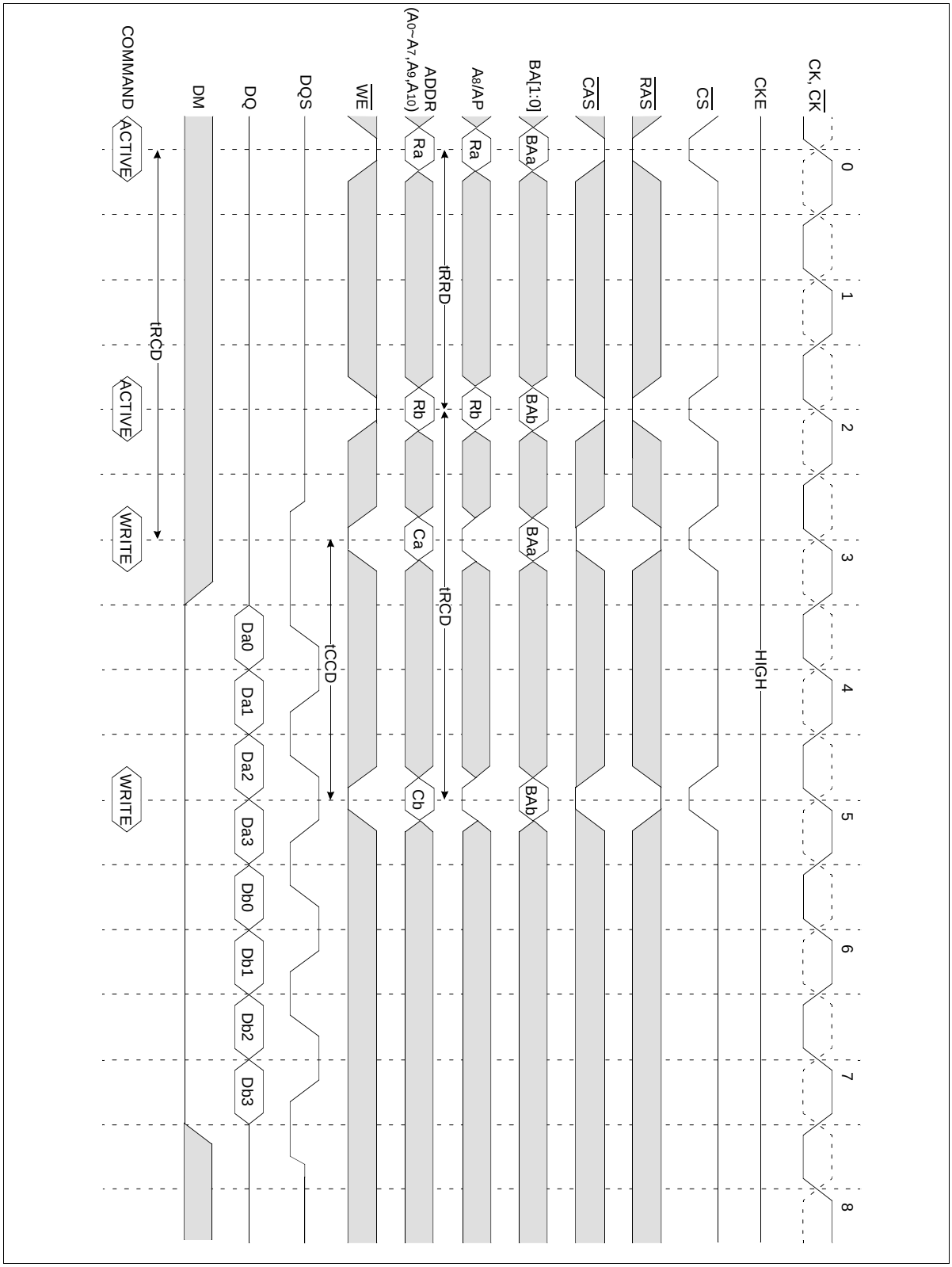
Basic Timing (Setup, Hold and Access Time @BL=4, CL=2)



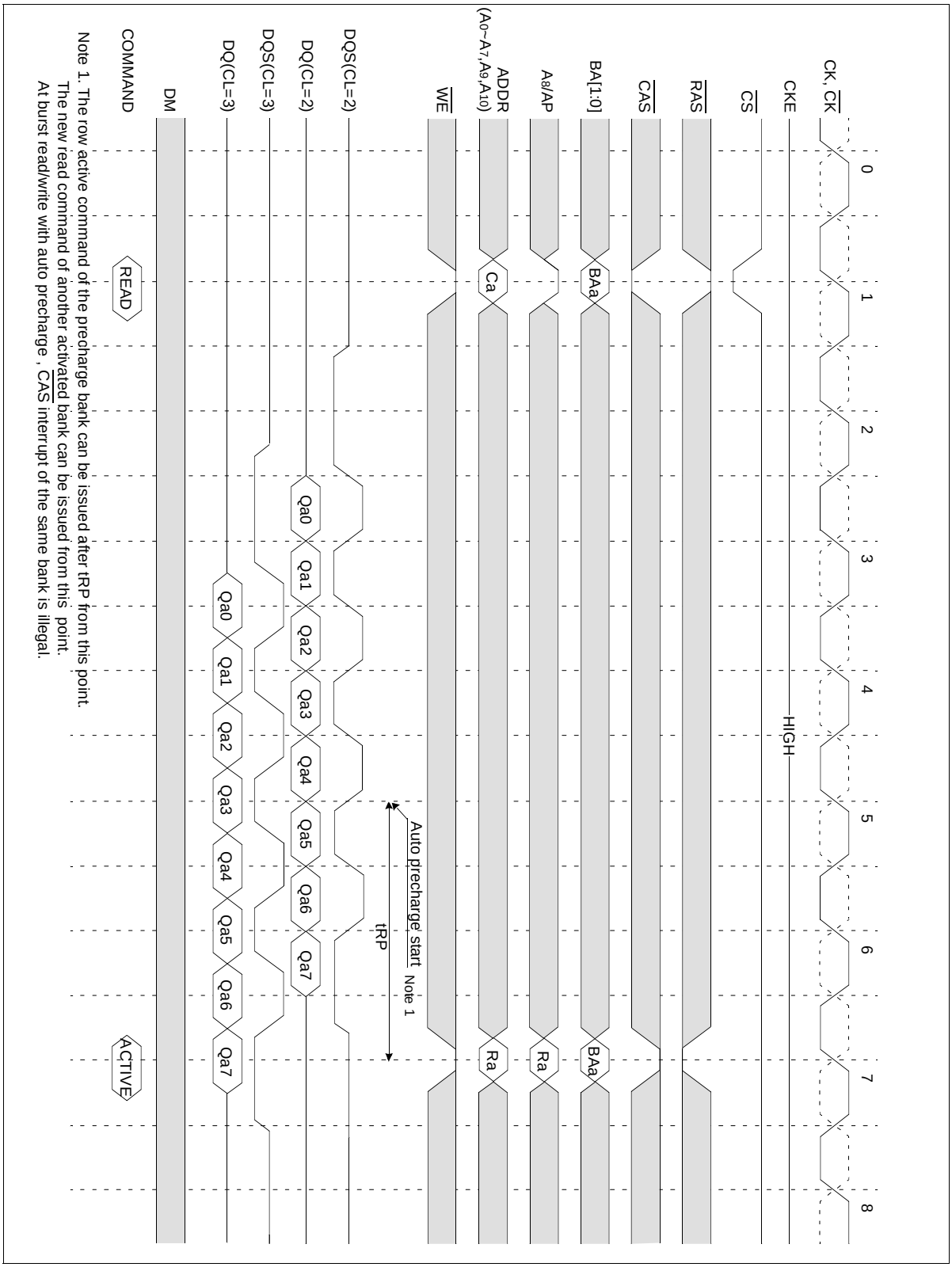
Multi Bank Interleaving READ (@BL=4, CL=2)



Multi Bank Interleaving WRITE (@BL=4)

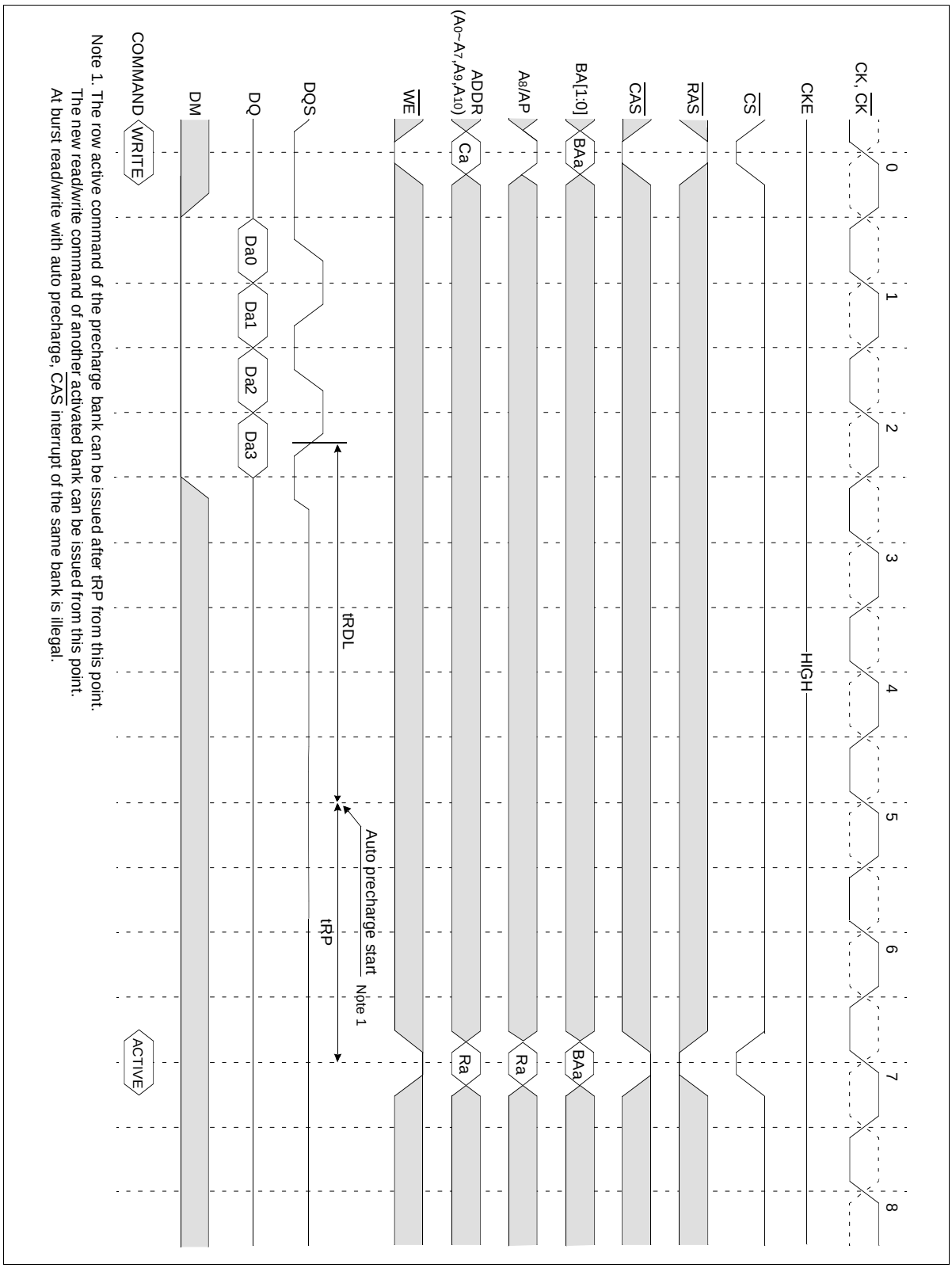


Auto Precharge after READ Burst (@BL=8)



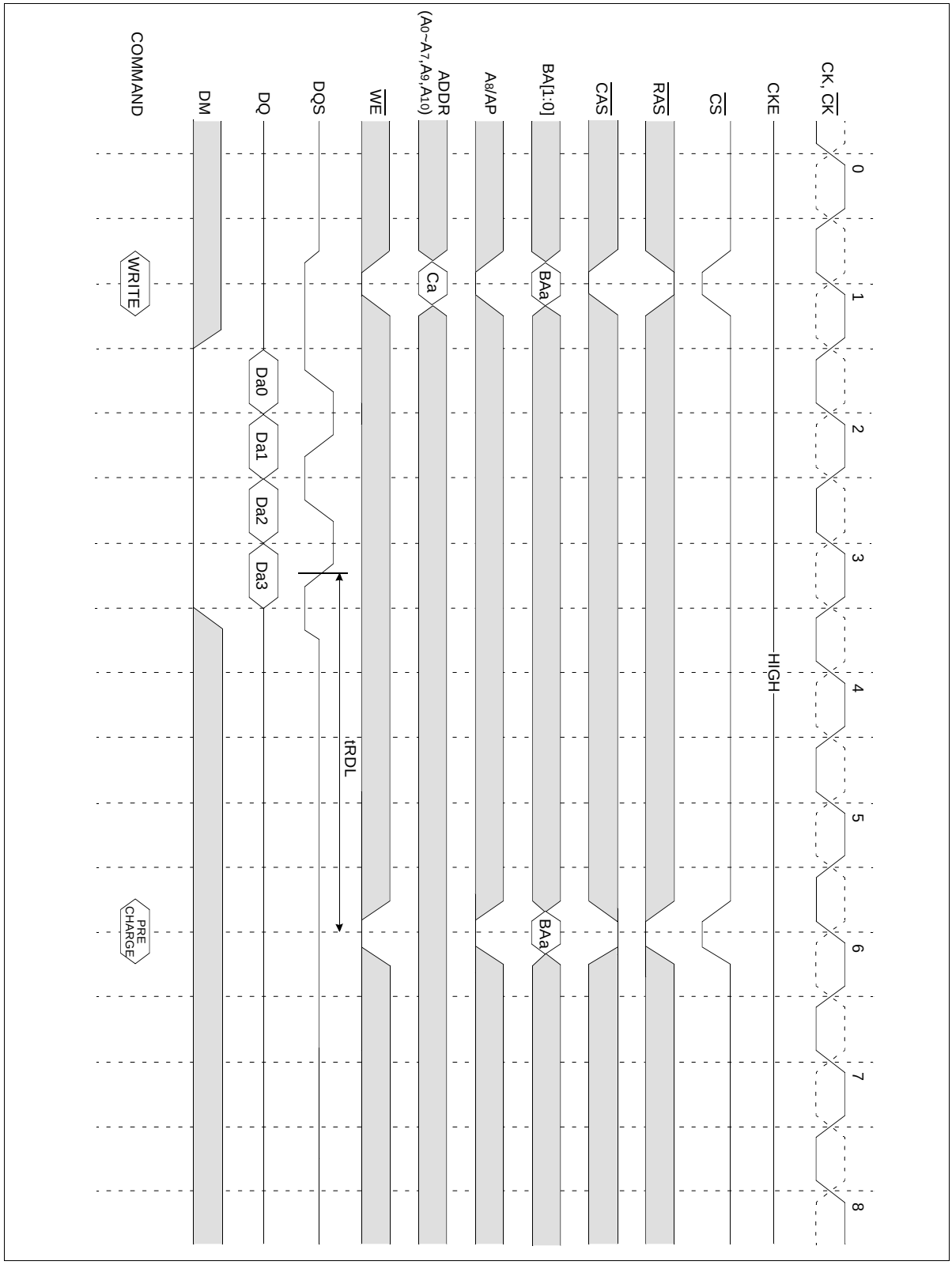
Note 1. The row active command of the precharge bank can be issued after tRP from this point.
The new read command of another activated bank can be issued from this point.
At burst read/write with auto precharge , CAS interrupt of the same bank is illegal.

Auto Precharge after WRITE Burst (@BL=4)

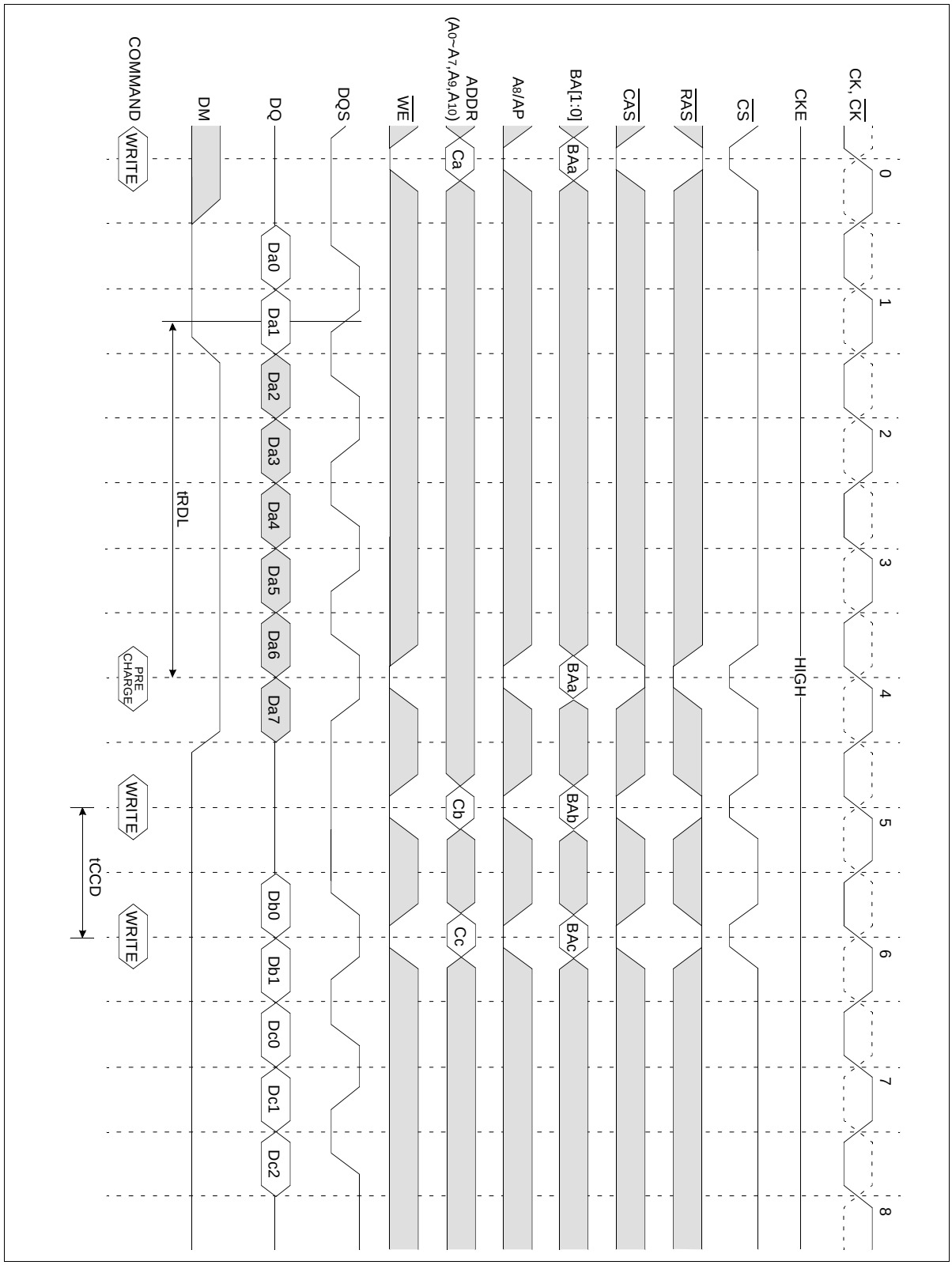


Note 1. The row active command of the precharge bank can be issued after tRP from this point.
The new read/write command of another activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same bank is illegal.

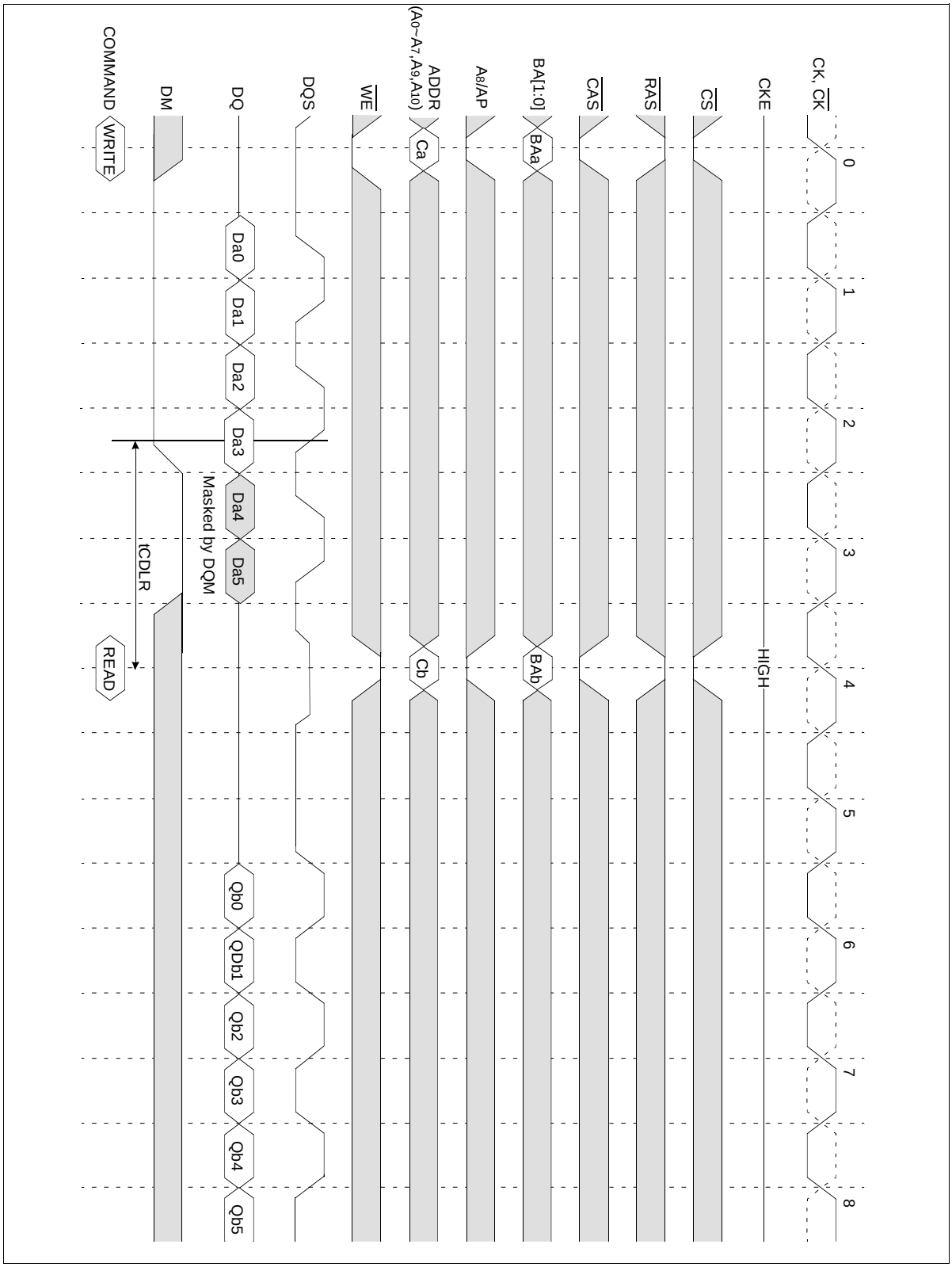
Normal WRITE Burst (@BL=4)



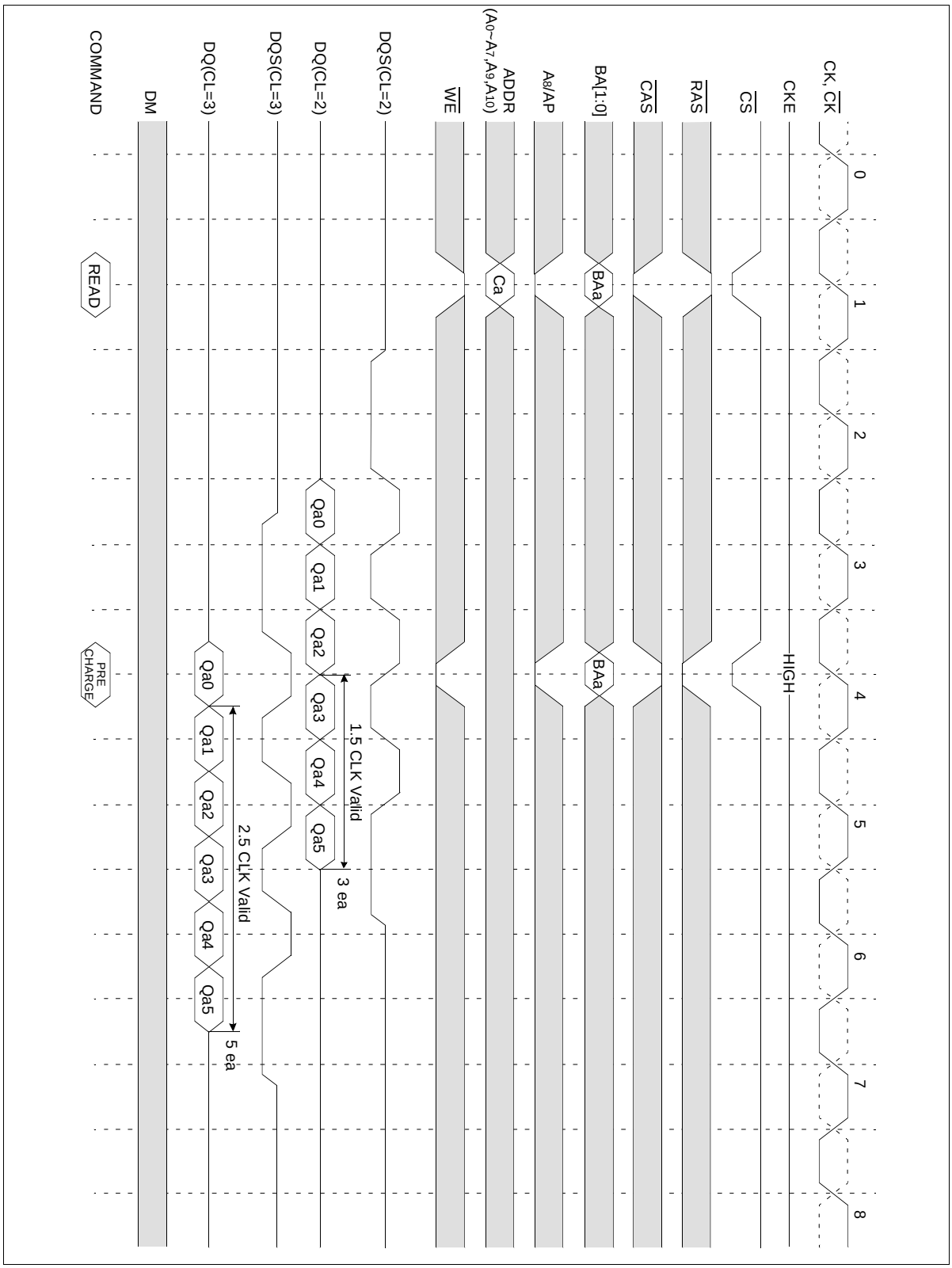
Write Interrupted by Precharge & DM (@BL=8)



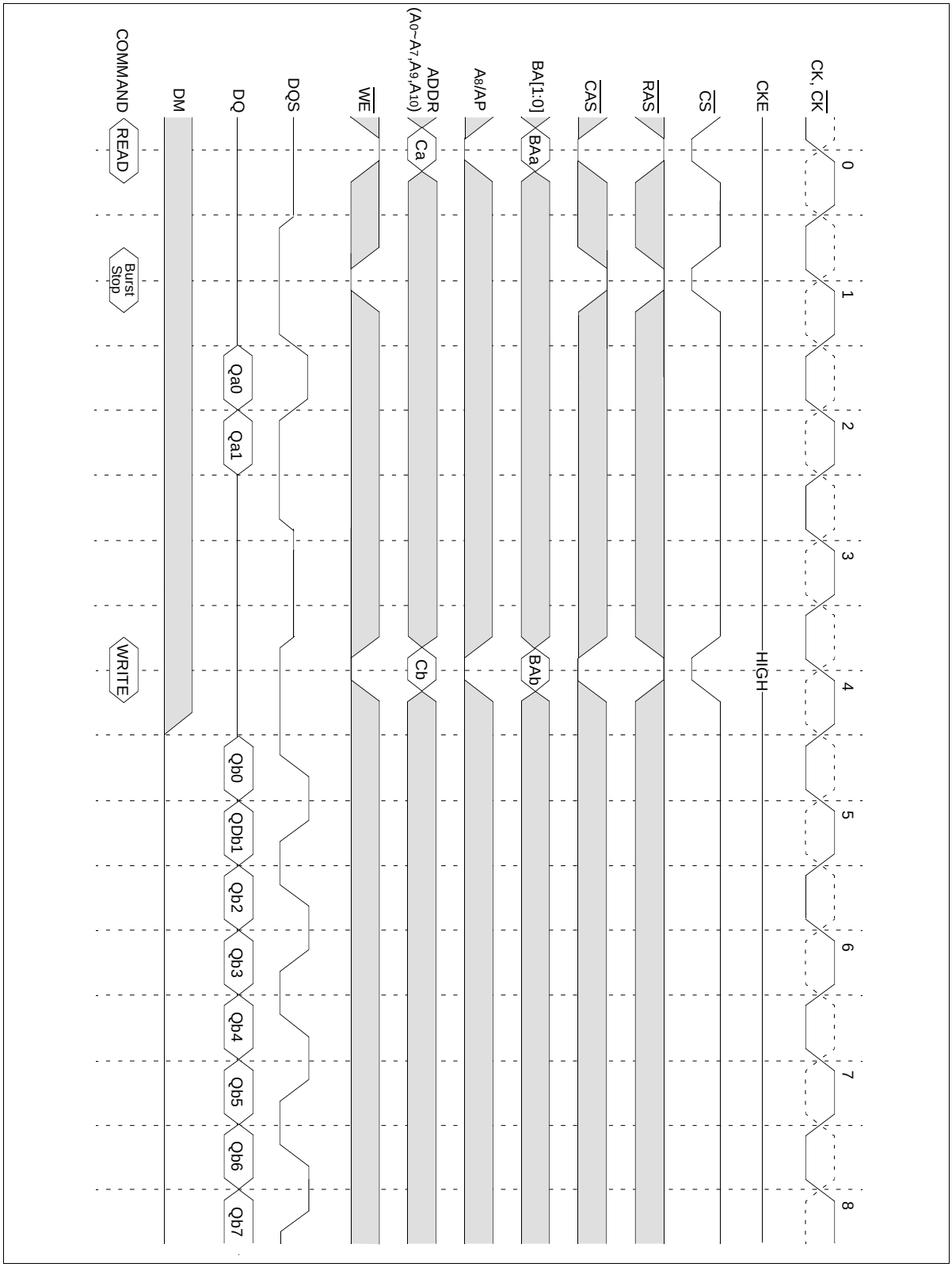
Write Interrupted by a Read (@BL=8, CL=2)



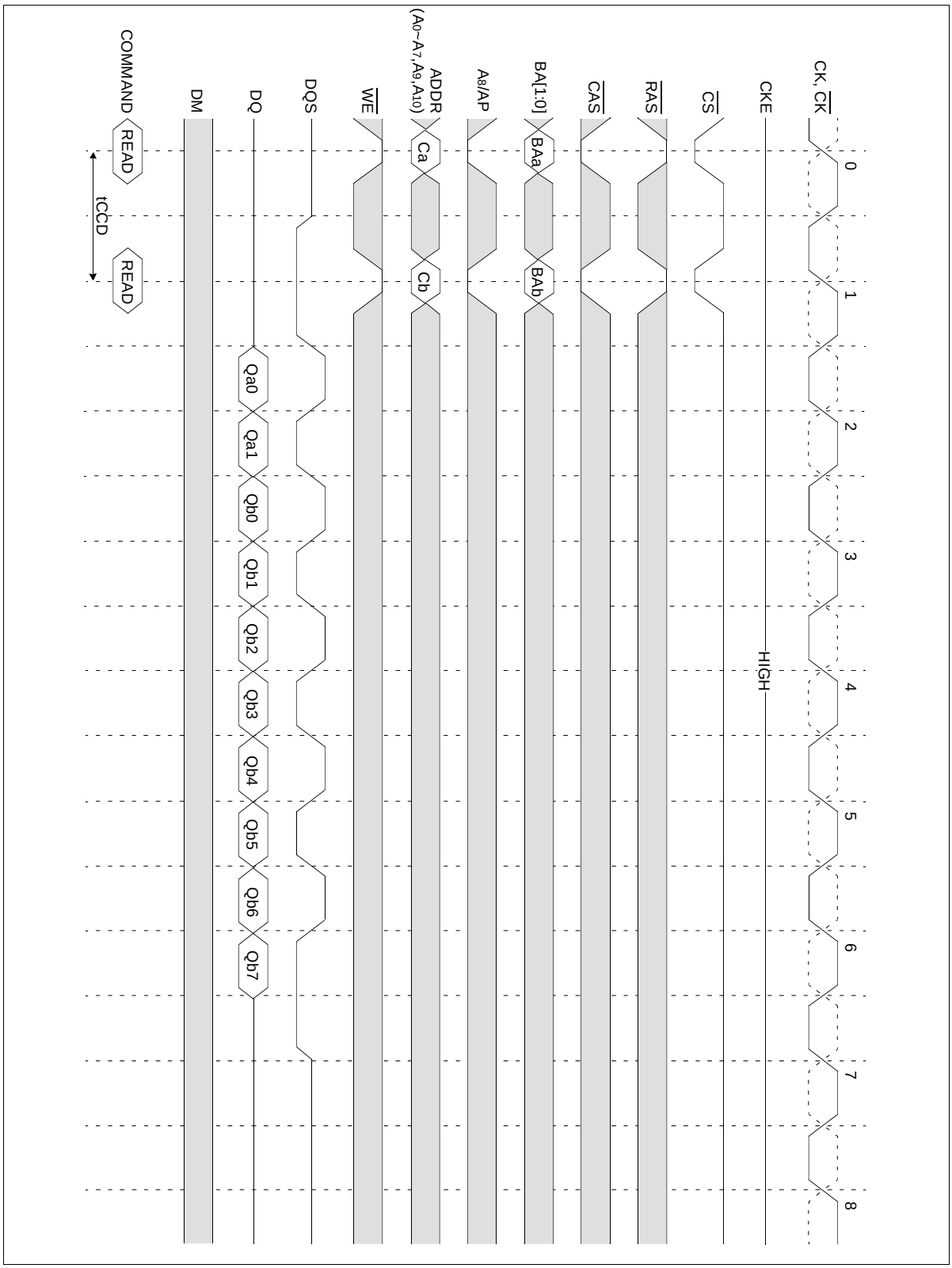
Read Interrupted by Precharge (@BL=8)



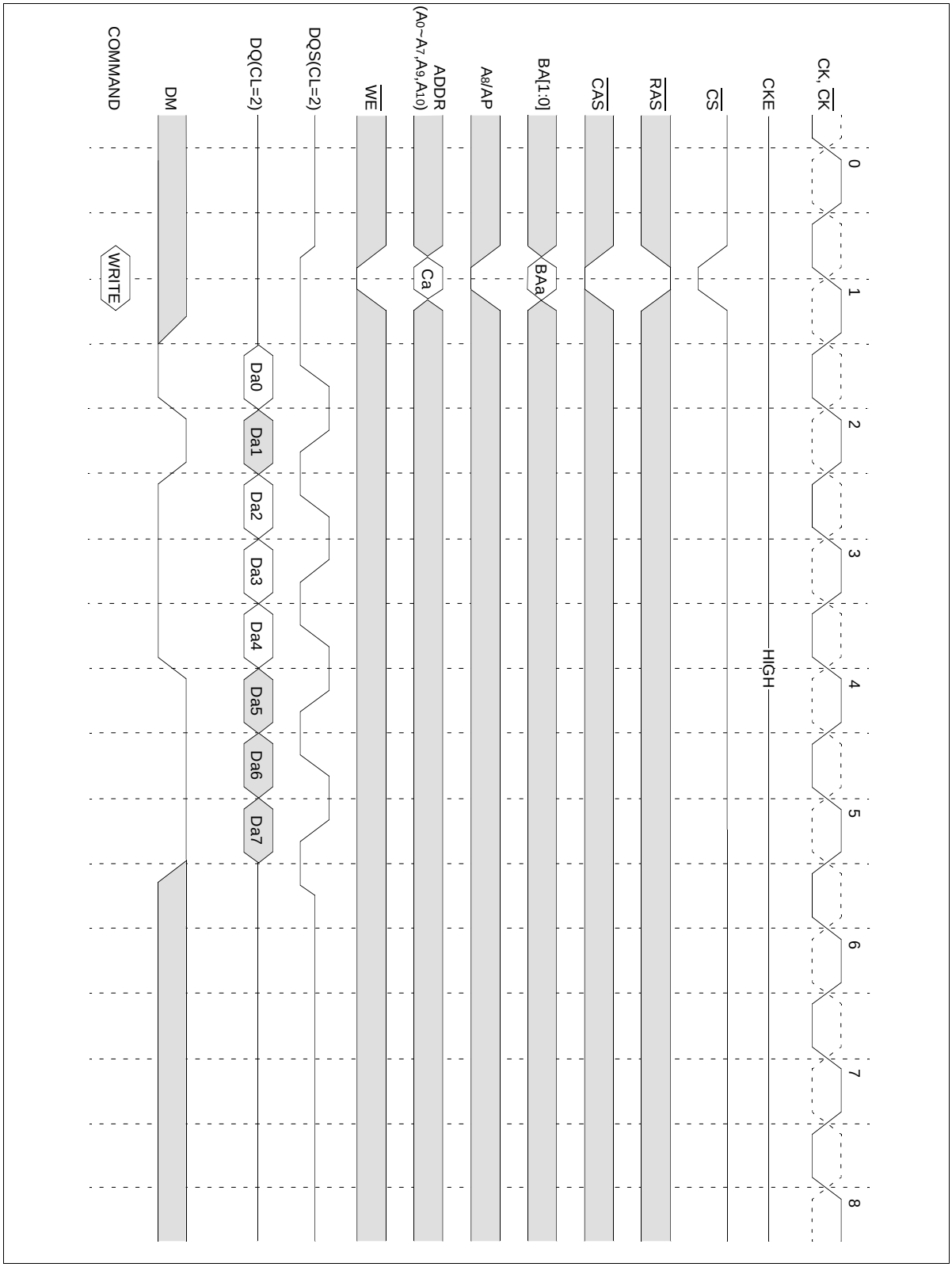
Read Interrupted by Burst stop & Write (@BL=8, CL=2)



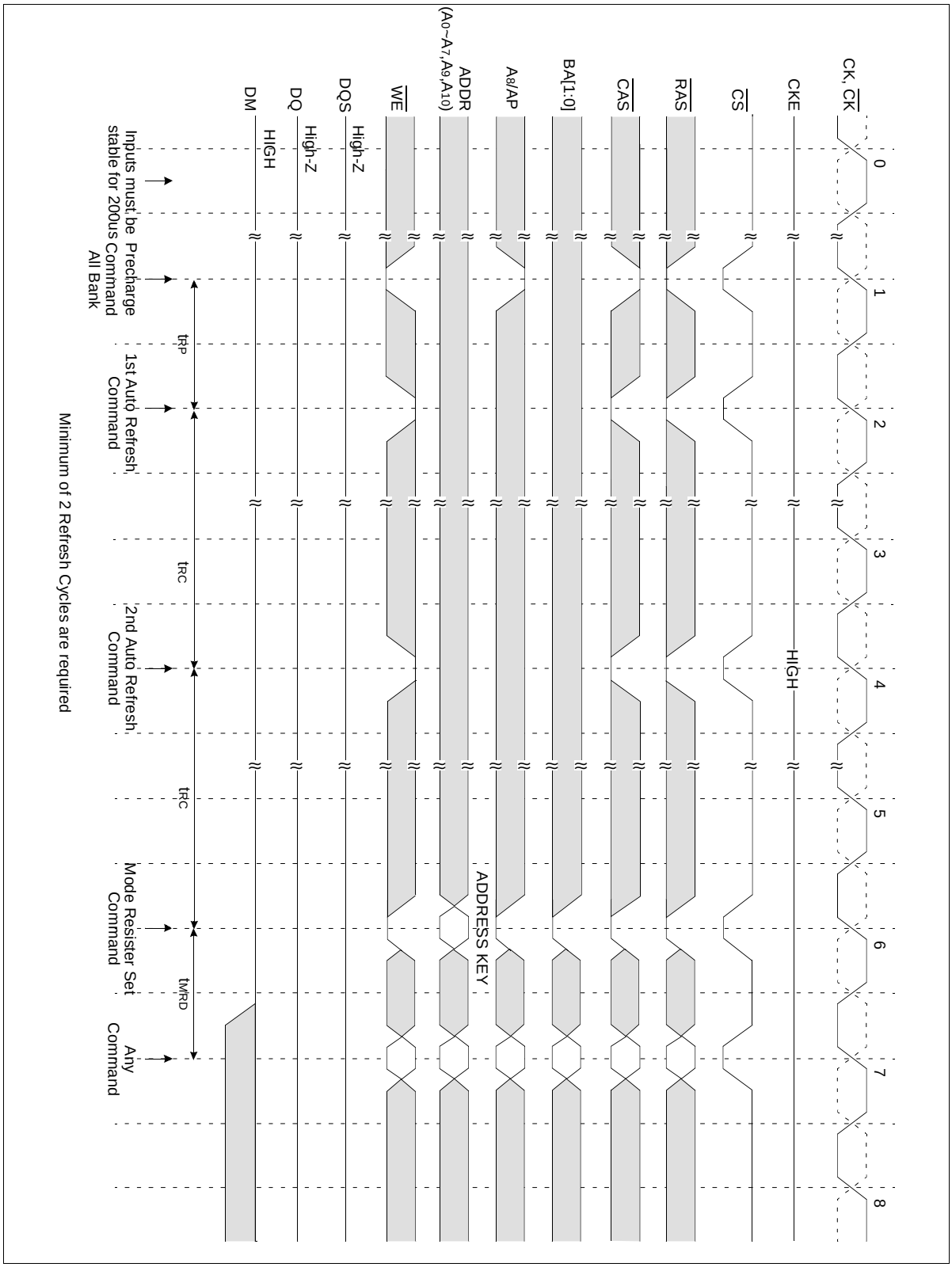
Read Interrupted by a Read (@BL=8, CL=2)



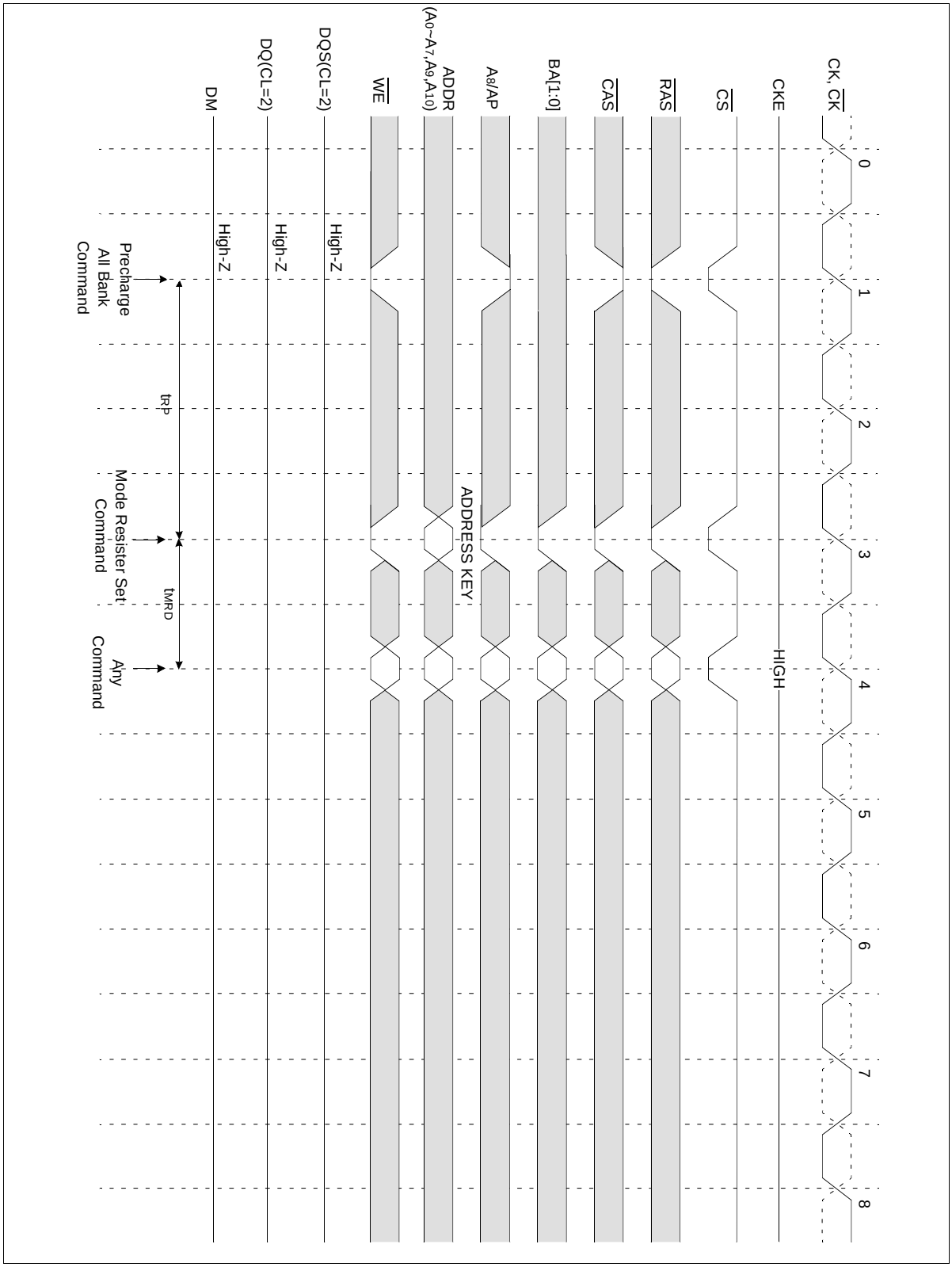
DM Function (@BL=8) only for write



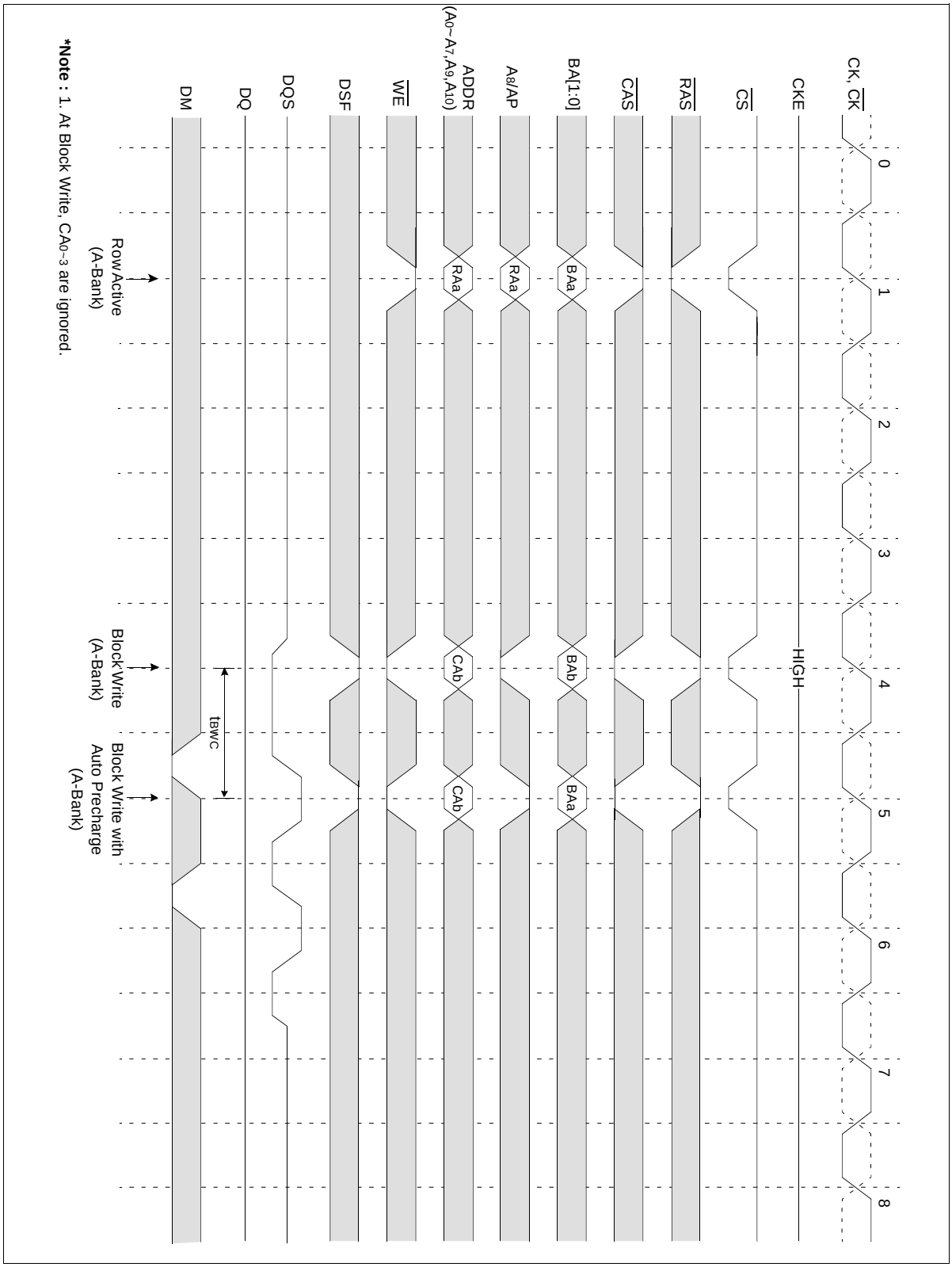
Power up Sequence & Auto Refresh(CBR)



Mode Register Set



Block Write cycle (with Auto Precharge)



***Note :** 1. At Block Write, $CA_{0\sim3}$ are ignored.

PACKAGE DIMENSIONS (TQFP)

Dimensions in Millimeters