

HIGH SPEED 2K x 8 CMOS PROM/RPROM

**FOR MAINTENANCE PURPOSES ONLY! NOT TO BE USED FOR NEW DESIGNS.
SEE WS57C191C/291C FOR NEW VERSION!**

KEY FEATURES

- **Ultra-Fast Access Time**
— 35 ns
- **Pin Compatible with Am27S191/291 and N82S191 Bipolar PROMs**
- **Low Power Consumption**
- **Immune to Latch-UP**
— Up to 200 mA
- **Fast Programming**
- **ESD Protection Exceeds 2000 V**
- **DESC SMD Nos. 5962-87650/5962-88734**

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GENERAL DESCRIPTION

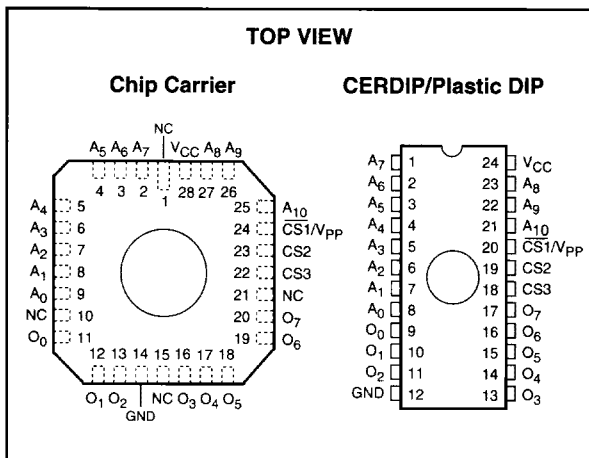
The WS57C191B/291B is an extremely High Performance 16K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts. The WS57C191B/291B is also configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

The WS57C191B is packaged in a conventional 600 mil DIP package as well as a leadless chip carrier. The WS57C291B is packaged in a space saving 300 mil DIP package configuration. Both are available in commercial, industrial, and military operating temperature ranges.

MODE SELECTION

MODE \ PINS	$\overline{CS1}/V_{PP}$	CS2	CS3	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	V_{IL}	X	V_{CC}	High Z
Program	V_{PP}	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	X	X	V_{IL}	V_{CC}	High Z

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	191B/291B-35	191B/291B-45	191B/291B-55
Address Access Time (Max)	35 ns	45 ns	55 ns
CS to Output Valid Time (Max)	20 ns	20 ns	20 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....-65° to + 150°C
 Voltage on any Pin with
 Respect to Ground-0.6V to +7V
 V_{PP} with Respect to Ground.....-0.6V to + 14V
 ESD Protection.....>2000V

***NOTICE:**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V $\pm$ 10%
Industrial	-40°C to +85°C	+5V $\pm$ 10%
Military	-55°C to +125°C	+5V $\pm$ 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)	-0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)	2.0	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	$I_{OL} = 16 \text{ mA}$		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l	30	mA
			Industrial	35	mA
			Military	35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l	40	mA
			Industrial	40	mA
			Military	40	mA
I_{LI}	Input Leakage Current	$V_{IN} = 5.5\text{V}$ or Gnd	-10	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5 \text{ V}$ or Gnd	-10	10	μA

NOTES: 1. CMOS inputs: $GND \pm 0.3\text{V}$ or $V_{CC} \pm 0.3\text{V}$.
 2. TTL inputs: $V_{IL} \leq 0.8\text{V}$, $V_{IH} \geq 2.0\text{V}$.
 3. Add 3 mA/MHz for A.C. power component.

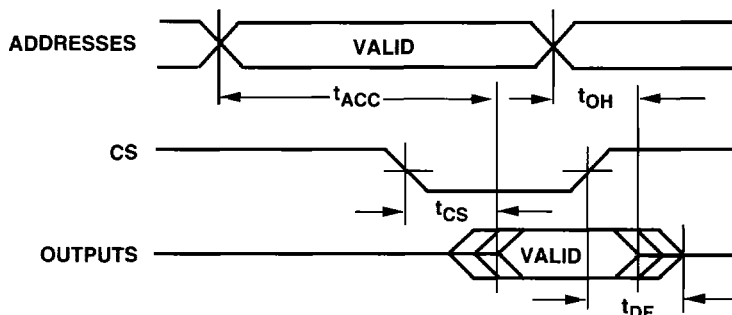
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	191B/291B-35		191B/291B-45		191B/291B-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20		20	
Output Disable to Output Float*	t_{DF}		20		20		20	
Address to Output Hold	t_{OH}	0		0		0		

* Sampled, Not 100% Tested

AC READ TIMING DIAGRAM



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CAPACITANCE⁽⁵⁾ $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$

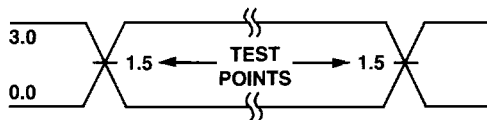
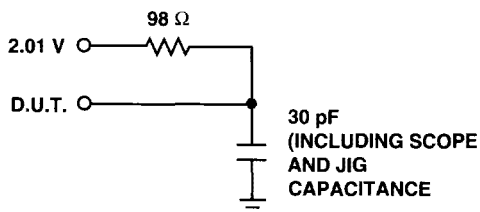
SYMBOL	PARAMETER	CONDITIONS	TYP ⁽⁶⁾	MAX	UNITS
C_{IN}	Input Capacitance	$V_{IN} = 0\text{ V}$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{ V}$	8	12	pF
C_{VPP}	V_{PP} Capacitance	$V_{PP} = 0\text{ V}$	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.

6. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

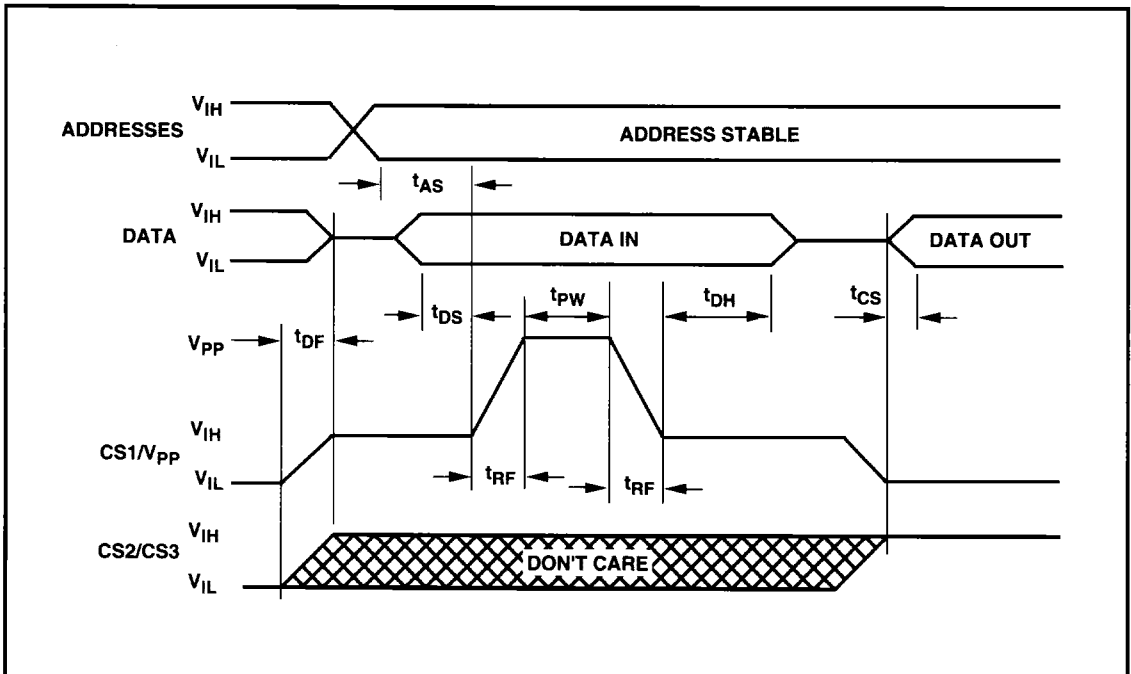
PROGRAMMING INFORMATION**DC CHARACTERISTICS** ($T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 5.6 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 13.5 \pm 0.5 \text{ V}$)

SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current ($V_{IN} = V_{CC}$ or Gnd)	-10	10	μA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		25	mA
V_{OL}	Output Low Voltage During Verify ($I_{OL} = 16 \text{ mA}$)		0.45	V
V_{OH}	Output High Voltage During Verify ($I_{OH} = -4 \text{ mA}$)	2.4		V

NOTE: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS ($T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 5.6 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 13.5 \pm 0.5 \text{ V}$)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			μs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			μs
t_{PW}	Program Pulse Width	1	3	10	ms
t_{DH}	Data Hold Time	2			μs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			μs

PROGRAMMING WAVEFORM

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191B					
WS57C191B-35D	35	24 Pin Cerdip, 0.6"	D1	Comm'l	Standard
WS57C191B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191B-35P	35	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191B-45CMB*	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C191B-45D	45	24 Pin Cerdip, 0.6"	D1	Comm'l	Standard
WS57C191B-45DI	45	24 Pin Cerdip, 0.6"	D1	Industrial	Standard
WS57C191B-45DMB*	45	24 Pin Cerdip, 0.6"	D1	Military	MIL-STD-883C
WS57C191B-45FMB*	45	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C191B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191B-45P	45	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191B-45YMB*	45	24 Pin Cerdip, 0.6"	Y3	Military	MIL-STD-883C
WS57C191B-45ZMB*	45	28 Pad CLLCC	Z2	Military	MIL-STD-883C
WS57C191B-50CMB*	50	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C191B-50DMB*	50	24 Pin Cerdip, 0.6"	D1	Military	MIL-STD-883C
WS57C191B-55D	55	24 Pin Cerdip, 0.6"	D1	Comm'l	Standard
WS57C191B-55DMB*	55	24 Pin Cerdip, 0.6"	D1	Military	MIL-STD-883C
WS57C191B-55ZMB*	55	28 Pad CLLCC	Z2	Military	MIL-STD-883C
WS57C291B					
WS57C291B-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291B-35T	35	24 Pin Cerdip, 0.3"	T1	Comm'l	Standard
WS57C291B-45KMB*	45	24 Pin Cerdip, 0.3"	K1	Military	MIL-STD-883C
WS57C291B-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291B-45T	45	24 Pin Cerdip, 0.3"	T1	Comm'l	Standard
WS57C291B-45TI	45	24 Pin Cerdip, 0.3"	T1	Industrial	Standard
WS57C291B-45TMB*	45	24 Pin Cerdip, 0.3"	T1	Military	MIL-STD-883C
WS57C291B-50TMB*	50	24 Pin Cerdip, 0.3"	T1	Military	MIL-STD-883C
WS57C291B-55KMB*	55	24 Pin Cerdip, 0.3"	K1	Military	MIL-STD-883C
WS57C291B-55T	55	24 Pin Cerdip, 0.3"	T1	Comm'l	Standard
WS57C291B-55TMB*	55	24 Pin Cerdip, 0.3"	T1	Military	MIL-STD-883C

NOTE: 9. The actual part marking will not include the initials "WS."

*SMD product. See section 5 for SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

**REFER TO
PAGE 6-1**

The WS57C191B and WS57C291B are programmed using Algorithm A shown on page 6-3.

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