DRAM

MT4C16270

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply*
- All inputs, outputs and clocks are TTL-compatible
- 512-cycle refresh in 8ms (9 row and 9 column addresses)
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- Extended Data-Out (EDO) PAGE MODE access
- BYTE WRITE and BYTE READ access cycles

OPTIONS — MARKING

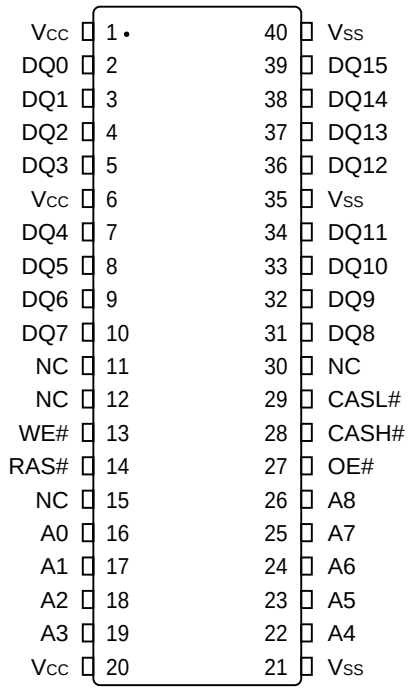
- Package
  Plastic SOJ (400 mil) — DJ
- Timing
  40ns access — -4*
  50ns access — -5*
  60ns access — -6
- Part Number Example: MT4C16270DJ-4

NOTE: 1. The "#" symbol indicates signal is active LOW.

*40ns and 50ns access specifications are limited to a V_{CC} range of ±5%.

PIN ASSIGNMENT (Top View)

40-Pin SOJ



KEY TIMING PARAMETERS

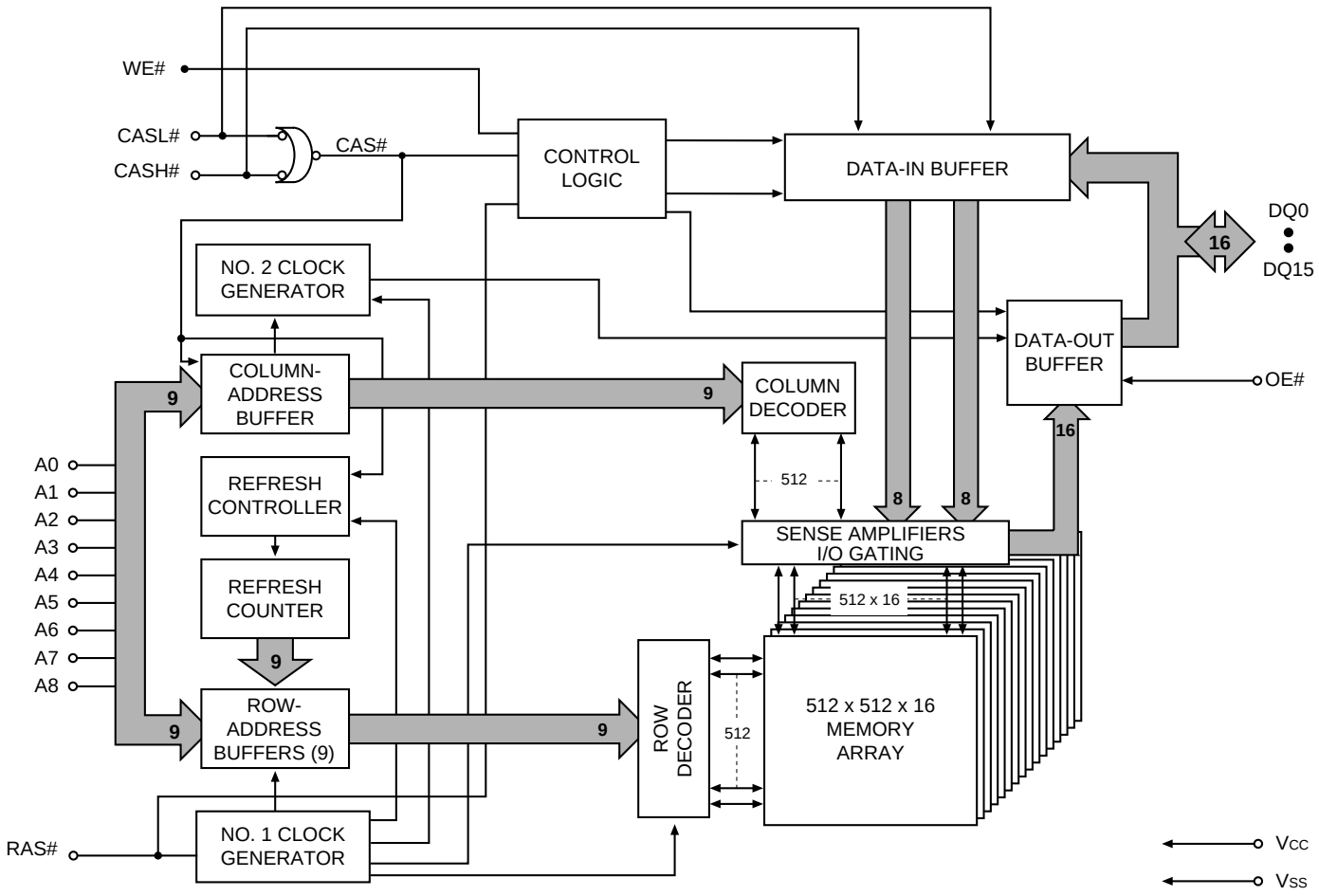
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}	t_{CP}
-4	75ns	40ns	15ns	20ns	12ns	6ns	6ns
-5	100ns	50ns	20ns	25ns	15ns	8ns	8ns
-6	110ns	60ns	25ns	30ns	15ns	10ns	10ns

GENERAL DESCRIPTION

The MT4C16270 is a randomly accessed, solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4C16270 has both BYTE WRITE and WORD WRITE access cycles via two CAS# pins.

The MT4C16270 CAS# function and timing are determined by the first CAS# (CASL# or CASH#) to transition LOW and by the last to transition back HIGH. CASL# and CASH# function like CAS# in that either CASL# or CASH# will generate an internal CAS#. Using only one of the two signals results in a BYTE WRITE cycle. CASL# transitioning LOW selects a WRITE cycle for the lower byte (DQ0-DQ7), and CASH# transitioning LOW selects a WRITE cycle for the upper byte (DQ8-DQ15). BYTE READ cycles are achieved through CASL# or CASH# in the same manner.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered nine bits (A0-A8) at a time. RAS# is used to latch the first nine bits and CAS#, the latter nine bits.

The CAS# control also determines whether the cycle will be a refresh cycle (RAS#-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS# goes LOW. The MT4C16270 has two CAS# controls: CASL# and CASH#.

The CASL# and CASH# inputs internally generate a CAS# signal that functions like the single CAS# input on other 256K x 16 DRAMs. The key difference is that each CAS# controls its corresponding DQ tristate logic (in conjunction with OE#, WE# and RAS#). CASL# controls DQ0-DQ7 and CASH# controls DQ8-DQ15.

The MT4C16270 CAS# function is determined by the first CAS# (CASL# or CASH#) transitioning LOW and the last transitioning back HIGH. The two CAS# controls give the MT4C16270 both BYTE READ and BYTE WRITE cycle capabilities. (See Figures 1 and 2.)

A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS# (CASL# or CASH#), whichever occurs last. An EARLY WRITE occurs when WE is taken LOW prior to either CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE falls after CAS# (CASL# or CASH#) is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE#. During

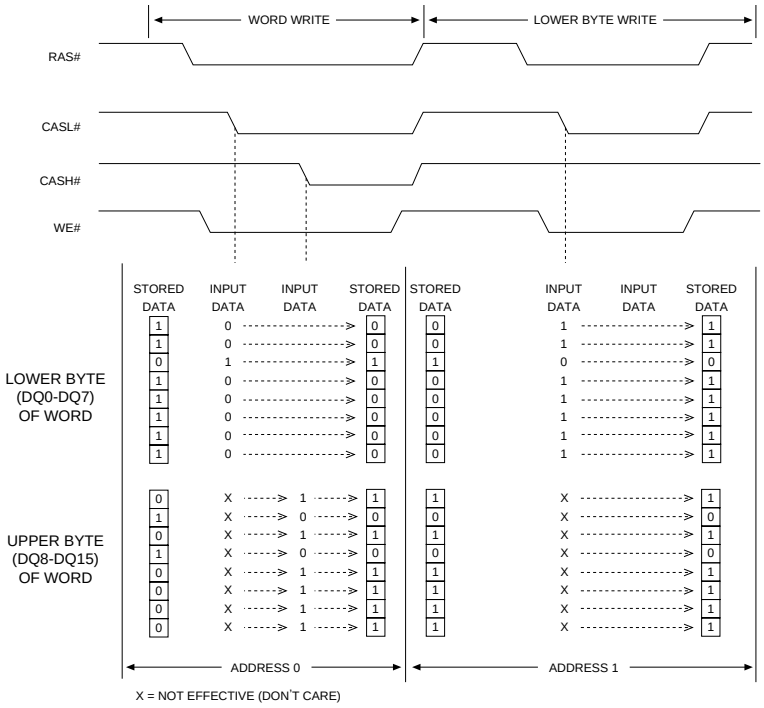


Figure 1
WORD AND BYTE WRITE EXAMPLE

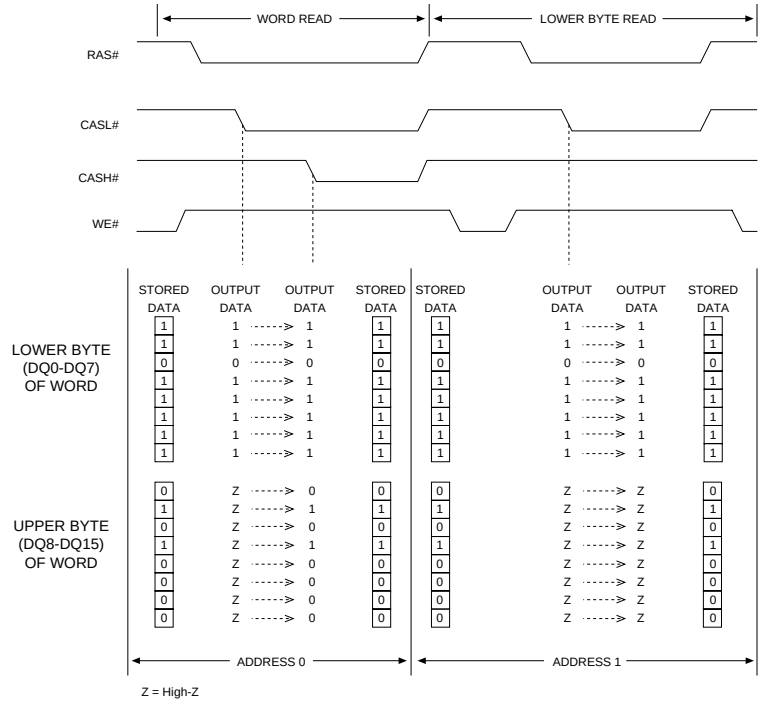


Figure 2
WORD AND BYTE READ EXAMPLE

FUNCTIONAL DESCRIPTION (continued)

LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data outputs will drive read data from the accessed location.

Additionally, both bytes must always be of the same mode of operation if both bytes are active. A CAS# precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte are not allowed during the same cycle. However, an EARLY WRITE on one byte and a LATE WRITE on the other byte, after a CAS# precharge has been satisfied, are permissible.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE#, WE# and RAS#.

EDO-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The EDO-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the EDO-PAGE-MODE operation.

BYTE ACCESS CYCLE

The BYTE WRITE cycle is determined by the use of CASL# and CASH#. Enabling CASL# selects a lower BYTE WRITE cycle (DQ0-DQ7), while enabling CASH# selects an upper BYTE WRITE cycle (DQ8-DQ15). Enabling both CASL# and CASH# selects a WORD WRITE cycle.

The MT4C16270 can be viewed as two 256K x 8 DRAMs that have common input controls. Figure 1 illustrates the BYTE WRITE and WORD WRITE cycles. The BYTE READ is accomplished in the same manner (see Figure 2).

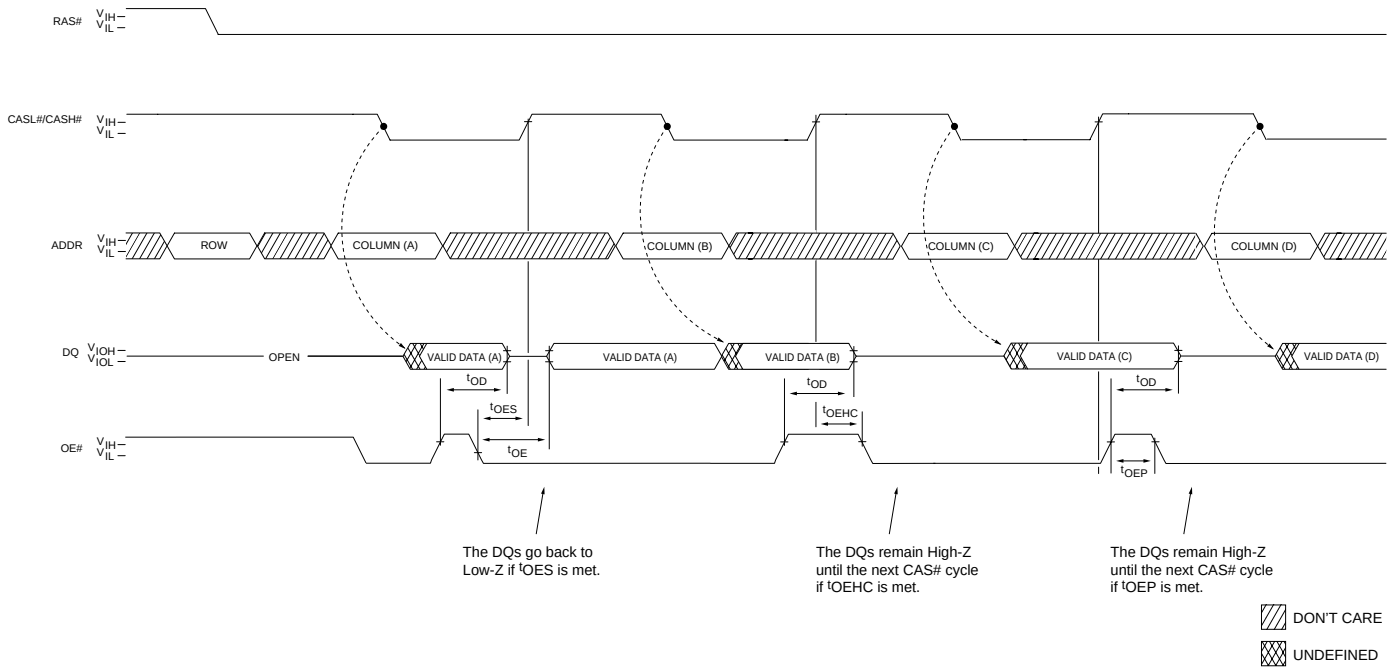


Figure 3
OE# CONTROL OF DQs

EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. If CAS# goes HIGH, and OE# is LOW (active), the output buffers will be disabled. The MT4C16270 offers an accelerated page mode cycle by eliminating output disable from CAS# HIGH. This option is called EDO, and it allows CAS# precharge time (^{t}CP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms).

EDO operates like any DRAM READ or FAST-PAGE-MODE READ, except data is held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH. OE# can be brought LOW or HIGH while CAS# and RAS# are LOW, and the DQs will transition between valid data and High-Z. Using OE#, there are two methods to disable the outputs and keep them disabled during the CAS# HIGH time. The first method is to have OE# HIGH when CAS# transitions HIGH and keep OE# HIGH for ^{t}OEHC. This will tristate the DQs and they will remain tristate, regardless of OE#, until CAS# falls again. The second method is to have OE# LOW when CAS# transitions HIGH. Then OE# can pulse HIGH for a minimum of ^{t}OEP anytime during the CAS# HIGH period and the DQs will tristate and remain tristate, regardless of OE#, until CAS# falls again. (Please refer to Figure 3 for further detail on the toggling OE# condition.) During other cycles, the outputs are disabled at ^{t}OFF time after RAS# and CAS# are HIGH or at ^{t}WHZ after WE# transitions LOW. The ^{t}OFF time is referenced from the rising edge of RAS# or CAS#, whichever occurs last. WE# can also perform the function of turning off the output drivers under certain conditions, as shown in Figure 4.

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all 512 combinations of RAS# addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

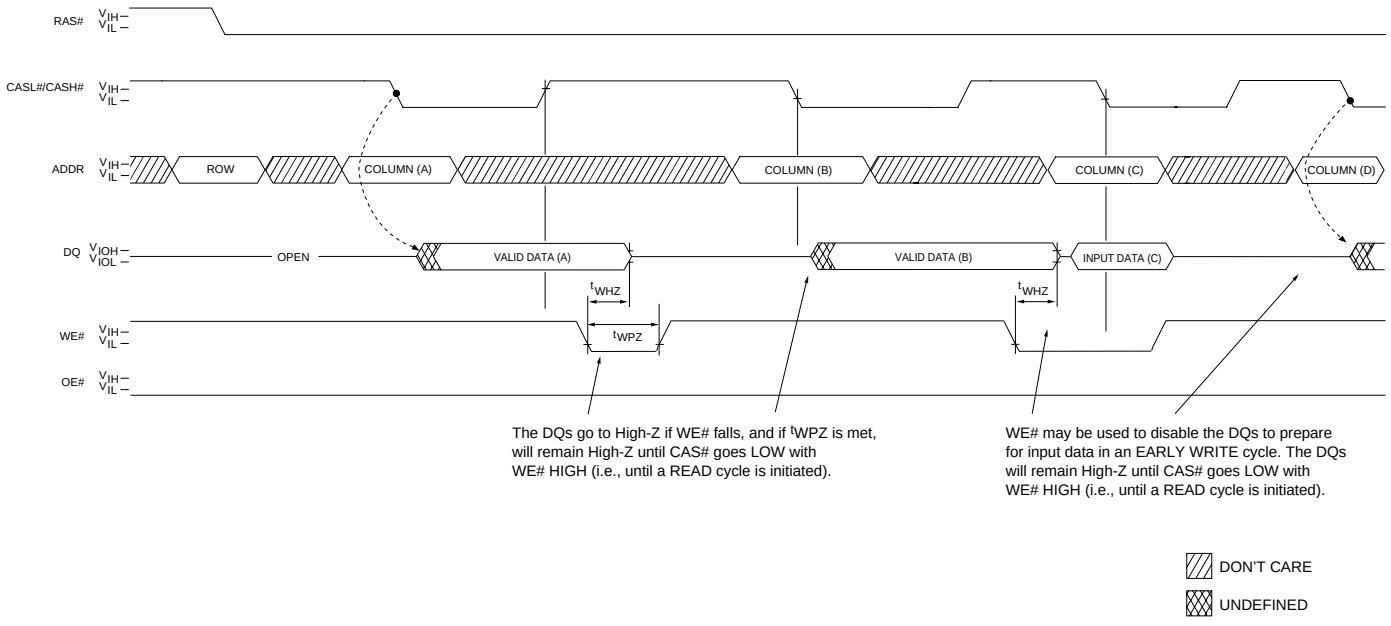


Figure 4
WE# CONTROL OF DQs

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.2W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)**

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{CC}**	4.5	5.5	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs	V_{IH}	2.4	V_{CC} + 1	V	
INPUT LOW VOLTAGE: Valid Logic 0; All inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{CC} + 1; All other pins not under test = 0V	I_I	-2	2	µA	3
OUTPUT HIGH VOLTAGE: I_{OUT} = -2.5mA	V_{OH}	2.4	–	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 2.1mA	V_{OL}	–	0.4	V	
OUTPUT LEAKAGE CURRENT: DQ is disabled; 0V ≤ V_{OUT} ≤ V_{CC}	I_{OZ}	-10	10	µA	

**40 and 50ns specifications are limited to a V_{CC} range of ±5%.

Icc OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)**

		MAX				
PARAMETER/CONDITIONS	**SYMBOL**	**-4**	**-5**	**-6**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# = V_{CC} - 0.2V)	I_{CC2}	1	1	1	mA	23
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC3}	205	195	185	mA	4, 38
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN]; ^{t}CP, ^{t}ASC = 10ns)	I_{CC4}	125	120	115	mA	4, 38
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^{t}RC = ^{t}RC [MIN])	I_{CC5}	205	195	185	mA	4
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC6}	180	170	160	mA	4, 5

**40 and 50ns specifications are limited to a V_{CC} range of ±5%.

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: RAS#, CASL#, CASH#, WE#, OE#	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

AC ELECTRICAL CHARACTERISTICS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)*

AC CHARACTERISTICS		-4		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		20		25		30	ns	
Column-address setup to CAS# precharge during WRITE	^tACH	15		15		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	30		40		40		ns	
Column-address setup time	^tASC	0		0		0		ns	27
Row-address setup time	^tASR	0		0		0		ns	
Column address to WE# delay time	^tAWD	37		48		55		ns	19
Access time from CAS#	^tCAC		12		15		15	ns	29
Column-address hold time	^tCAH	7		8		10		ns	27
CAS# pulse width	^tCAS	6	10,000	8	10,000	10	10,000	ns	35
CAS# hold time (CBR Refresh)	^tCHR	10		10		10		ns	5, 28
Last CAS# going LOW to first CAS# returning HIGH	^tCLCH	10		10		10		ns	30
CAS# to output in Low-Z	^tCLZ	3		3		3		ns	29, 39
Data output hold after CAS# LOW	^tCOH	3		3		3		ns	
CAS# precharge time	^tCP	6		8		10		ns	14, 32
Access time from CAS# precharge	^tCPA		25		28		35	ns	29
CAS# to RAS# precharge time	^tCRP	5		5		5		ns	28
CAS# hold time	^tCSH	37		40		45		ns	28
CAS# setup time (CBR Refresh)	^tCSR	10		10		10		ns	5, 27
CAS# to WE# delay time	^tCWD	30		35		40		ns	19, 27
WRITE command to CAS# lead time	^tCWL	7		8		10		ns	24, 28
Data-in hold time	^tDH	7		8		10		ns	20, 29
Data-in setup time	^tDS	0		0		0		ns	20, 29
Output disable time	^tOD	3	8	3	10	3	15	ns	26, 37, 39
Output enable time	^tOE		12		15		15	ns	21
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	6		10		15		ns	25
OE# HIGH hold time from CAS# HIGH	^tOEHC	10		10		10		ns	
OE# HIGH pulse width	^tOEP	10		10		10		ns	
OE# LOW to CAS# HIGH setup time	^tOES	5		5		5		ns	
Output buffer turn-off delay from CAS# or RAS#	^tOFF	3	15	3	15	3	15	ns	19, 26, 29, 39

*40ns and 50ns specifications are limited to a V_{CC} range of ±5%.

AC ELECTRICAL CHARACTERISTICS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)*

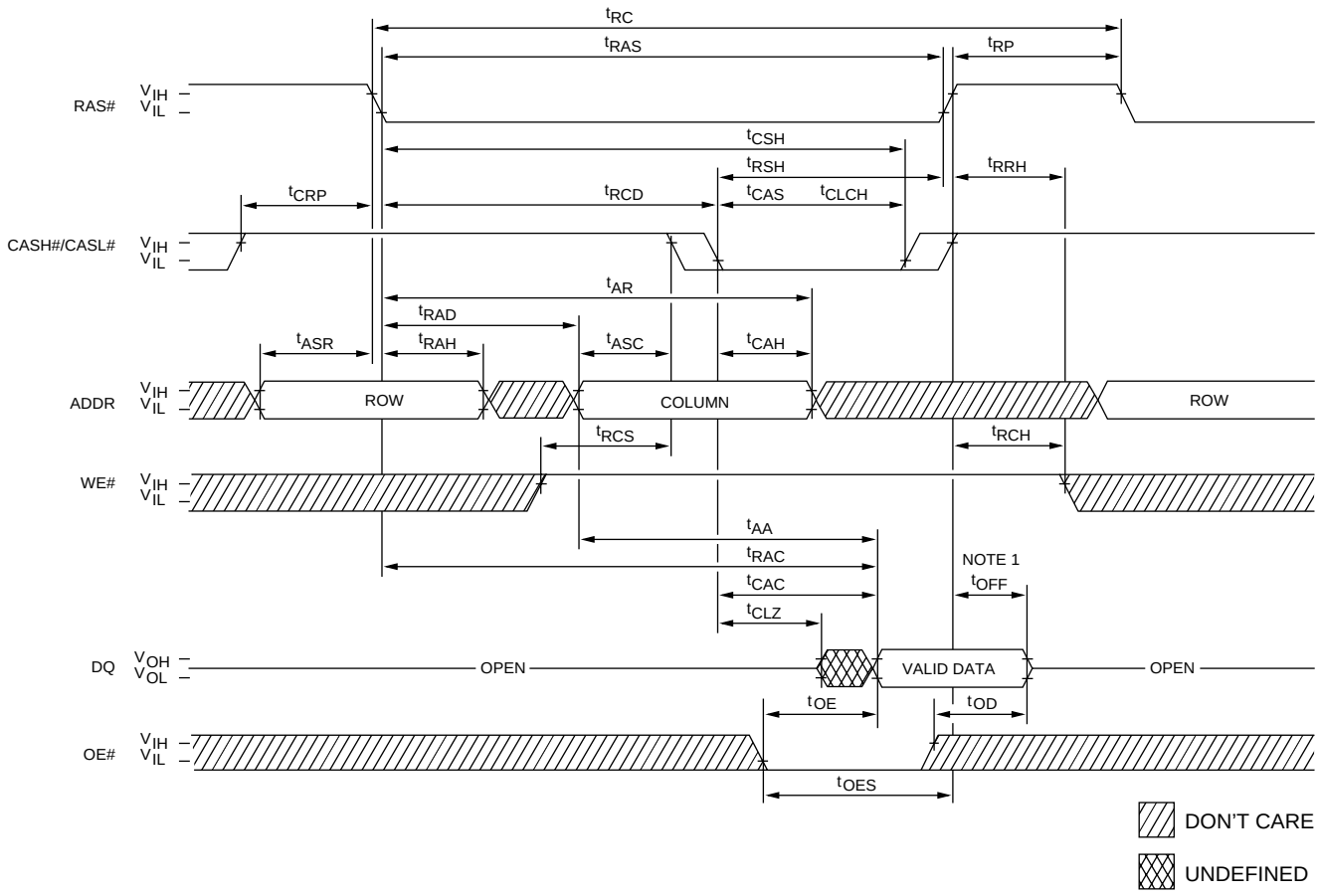
AC CHARACTERISTICS		-4		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	15		20		25		ns	31
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	60		65		72		ns	31
Access time from RAS#	^{t}RAC		40		50		60	ns	
RAS# to column-address delay time	^{t}RAD	7		13		15		ns	16
Row address hold time	^{t}RAH	7		10		10		ns	
RAS# pulse width	^{t}RAS	40	10,000	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	^{t}RASP	40	100,000	50	100,000	60	100,000	ns	
Random READ or WRITE cycle time	^{t}RC	75		100		110		ns	
RAS# to CAS# delay time	^{t}RCD	17		18		20		ns	15, 27
READ command hold time (referenced to CAS#)	^{t}RCH	0		0		0		ns	17, 24, 28
READ command setup time	^{t}RCS	0		0		0		ns	24, 27
Refresh period (512 cycles)	^{t}REF		8		8		8	ms	
RAS# precharge time	^{t}RP	25		30		35		ns	
RAS# to CAS# precharge time	^{t}RPC	10		10		10		ns	
READ command hold time (referenced to RAS#)	^{t}RRH	0		0		0		ns	17
RAS# hold time	^{t}RSH	7		8		10		ns	36
READ-WRITE cycle time	^{t}RWC	105		126		140		ns	
RAS# to WE# delay time	^{t}RWD	60		69		85		ns	19
WRITE command to RAS# lead time	^{t}RWL	7		8		10		ns	24
Transition time (rise or fall)	^{t}T	2	50	2	50	2	50	ns	9, 10
WRITE command hold time	^{t}WCH	7		8		10		ns	24, 36
WRITE command hold time (referenced to RAS#)	^{t}WCR	30		40		40		ns	24
WRITE command setup time	^{t}WCS	0		0		0		ns	19, 24, 27
Output disable delay from WE#	^{t}WHZ	3	13	3	13	3	15	ns	
WRITE command pulse width	^{t}WP	7		8		10		ns	24
WE# pulse widths to disable outputs	^{t}WPZ	10		10		10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	10		10		10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	10		10		10		ns	

*40ns and 50ns specifications are limited to a V_{CC} range of ±5%.

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V; f = 1 MHz; T_A = 25°C.
3. NC pins are assumed to be left floating and are not tested for leakage.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
7. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated anytime the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 2ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If CAS# and RAS# = V_{IH}, data output is High-Z.
12. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and 50pF; V_{OL} = 0.8V and V_{OH} = 2V.
14. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS# and RAS# must be pulsed HIGH for ^{t}CP.
15. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC [^{t}RAC no longer applied]. With or without the ^{t}RCD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
16. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA [^{t}RAC and ^{t}CAC no longer applied]. With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
17. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
18. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
19. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS# and RAS# or OE# go back to V_{IH}) is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle.
20. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
21. During a READ cycle, if OE# is LOW then taken HIGH before CAS# goes HIGH, Q goes open. If OE# is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.
23. All other inputs at V_{CC} -0.2V.
24. Write command is defined as WE# going LOW.
25. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if CAS# remains LOW and OE# is taken back LOW after ^{t}OEH is met.
26. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur.
27. The first CAS#x edge to transition LOW.
28. The last CAS#x edge to transition HIGH.
29. Output parameter (DQx) is referenced to corresponding CAS# input, DQ0-DQ7 by CASL# and DQ8-DQ15 by CASH#.
30. Last falling CAS#x edge to first rising CAS#x edge.
31. Last rising CAS#x edge to next cycle's last rising CAS#x edge.
32. Last rising CAS#x edge to first falling CAS#x edge.
33. First DQs controlled by the first CAS#x to go LOW.
34. Last DQs controlled by the last CAS#x to go HIGH.
35. Each CAS#x must meet minimum pulse width.
36. Last CAS#x to go LOW.
37. All DQs controlled, regardless CASL# and CASH#.
38. Column address changed once each cycle.
39. The 3ns minimum is a parameter guaranteed by design.

READ CYCLE



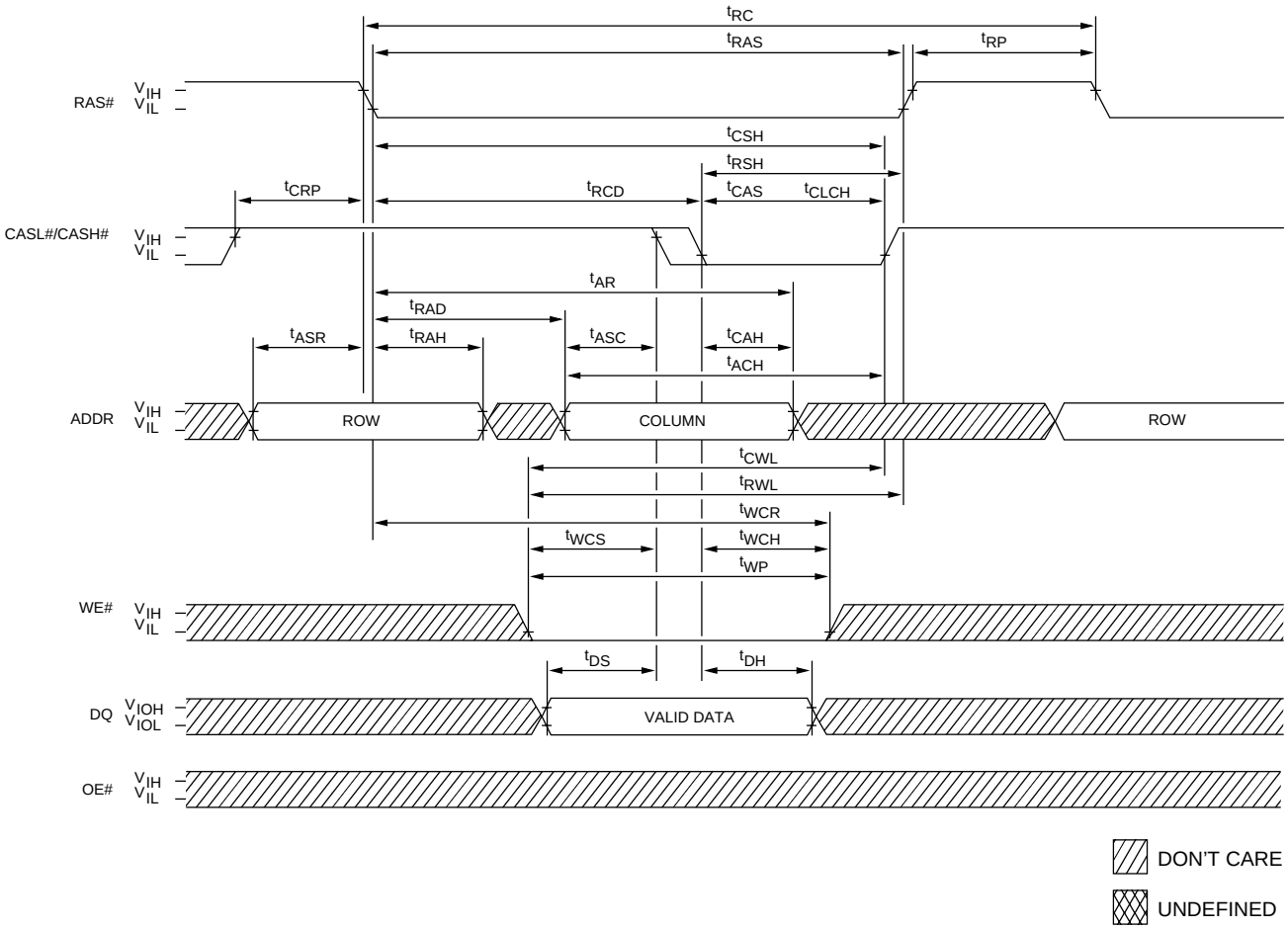
TIMING PARAMETERS

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		20		25		30	ns
tAR	30		40		40		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		12		15		15	ns
tCAH	7		8		10		ns
tCAS	6	10,000	8	10,000	10	10,000	ns
tCLCH	10		10		10		ns
tCLZ	3		3		3		ns
tCRP	5		5		5		ns
tCSH	37		40		45		ns
tOD	3	8	3	10	3	15	ns
tOE		12		15		15	ns

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOES		5		5		5	ns
tOFF	3	15	3	15	3	15	ns
tRAC		40		50		60	ns
tRAD	7		13		15		ns
tRAH	7		10		10		ns
tRAS	40	10,000	50	10,000	60	10,000	ns
tRC	75		100		110		ns
tRCD	17		18		20		ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tRP	25		30		35		ns
tRRH	0		0		0		ns
tRSH	7		8		10		ns

NOTE: 1. tOFF is referenced from the rising edge of RAS# or CAS#, whichever occurs last.

EARLY WRITE CYCLE

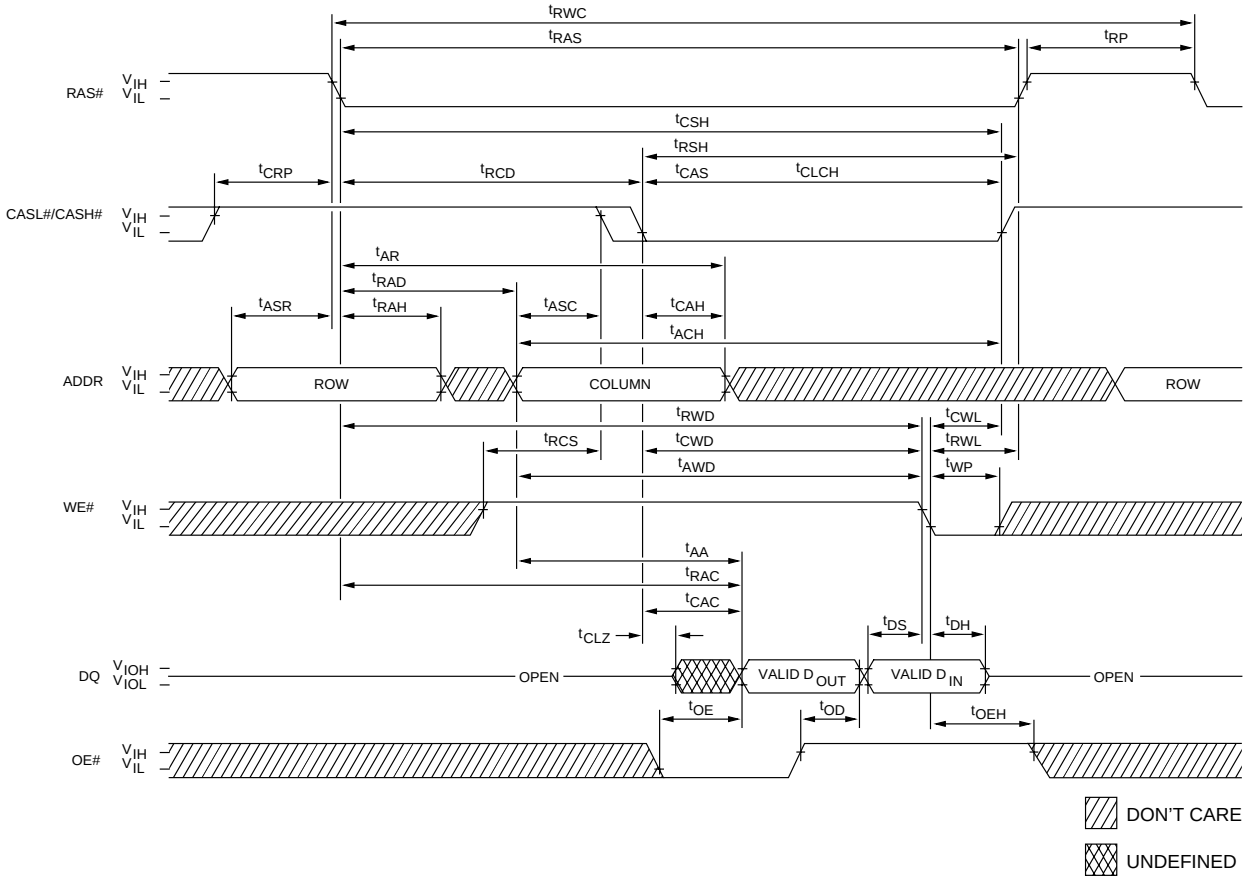


TIMING PARAMETERS

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tACH	15		15		15		ns
tAR	30		40		40		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAH	7		8		10		ns
tCAS	6	10,000	8	10,000	10	10,000	ns
tCLCH	10		10		10		ns
tCRP	5		5		5		ns
tCSH	37		40		45		ns
tCWL	7		8		10		ns
tDH	7		8		10		ns
tDS	0		0		0		ns

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tRAD	7		13		15		ns
tRAH	7		10		10		ns
tRAS	40	10,000	50	10,000	60	10,000	ns
tRC	75		100		110		ns
tRCD	17		18		20		ns
tRP	25		30		35		ns
tRSH	7		8		10		ns
tRWL	7		8		10		ns
tWCH	7		8		10		ns
tWCR	30		40		40		ns
tWCS	0		0		0		ns
tWP	7		8		10		ns

READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

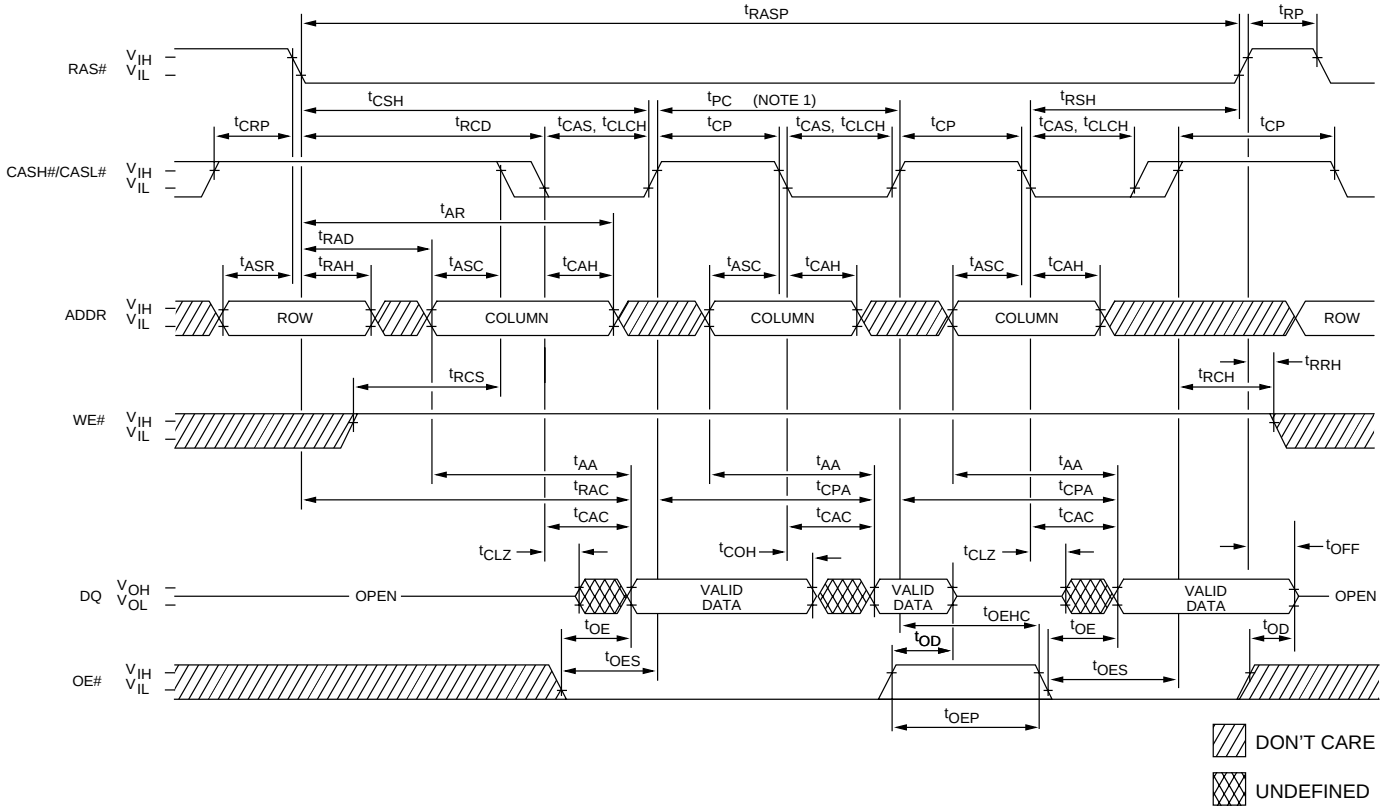


TIMING PARAMETERS

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		20		25		30	ns
tACH	15		15		15		ns
tAR	30		40		40		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tAWD	37		48		55		ns
tCAC		12		15		15	ns
tCAH	7		8		10		ns
tCAS	6	10,000	8	10,000	10	10,000	ns
tCLCH	10		10		10		ns
tCLZ	3		3		3		ns
tCRP	5		5		5		ns
tCSH	37		40		45		ns
tCWD	30		35		40		ns
tCWL	7		8		10		ns
tDH	7		8		10		ns

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tDS	0		0		0		ns
tOD	3	8	3	10	3	15	ns
tOE		12		15		15	ns
tOEH	6		10		15		ns
tRAC		40		50		60	ns
tRAD	7		13		15		ns
tRAH	7		10		10		ns
tRAS	40	10,000	50	10,000	60	10,000	ns
tRCD	17		18		20		ns
tRCS	0		0		0		ns
tRP	25		30		35		ns
tRSH	7		8		10		ns
tRWC	105		126		140		ns
tRWD	60		69		85		ns
tRWL	7		8		10		ns
tWP	7		8		10		ns

EDO-PAGE-MODE READ CYCLE



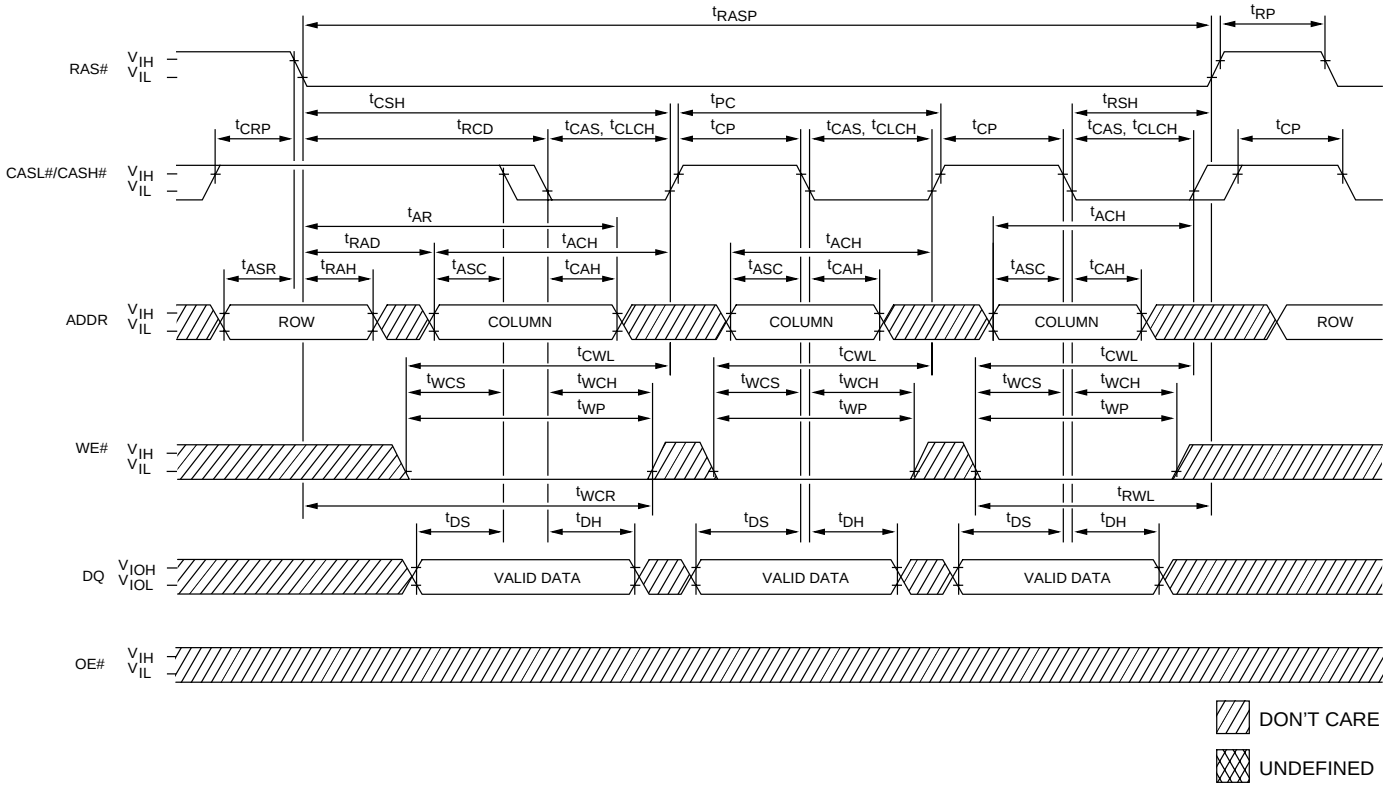
TIMING PARAMETERS

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		20		25		30	ns
tAR	30		40		40		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		12		15		15	ns
tCAH	7		8		10		ns
tCAS	6	10,000	8	10,000	10	10,000	ns
tCLCH	10		10		10		ns
tCLZ	3		3		3		ns
tCOH	3		3		3		ns
tCP	6		8		10		ns
tCPA		25		28		35	ns
tCRP	5		5		5		ns
tCSH	37		40		45		ns
tOD	3	8	3	10	3	15	ns
tOE		12		15		15	ns

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOEHC	10		10		10		ns
tOEP	10		10		10		ns
tOES	5		5		5		ns
tOFF	3	15	3	15	3	15	ns
tPC	15		20		25		ns
tRAC		40		50		60	ns
tRAD	7		13		15		ns
tRAH	7		10		10		ns
tRASP	40	100,000	50	100,000	60	100,000	ns
tRCD	17		18		20		ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tRP	25		30		35		ns
tRRH	0		0		0		ns
tRSH	7		8		10		ns

NOTE: 1. tPC can be measured from falling edge of CAS# to falling edge of CAS#, or from rising edge of CAS# to rising edge of CAS#. Both measurements must meet the tPC specification.

EDO-PAGE-MODE EARLY WRITE CYCLE

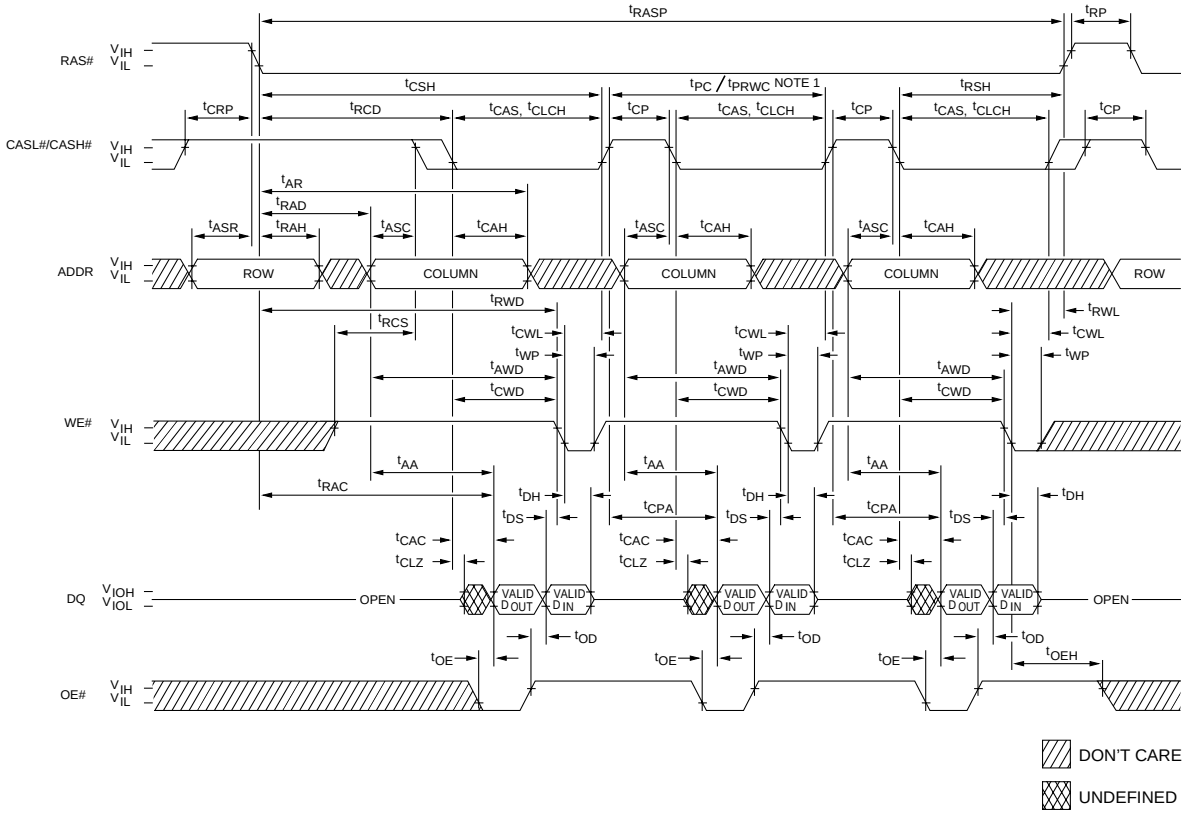


TIMING PARAMETERS

	-4		-5		-6		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tACH	15		15		15		ns
tAR	30		40		40		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAH	7		8		10		ns
tCAS	6	10,000	8	10,000	10	10,000	ns
tCLCH	10		10		10		ns
tCP	6		8		10		ns
tCRP	5		5		5		ns
tCSH	37		40		45		ns
tCWL	7		8		10		ns
tDH	7		8		10		ns
tDS	0		0		0		ns

	-4		-5		-6		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tPC	15		20		25		ns
tRAD	7		13		15		ns
tRAH	7		10		10		ns
tRASP	40	100,000	50	100,000	60	100,000	ns
tRCD	17		18		20		ns
tRP	25		30		35		ns
tRSH	7		8		10		ns
tRWL	7		8		10		ns
tWCH	7		8		10		ns
tWCR	30		40		40		ns
tWCS	0		0		0		ns
tWP	7		8		10		ns

EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



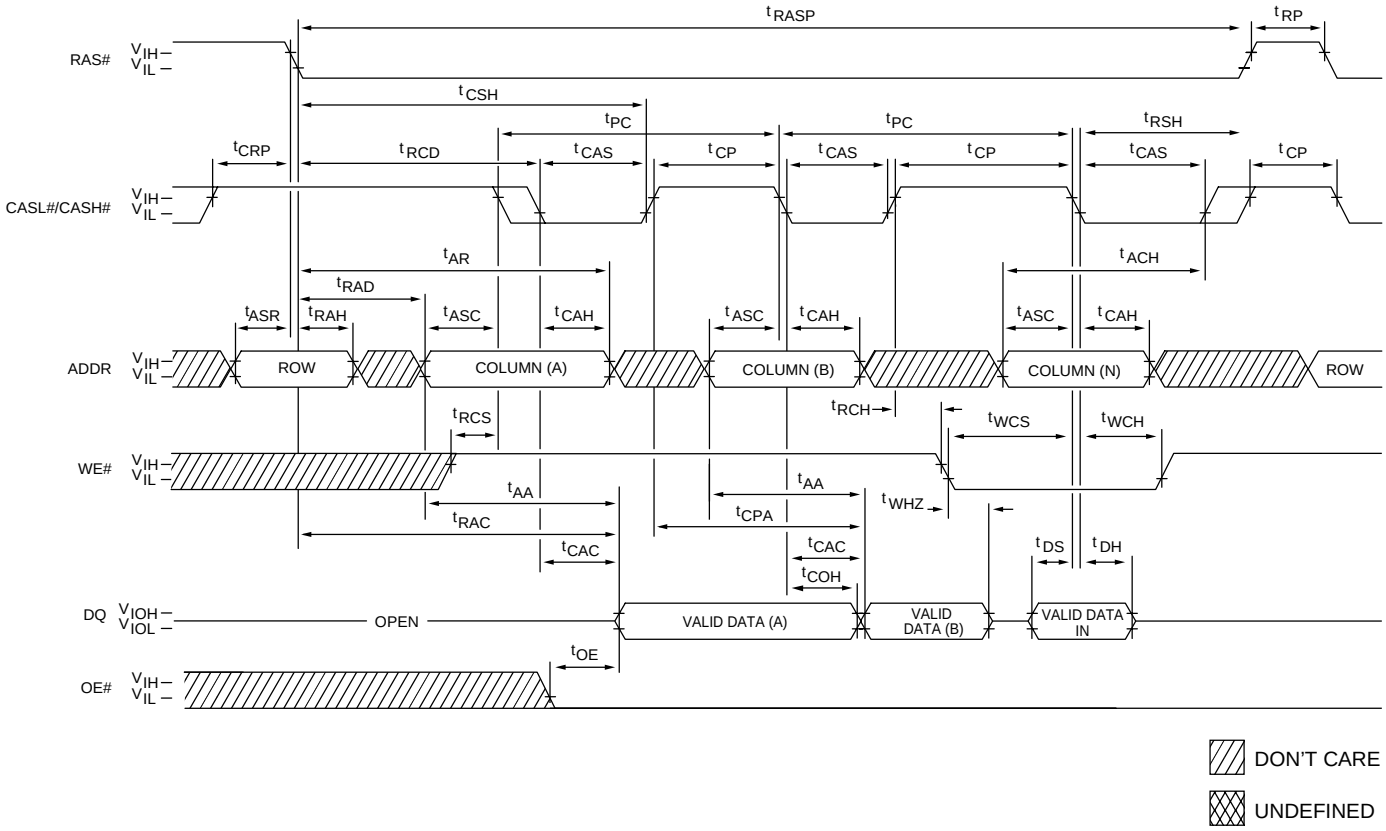
TIMING PARAMETERS

SYMBOL	-4 MIN	-4 MAX	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		20		25		30	ns
tAR	30		40		40		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tAWD	37		48		55		ns
tCAC		12		15		15	ns
tCAH	7		8		10		ns
tCAS	6	10,000	8	10,000	10	10,000	ns
tCLCH	10		10		10		ns
tCLZ	3		3		3		ns
tCP	6		8		10		ns
tCPA		25		28		35	ns
tCRP	5		5		5		ns
tCSH	37		40		45		ns
tCWD	30		35		40		ns
tCWL	7		8		10		ns
tDH	7		8		10		ns

SYMBOL	-4 MIN	-4 MAX	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tDS	0		0		0		ns
tOD	3	8	3	10	3	15	ns
tOE		12		15		15	ns
tOEH	6		10		15		ns
tPC	15		20		25		ns
tPRWC	60		65		72		ns
tRAC		40		50		60	ns
tRAD	7		13		15		ns
tRAH	7		10		10		ns
tRASP	40	100,000	50	100,000	60	100,000	ns
tRCD	17		18		20		ns
tRCS	0		0		0		ns
tRP	25		30		35		ns
tRSH	7		8		10		ns
tRWD	60		69		85		ns
tRWL	7		8		10		ns
tWP	7		8		10		ns

NOTE: 1. tPC can be measured from falling edge to falling edge of CAS#, or from rising edge to rising edge of CAS#. Both measurements must meet the tPC specification.

EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Psuedo READ-MODIFY-WRITE)

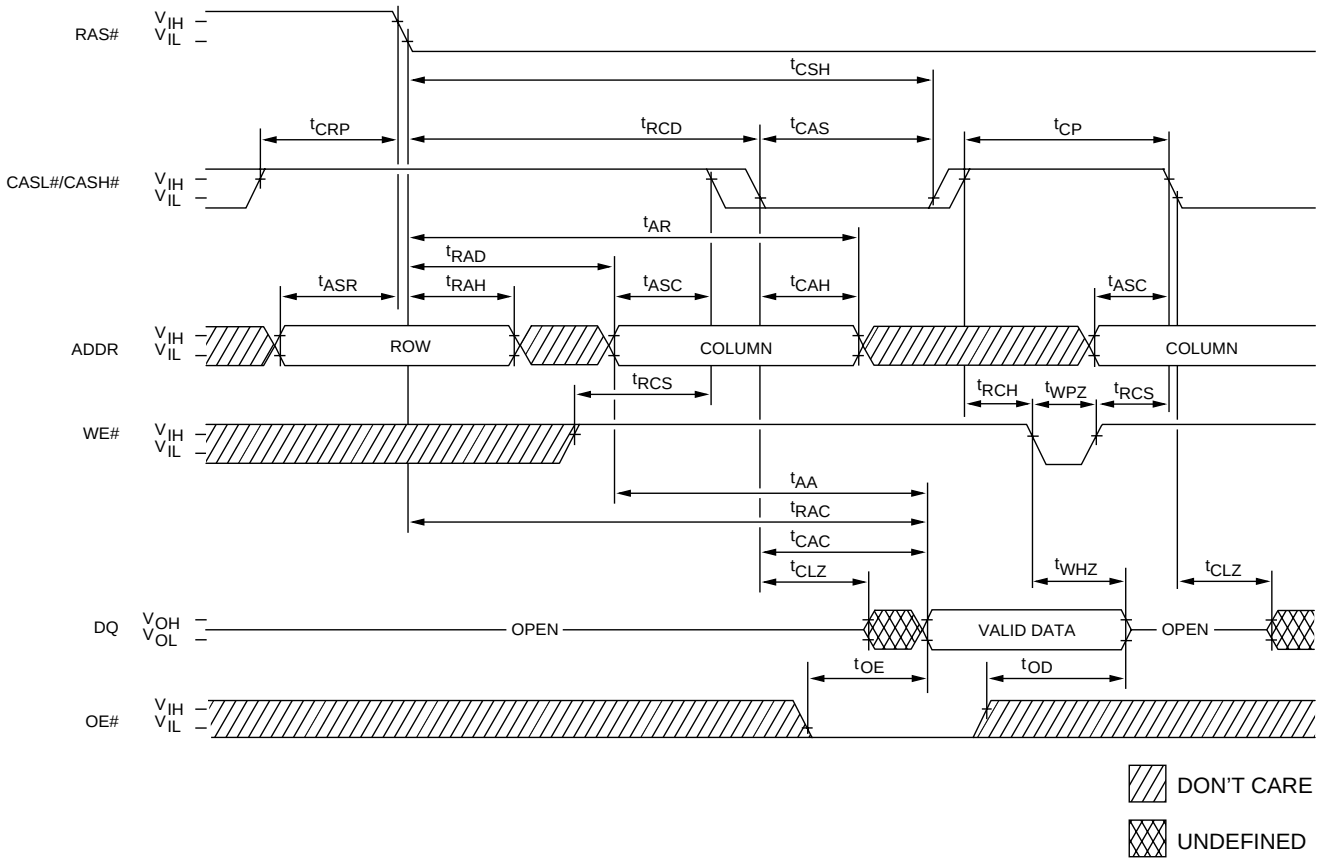


TIMING PARAMETERS

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		20		25		30	ns
tACH	15		15		15		ns
tAR	30		40		40		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		12		15		15	ns
tCAH	7		8		10		ns
tCAS	6	10,000	8	10,000	10	10,000	ns
tCOH	3		3		3		ns
tCP	6		8		10		ns
tCPA		25		28		35	ns
tCRP	5		5		5		ns
tCSH	37		40		45		ns
tDH	7		8		10		ns
tDS	0		0		0		ns

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOE		12		15		15	ns
tPC	15		20		25		ns
tRAC		40		50		60	ns
tRAD	7		13		15		ns
tRAH	7		10		10		ns
tRASP	40	100,000	50	100,000	60	100,000	ns
tRCD	17		18		20		ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tRP	25		30		35		ns
tRSH	7		8		10		ns
tWCH	7		8		10		ns
tWCS	0		0		0		ns
tWHZ	3	13	3	13	3	15	ns

READ CYCLE
(with WE#-controlled disable)



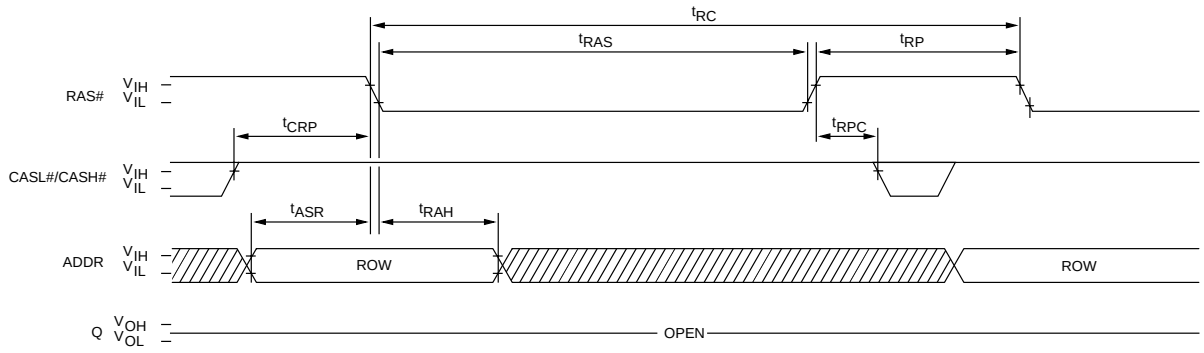
TIMING PARAMETERS

SYMBOL	-4 MIN	-4 MAX	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		20		25		30	ns
tAR	30		40		40		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		12		15		15	ns
tCAH	7		8		10		ns
tCAS	6	10,000	8	10,000	10	10,000	ns
tCLZ	3		3		3		ns
tCP	6		8		10		ns
tCRP	5		5		5		ns
tCSH	37		40		45		ns

SYMBOL	-4 MIN	-4 MAX	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	3	8	3	10	3	15	ns
tOE		12		15		15	ns
tRAC		40		50		60	ns
tRAD	7		13		15		ns
tRAH	7		10		10		ns
tRCH	0		0		0		ns
tRCD	17		18		20		ns
tRCS	0		0		0		ns
tWHZ	3	13	3	13	3	15	ns
tWPZ	10		10		10		ns

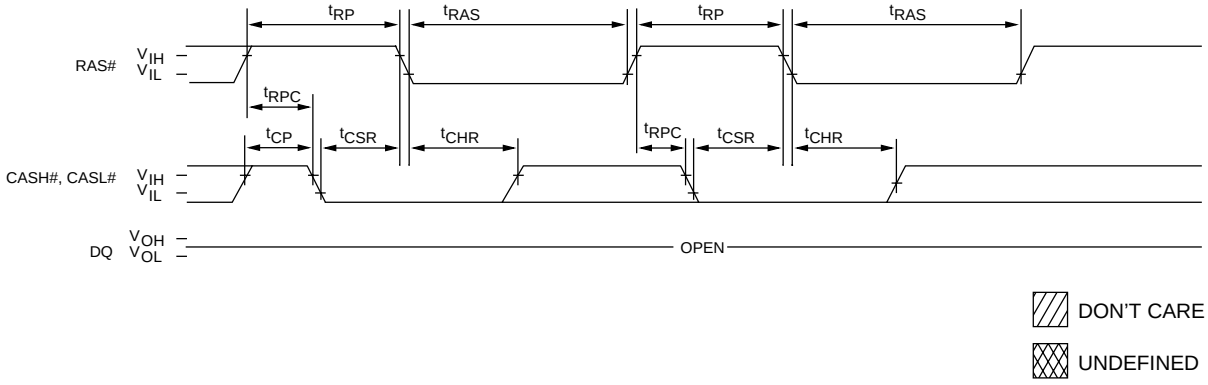
RAS#-ONLY REFRESH CYCLE

(OE#, WE# = DON'T CARE)



CBR REFRESH CYCLE

(Addresses; OE#, WE# = DON'T CARE)

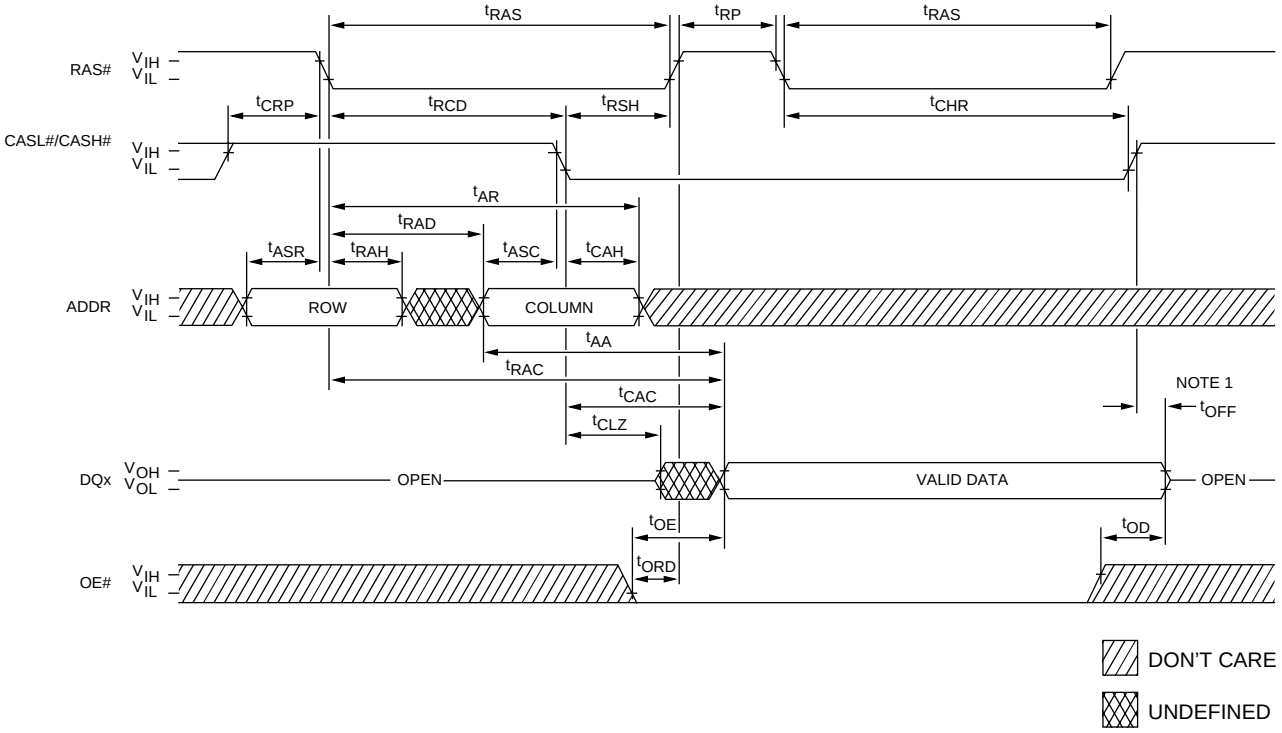


TIMING PARAMETERS

SYMBOL	-4 MIN	-4 MAX	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		0		ns
tCHR	10		10		10		ns
tCP	6		8		10		ns
tCRP	5		5		5		ns
tCSR	10		10		10		ns

SYMBOL	-4 MIN	-4 MAX	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAH	7		10		10		ns
tRAS	40	10,000	50	10,000	60	10,000	ns
tRC	75		100		110		ns
tRP	25		30		35		ns
tRPC	10		10		10		ns

HIDDEN REFRESH CYCLE [24]
(WE# = HIGH; OE# = LOW)



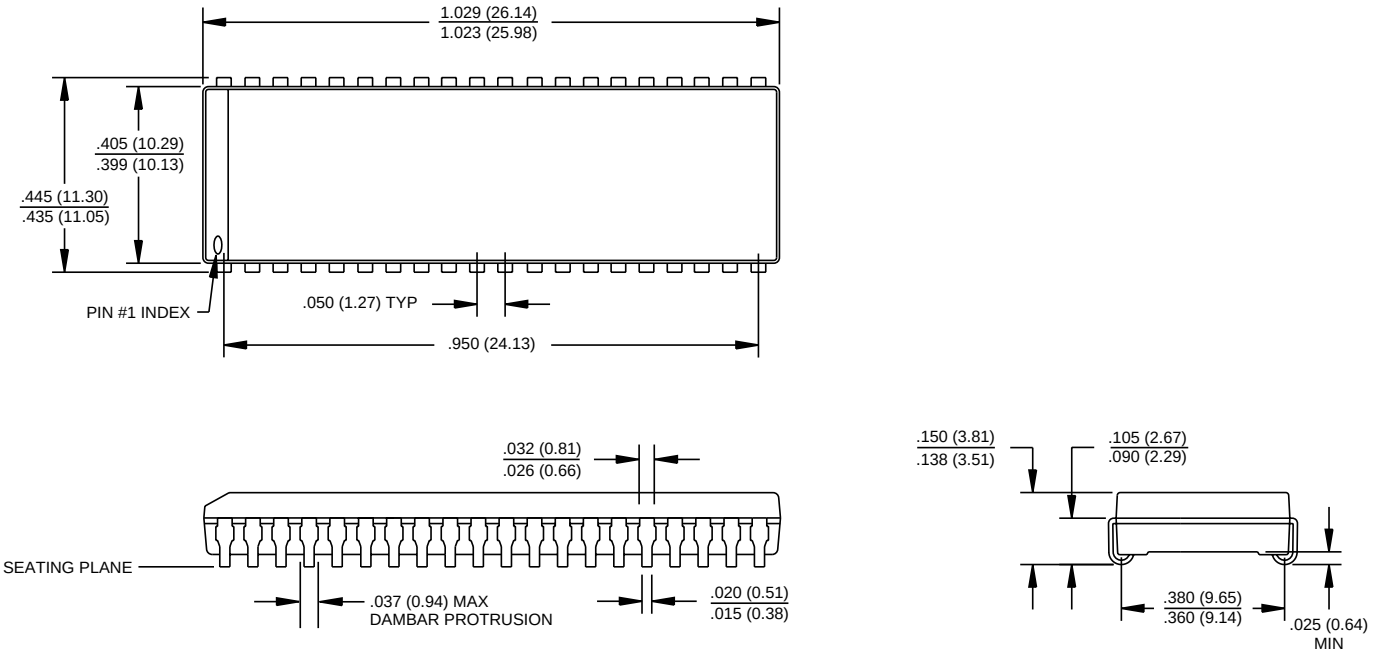
TIMING PARAMETERS

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		20		25		30	ns
tAR	30		40		40		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		12		15		15	ns
tCAH	7		8		10		ns
tCHR	10		10		10		ns
tCLZ	3		3		3		ns
tCRP	5		5		5		ns
tOD	3	8	3	10	3	15	ns

	-4		-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOE		12		15		15	ns
tOFF	3	15	3	15	3	15	ns
tORD	0		0		0		ns
tRAC		40		50		60	ns
tRAD	7		13		15		ns
tRAH	7		10		10		ns
tRAS	40	10,000	50	10,000	60	10,000	ns
tRCD	17		18		20		ns
tRP	25		30		35		ns
tRSH	7		8		10		ns

40-PIN PLASTIC SOJ (400 mil)

DA-5



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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