WIDE DRAM

256K x 16 DRAM

FAST-PAGE-MODE WITH EXTENDED DATA-OUT

FEATURES

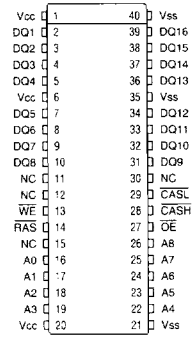
- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 500mW active, typical
- All device pins are TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFRORE-$\overline{RAS}$ (CBR) and HIDDEN
- Optional FAST-PAGE-MODE with EXTENDED DATA-OUT access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C16271 only)

OPTIONS — MARKING

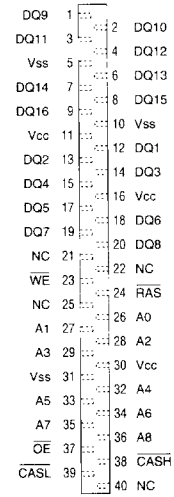
- Timing
  - 70ns access — -7
  - 80ns access — -8
- Write Cycle Access
  - BYTE or WORD via $\overline{CAS}$ (nonmaskable) — 16270
  - BYTE or WORD via $\overline{CAS}$ (maskable) — 16271
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
  - Plastic ZIP (475 mil) — Z
- Part Number Example: MT4C16270DJ-7

PIN ASSIGNMENT (Top View)

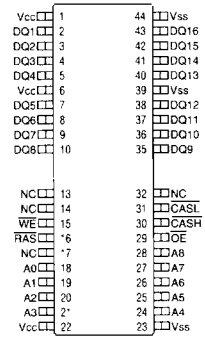
40-Pin SOJ (SDB-2)



40-Pin ZIP (SDA-2)



40-Pin TSOP (SDE-2)



GENERAL DESCRIPTION

The MT4C16270/1 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16270 and MT4C16271 have both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The MT4C16271 is also able to perform WRITE-PER-BIT accesses.

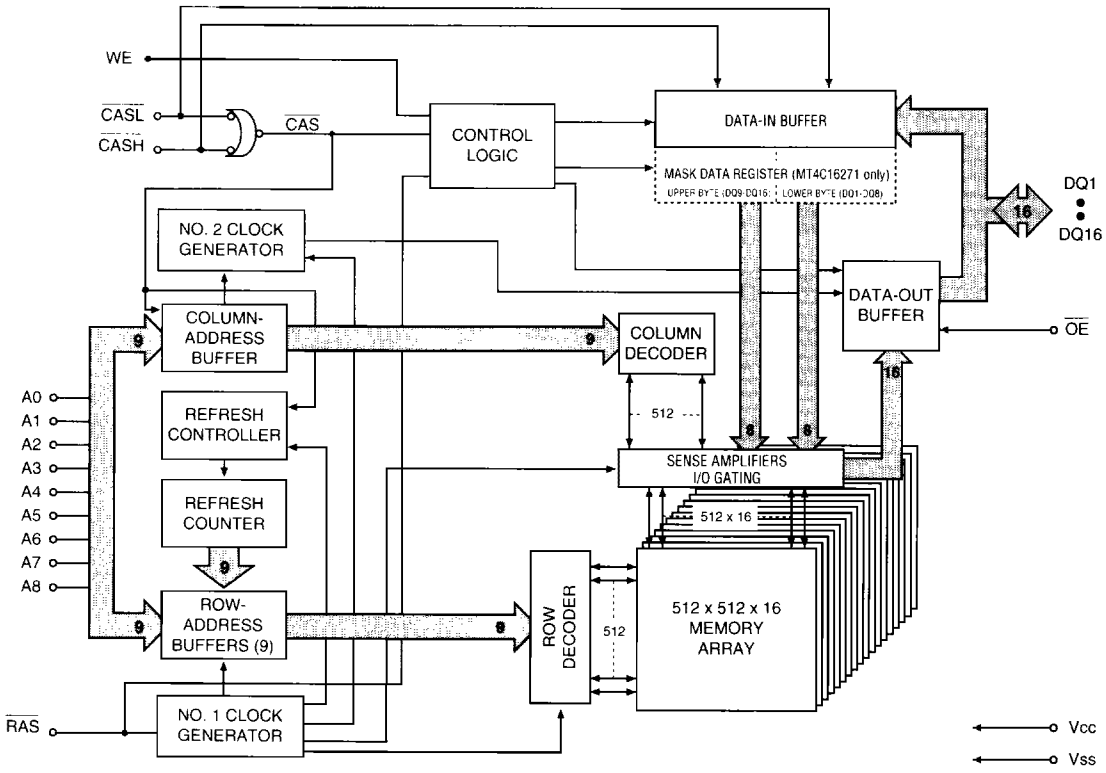
Both the MT4C16270 and MT4C16271 offer an accelerated FAST-PAGE-MODE cycle through a feature called EXTENDED DATA-OUT.

The MT4CMT4C16270/1 $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and by the last to transition back HIGH. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE

cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner.

The MT4C16271 functions in the same manner as MT4C16270; it has NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C216271 to operate with either normal WRITE cycles or with NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch in the 9 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C16271only).
28	30	38	$\overline{CASH}$	Input	Column-Address Strobe Upper Byte: $\overline{CASH}$ is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during a WRITE access cycle.
27	29	37	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CASL}$ / $\overline{CASH}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ controls DQ1 through DQ16 inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C16271 also uses $\overline{WE}$ to enable the mask register during $\overline{RAS}$ time.
29	31	39	$\overline{CASL}$	Input	Column-Address Strobe Low Byte: $\overline{CASL}$ is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during a WRITE access cycle.
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CASL}$ / $\overline{CASH}$ to select one 16-bit word (or 8-bit byte) out of the 256K available words.
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{CASL}$ / $\overline{CASH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. The MT4C16270/1 allow for BYTE READ cycles.
11, 12, 15, 30	13, 14, 17, 32	21, 22, 25, 40	NC		No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	V_{CC}	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter nine bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. Both the MT4C16270 and MT4C16271 have two $\overline{CAS}$ controls, $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 256K x 16 DRAMs. The key difference is that each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$ and $\overline{RAS}$). $\overline{CASL}$ controls DQ1 through DQ8 and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C16270/1 $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C16270/1 both byte READ and byte WRITE cycle capabilities.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by $\overline{OE}$, $\overline{WE}$ and $\overline{RAS}$.

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

EXTENDED DATA-OUT

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. If $\overline{CAS}$ goes HIGH, and OE is LOW (active), the output buffers will be disabled. The MT4C16270/1 offer an accelerated FAST-PAGE-MODE cycle by eliminating output disable from $\overline{CAS}$ HIGH. This option is called EXTENDED DATA-OUT and it allows $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid (see READ and FAST-PAGE-MODE READ waveforms).

EXTENDED DATA-OUT operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after $\overline{CAS}$ goes HIGH, as long as $\overline{RAS}$ is LOW. If the DQ outputs are wire OR'd, OE must be used to disable idle banks of DRAMs. During cycles other than PAGE-MODE READ, the outputs are disabled at ^tOFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH. The ^tOFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C16270/1 can be viewed as two 256K x 8 DRAMS which have common input controls. Figure 1 illustrates the MT4C16270 BYTE WRITE and WORD WRITE cycles.

The MT4C16270/1 also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 2 illustrates the MT4C16270 BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C16271 only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C216270 does not have the MASKED WRITE cycle function.

The mask data present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port

and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a NONPERSISTENT MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 3 illustrates the MT4C16271 MASKED WRITE operation.

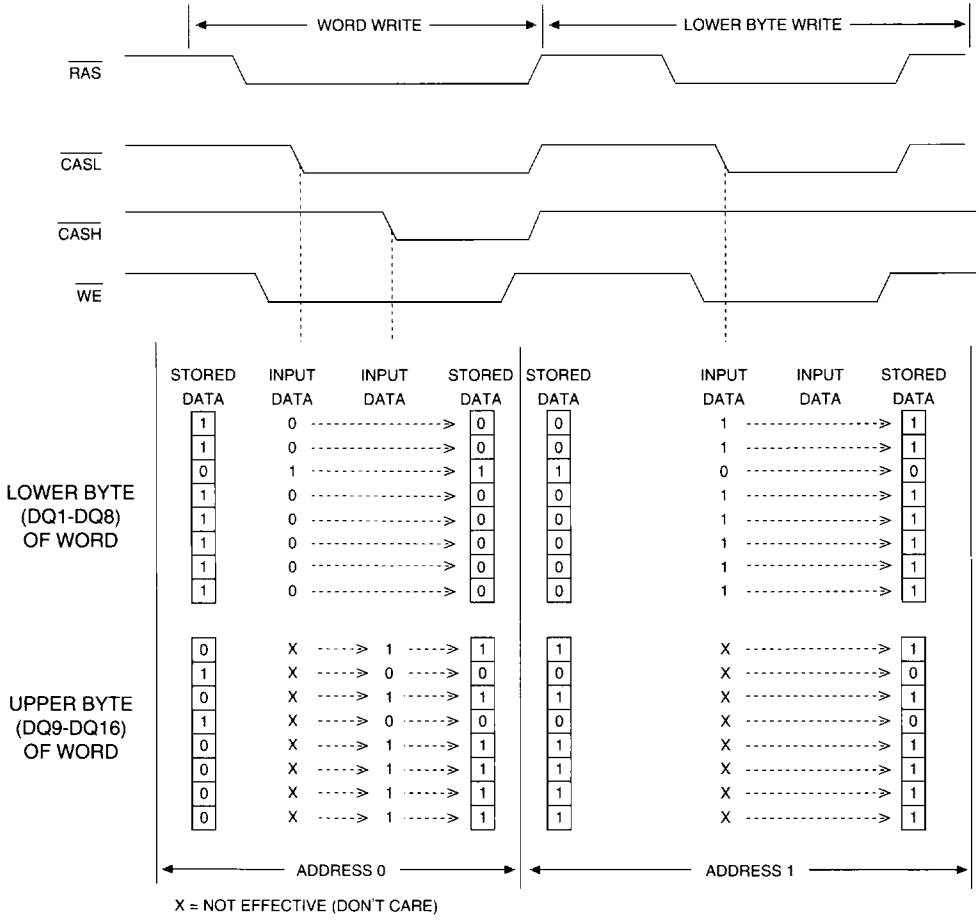


Figure 1
MT4C16270 WORD AND BYTE WRITE EXAMPLE

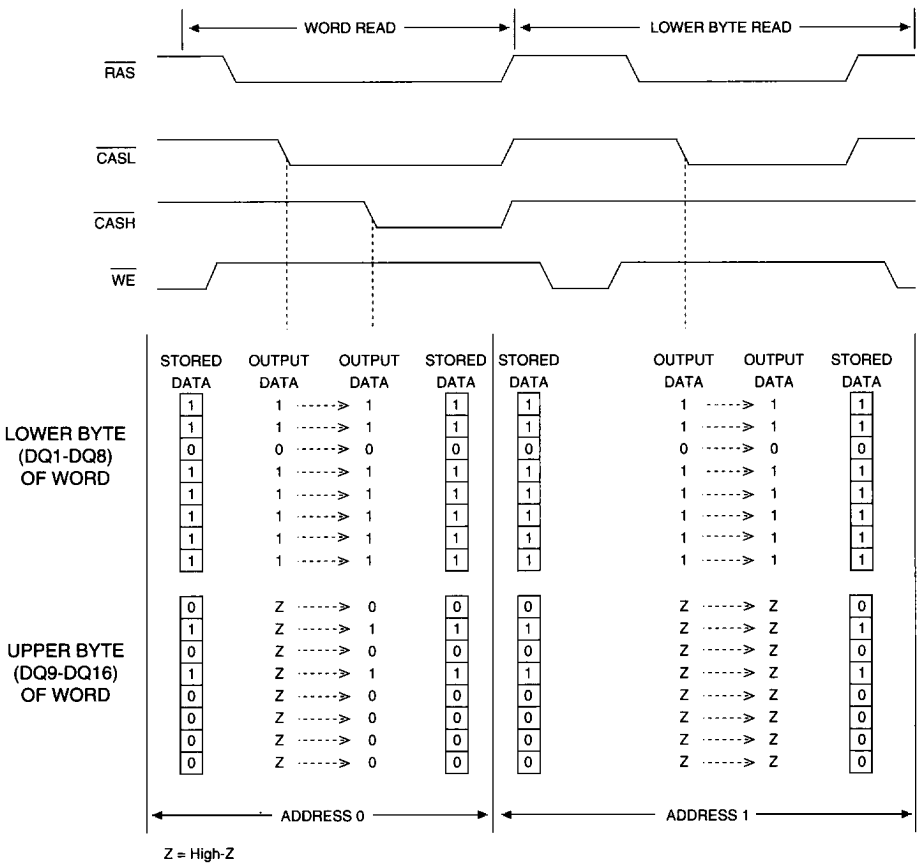


Figure 2
MT4C16270 WORD AND BYTE READ EXAMPLE

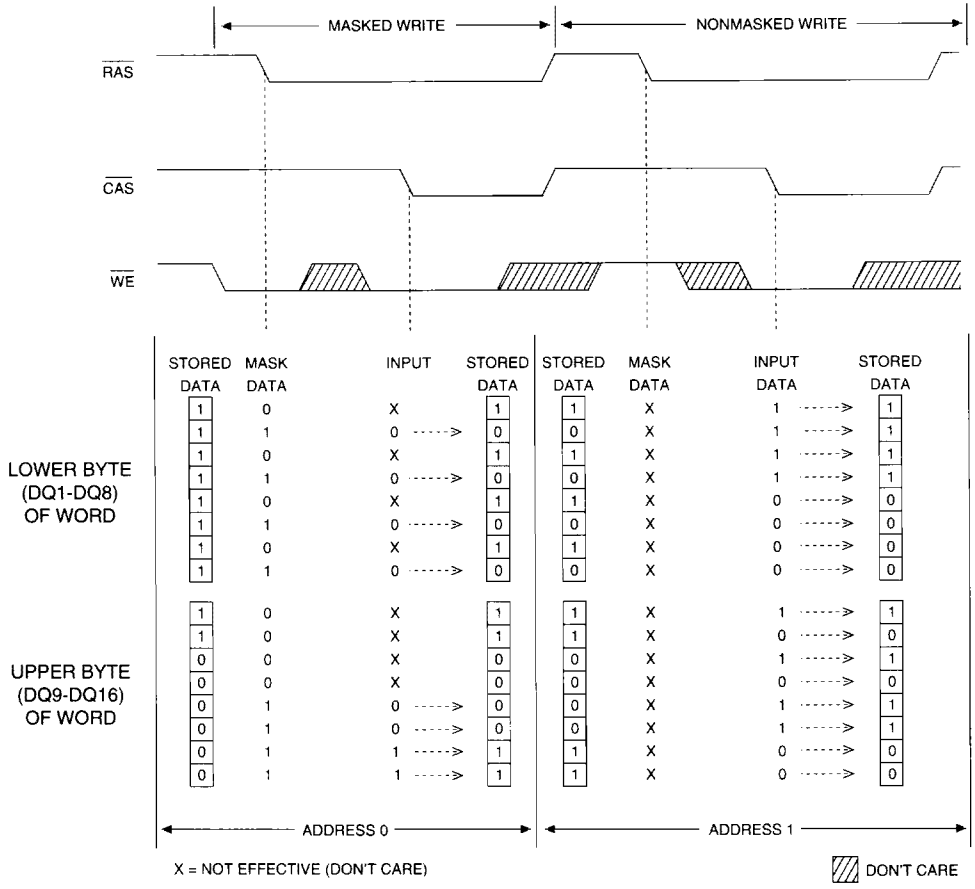


Figure 3
MT4C16271 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C16270/1

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one of the two CAS signals must be active (CASL or CASH).
5. Data-in will be dependent on the mask provided (MT4C256K16E5 only). Refer to Figure 3.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	170	150	mA	3, 4, 41
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	110	100	mA	3, 4, 41
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	170	150	mA	3, 5, 41
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	160	140	mA	3, 5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$,$\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-WRITE cycle time	^tRWC	175		195		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		ns	34
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20	ns	15, 32
Output Enable time	^tOE		20		20	ns	23, 32
Access time from column-address	^tAA		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	32
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (PAGE-MODE)	^tRASP	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		ns	39
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	15	100,000	ns	38
$\overline{CAS}$ hold time	^tCSH	70		80		ns	31
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16, 35
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	10		10		ns	35
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	ns	17, 30
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	31
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		ns	30
Column-address hold time	^tCAH	15		15		ns	30
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	26, 30
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19, 26, 31
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	32, 42

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay from $\overline{CAS}$ or $\overline{RAS}$	^tOFF	3	15	3	15	ns	20, 29, 32, 42
Output disable time	^tOD	3	15	3	15	ns	29, 40, 42
Write command setup time	^tWCS	0		0		ns	21, 26, 30
Write command hold time	^tWCH	10		10		ns	26, 39
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		ns	26
Write command pulse width	^tWP	10		10		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	26, 31
Data-in setup time	^tDS	0		0		ns	22, 32
Data-in hold time	^tDH	15		15		ns	22, 32
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	95		105		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		45		ns	21, 30
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8	ns	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5, 30
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	5, 31
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		ns	26, 27
$\overline{WE}$ hold time (MASKED WRITE)	^tWRH	15		15		ns	26
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH	^tCLCH	10		10		ns	33
Data output hold after $\overline{CAS}$ LOW	^tCOH	5		5		ns	

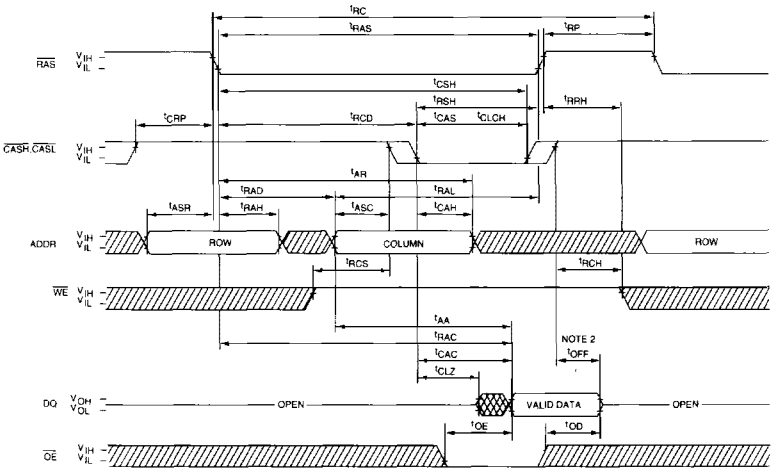
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C16271 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur.

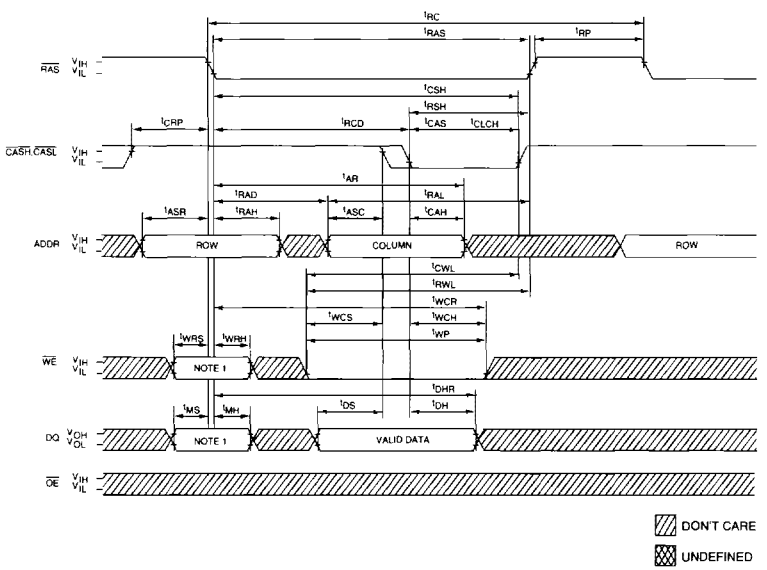
NOTES (continued)

30. The first $\overline{CAS}$x edge to transition LOW.
31. The last $\overline{CAS}$x edge to transition HIGH.
32. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
33. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
34. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
36. First DQs controlled by the first $\overline{CAS}$x to go LOW.
37. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
38. Each $\overline{CAS}$x must meet minimum pulse width.
39. Last $\overline{CAS}$x to go LOW.
40. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
41. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
42. The 3ns minimum is a parameter guaranteed by design.

READ CYCLE



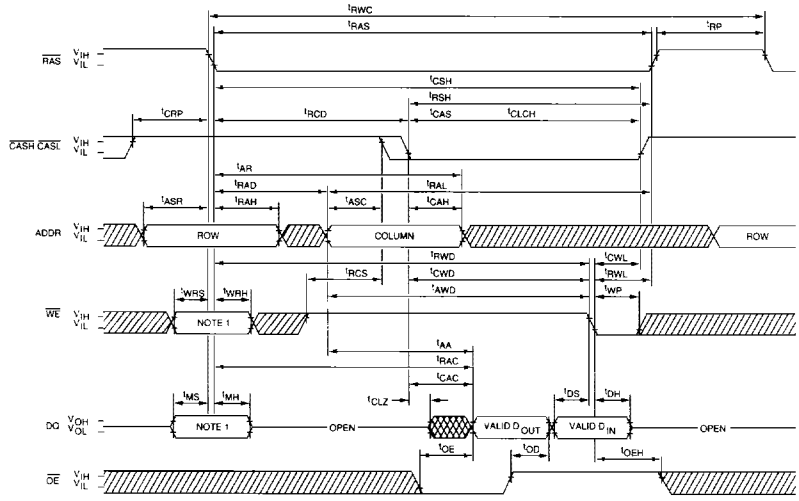
EARLY-WRITE CYCLE



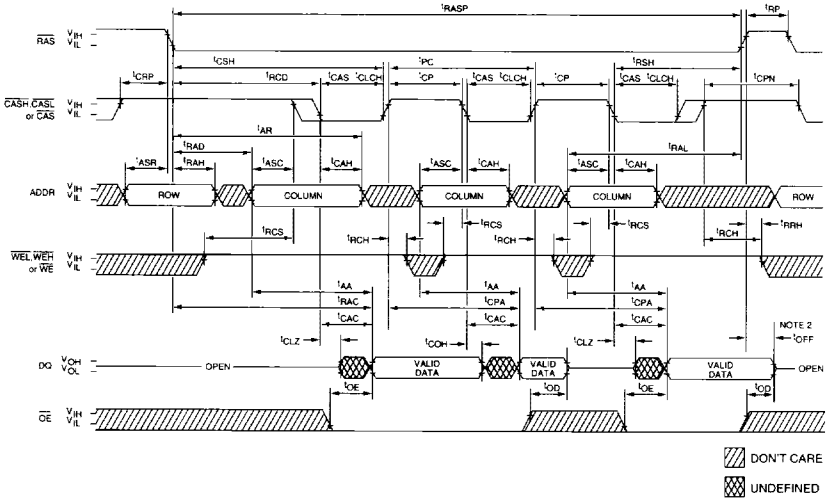
NOTE: 1. Applies to MT4C16271 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WE}$ and DQ inputs on MT4C16270 is a "don't care" at $\overline{RAS}$ time.

2. ^{t}OFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



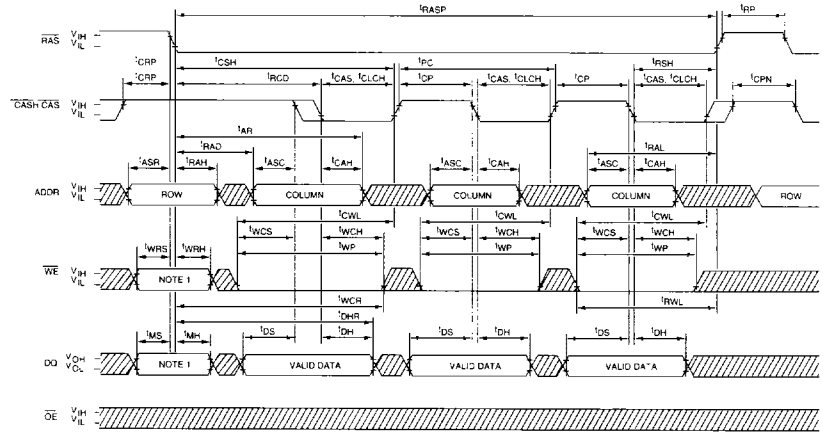
FAST-PAGE-MODE READ CYCLE with EXTENDED DATA-OUT



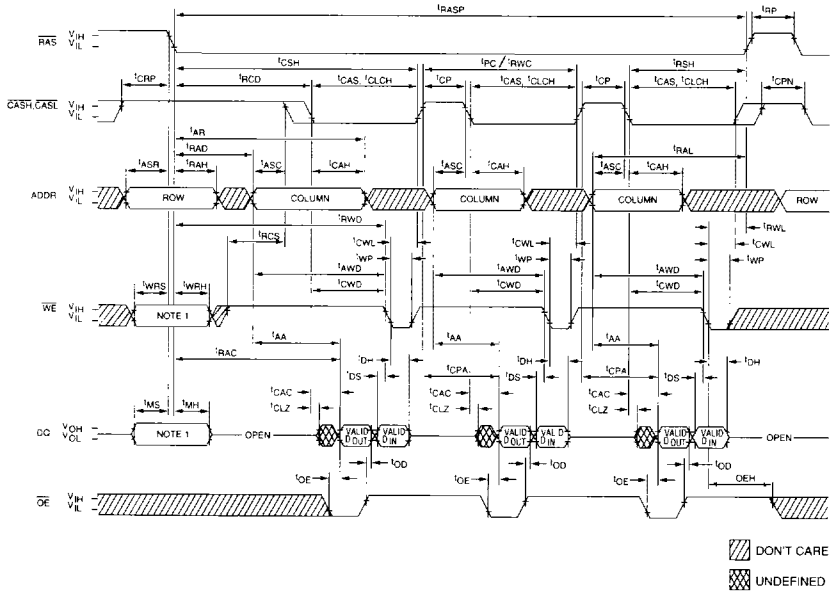
NOTE: 1. Applies to MT4C16271 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WE}$ and DQ inputs on MT4C16270 is a "don't care" at $\overline{RAS}$ time.

2. ^{t}OFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

FAST-PAGE-MODE EARLY-WRITE CYCLE

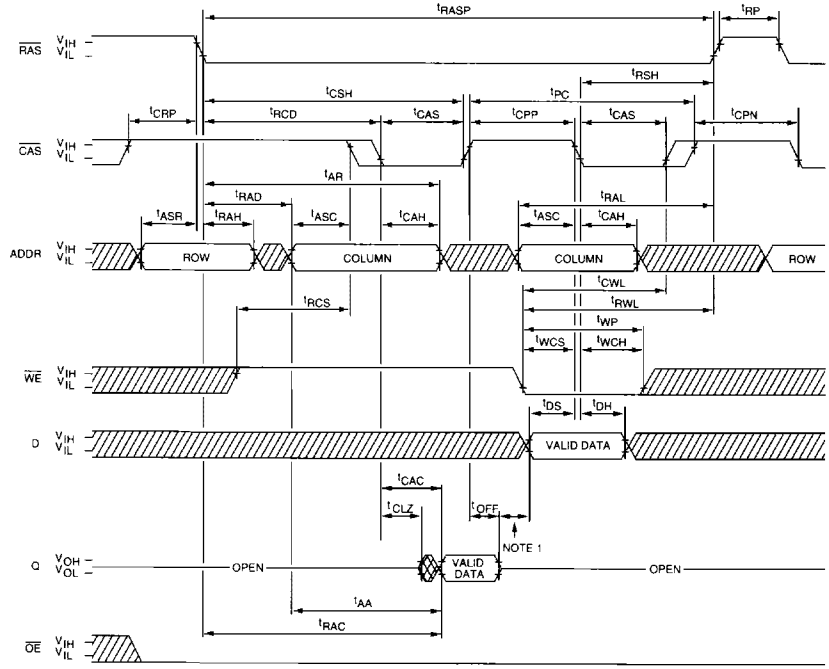


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



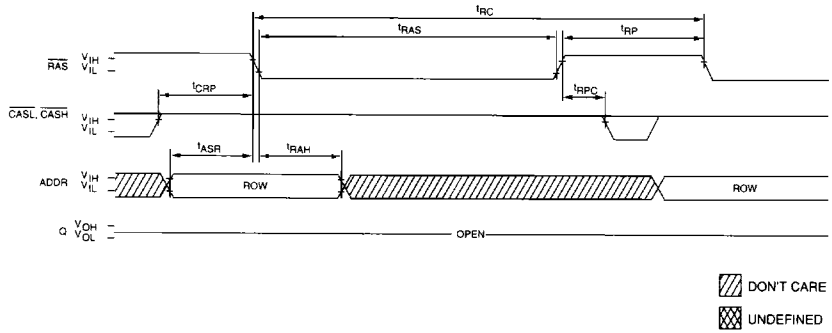
NOTE: 1. Applies to MT4C16271 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WE}$ and DQ inputs on MT4C16270 is a "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

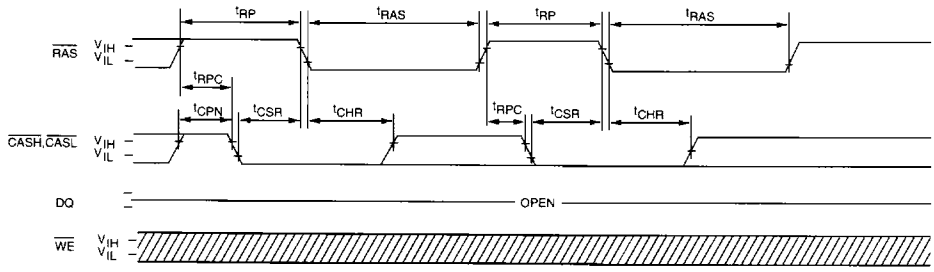


NOTE: 1. Do not drive data prior to High-Z; that is completion of tOFF. tCPP is equal to tOFF + tDS(MIN) + guardband between data-out and driving new data-in.

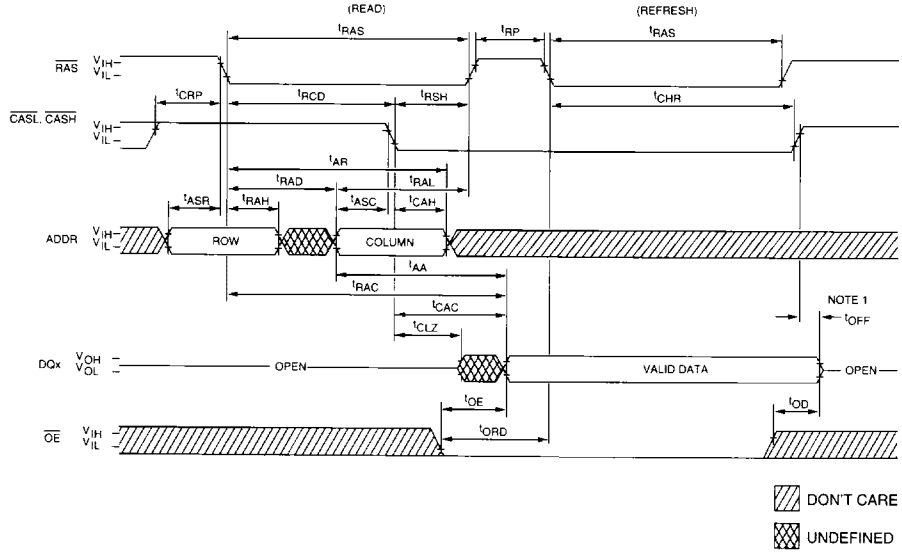
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8, OE; WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A8; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NOTE: 1. tOFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.