FORCE TECHNOLOGIES LTD

FT1002

Precision Operational Amplifier

Features

- *Guaranteed* low offset voltage
  FT1002A 60µV max
  FT1002 100µV max
- *Guaranteed* offset voltage match
  FT1002A 40µV max
  FT1002 80µV max
- *Guaranteed* low drift
  FT1002A 0.9µV/°C max
  FT1002 1.3µV/°C max
- *Guaranteed* CMRR
  FT1002A 110dB min
  FT1002 110dB min
- *Guaranteed* channel separation
  FT1002A 132dB min
  FT1002 130dB min
- *Guaranteed* matching characteristics
- Low noise 0.35µV_{P-P}

Applications

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low level signal processing
- Medical instrumentation
- Precision dual limit threshold detection
- Instrumentation amplifiers

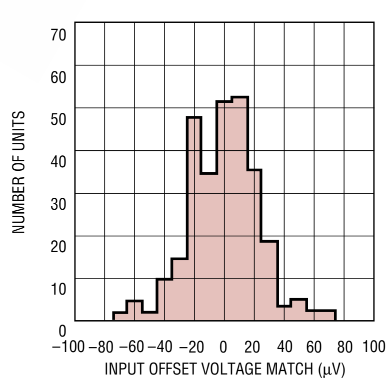
Description

The FT1002 dual, matched precision operational amplifiers combine excellent individual amplifier performance with tight matching and temperature tracking between amplifiers.

In the design, processing, and testing of the device, particular attention has been paid to the optimisation of the entire distribution of several key parameters and their matching. Consequently, the specifications of even the low cost commercial grade (FT1002C) have been spectacularly improved compared to presently available devices.

Essentially, the input offset voltage of all units is less than 80µV, and matching between amplifiers is consistently beter than 60µV (see distribution plot below). Input bias and offset currents, channel separation, common mode and power suply rejections of the FT1002C are all specified at levels which were previsouly attainable only on very expensive, selected grades of other dual devices. Power dissipation is nearly halved compared to the most popular precision duals, without adversely affecting noise or speed performance. A by-product of lower dissipation is decreased warm-up drift. For even better performance in a single precision op amp, refer to the FT1001 data sheet. A bridge signal conditioning application is shown below. This circuit illustrates the requirement for both excellent matching and individual amplifier specifications.

Distribution of Offset Voltage Match



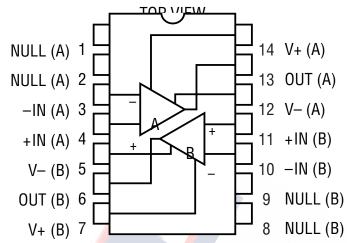
$V_S = \pm 15V$
$T_A = 25°C$
287 UNITS TESTED

Absolute Maximum Ratings

(Note 1)

Supply Voltage (Note 7) .... ±22V
Differential Input Voltage .... ±30V
Input Voltage Equal to Supply Voltage
Output Short Circuit Duration .... Indefinite
Operating Temperature Range
  FT1002AM/FT1002M .... −55°C to 125°C
  FT1002AC/FT1002C .... 0°C to 70°C
Storage Temperature Range
  All Grades .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)................. 300°C

Package/Order Information



	ORDER PART NO.	OFFSET VOLTAGE MAX at 25°C
N PACKAGE 14 PIN PLASTIC $T_{JMAX} = 125°C$, $\theta_{JA} = 100°C/W$ **NOTE:** Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B. (Note 7)	FT1002ACN FT1002CN	60μV 100μV
J PACKAGE 14 PIN HERMETIC $T_{JMAX} = 125°C$, $\theta_{JA} = 100°C/W$	FT1002AMJ FT1002MJ FT1002ACJ FT1002CJ	60μV 100μV 60μV 100μV

Electrical Characteristics Individual Amplifiers

$V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	FT1002AM/FT1002AC MIN	TYP	MAX	FT1002M/FT1002C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		20	60		25	100	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 3 and 4)		0.3	1.5		0.4	2.0	μV/month
I_{OS}	Input Offset Current			0.3	2.8		0.4	4.2	nA
I_B	Input Bias Current			±0.6	±3.0		±0.7	±4.5	nA
$\overline{e}_n$	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		0.35	0.7		0.38	0.75	μV_{p-p}
e_n	Input Noise Voltage Density	$f_O = 10Hz$ (Note 6) $f_O = 1000Hz$ (Note 3)		10.3 9.6	20.0 11.5		10.5 9.8	20.0 12.0	$nV/\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm12V$ $R_L \geq 1k\Omega$, $V_O = \pm10V$	400 250	800 500		350 220	800 500		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm13V$	110	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm3V$ to $\pm18V$	108	123		105	123		dB
R_{in}	Input Resistance Differential Mode	(Note 5)	20	100		13	80		MΩ
	Input Voltage Range		±13	±14		±13	±14		V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±13 ±12	±14 ±13.5		±13 ±12	±14 ±13.5		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 5)	0.1	0.25		0.1	0.25		V/μs
GBW	Gain Bandwidth Product	(Note 5)	0.4	0.8		0.4	0.8		MHz
P_d	Power Dissipation per amplifier	No load No load, $V_S = \pm3V$		46 4	75 7		48 4	85 8	mW

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