Programmable-Flags, 2K×9 FIFO

FEATURES

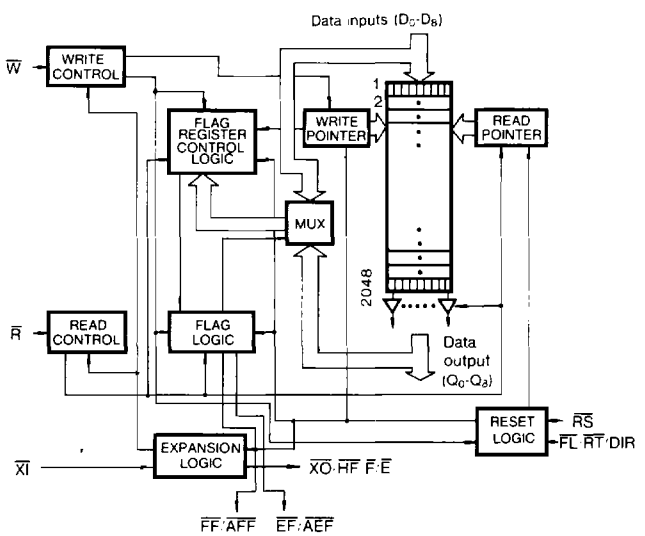
- **First-In-First-Out Dual Port Memory**
  —2K × 9 Organization
- **Very High Speed independent of depth/width**
  —30ns Cycle Time
- **Two Fully configurable Almost Full and Almost Empty Flags**
- **Register Loading via the Input or the Output pins**
- **Flag reconfiguration on the fly**
- **Programmable HF Flag or Full/Empty Flag option eliminates external counter requirement**
- **Fully Compatible with Existing FIFOs**
- **Retransmit Feature in Stand-Alone Mode**
- **Depth and Width Expandabilities**
- **Low Power Consumption**
  —Standby: 15mA
  —Active: 120mA

DESCRIPTION

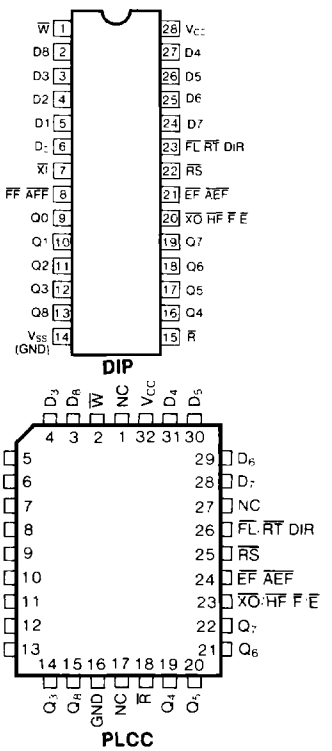
The 75C103A is a 2K×9 dual port memory that implements a special First-In-First-Out (FIFO) algorithm that loads and empties data on a first-in-first-out basis. Several fixed and configurable flags have been added for efficient device utilization. The part is fully expandable in both depth and width without any performance loss.

No address information is required for read or write operation. A ring counter generates required addresses for each operation. Data is toggled in and out of the device through the use of Write ($\overline{W}$) and Read ($\overline{R}$) pins. The Retransmit ($\overline{RT}$) pin allows one to re-read the previously read data. This feature is beneficial in applications such as graphics and data communications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top Views)



DESCRIPTION (Continued)

The FIFO status can be determined by its flag states. In non-configured mode, the device defaults to 75C03A mode, providing a Half-Full ($\overline{HF}$) Flag, a Full Flag ($\overline{FF}$) and an Empty Flag ($\overline{EF}$). The assertion and deassertion timing of these flags are identical to the flag timing of the 75C03A FIFO.

In configured mode, a maximum of three Flags are provided. The First two are the Almost-Full Flag ($\overline{AFF}$) and the Almost-Empty Flag ($\overline{AEF}$) with programmable offset. The third flag is either the $\overline{HF}$ or the $\overline{F}/\overline{E}$ flag based on bit configuration of the flag register. All three flags are reconfigurable on the fly.

The 75C103A is fabricated using proprietary high speed CMOS, 1.2 micron technology. These parts are ideal for applications requiring asynchronous and simultaneous read/write operation such as multiprocessing and data acquisition. These parts are typically used as temporary data storage for system synchronization.

Operating Mode

$\overline{RS}$	$\overline{R}$	$\overline{W}$	DIR	Mode
L	H	H	X	Device Rest
L	L	L	L	Flag register loading through input pings
L	L	L	H	Flag register loading through output pins
L	L	H	X	No OP
L	H	L	X	No OP
H	X	X	X	Normal array access

X: Don't Care

PIN DESCRIPTIONS

Symbol	Pin Number	Type	Name and Function
$\overline{W}$	1	I	WRITE: A low on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
D_0-D_8	2-6, 24-27	I	DATA INPUTS: Data on these lines are stored in the memory array or flag registers during array write or reguister programming respectively.
$\overline{XI}$	7	I	EXPANSION-IN: This pin is used for depth expansion mode. In single device mode, it should be grounded. In expanded mode, it should be connected to Expansion-out of the previous device in the daisy chain.
$\overline{FF}/\overline{AFF}$	8	O	FULL FLAG/ALMOST FULL FLAG: This output pin indicates the FIFO status. When in non-configured mode, this pin is a Full Flag output. In configured mode, it is an almost Full Flag output.
Q_0-Q_8	9-13, 16-19	I/O	DATA OUTPUTS: These pins can be used for data retrieval. The pins become inputs during register loading with DIR input high. The outputs are disabled (Three-state) during device idle ($\overline{R}$=High).
$\overline{R}$	15	I	READ: A low on this pin puts data in the memory arrary on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are Three-state when this pin is high.
$\overline{XO}/\overline{HF}/\overline{F}/\overline{E}$	20	O	EXPANSION OUT/HALF FULL/FULL/EMPTY: This pin's function is determined by its operation mode. When in single device mode, this pin is either $\overline{HF}$ Flag or a Full/Empty Flag, depending on the state of the 9th bit of Almost Full Flag Register. The pin is an $\overline{XO}$ output when the part is in depth expansion mode.
$\overline{EF}/\overline{AEF}$	21	O	EMPTY FLAG/ALMOST EMPTY FLAG: This output pin indicates the FIFO status. When in non-configured mode, this pin is an Empty flag output. When in configured mode, it is an Almost Empty Flag output. This pin is active low.

PIN DESCRIPTIONS (Continued)

Symbol	Pin Number	Type	Name and Function
$\overline{RS}$	22	I	RESET: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
$\overline{FL}/\overline{RT}$/DIR	23	I	FIRST LOAD/RETRANSMIT/DIRECTION: When in single device mode, this pin can be used to reread the previously read data. When in register load mode, the pin is used for register loading direction. When it is low, registers are loaded through the input pins. When it is high, registers are loaded through the output pins. In depth expansion mode, this pin should be tied low if the device is the first one in the chain and tied high if it is not the first one.
GND	14	I	GROUND
V_{CC}	28	I	V_{CC}

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−0.5 to +7.0	V
Operating Temperature	T_A	0 to + 70	°C
Temperature Under Bias	T_{bias}	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
DC Output Current	I_{OUT}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	—	V
Input Low Voltage	V_{IL}	—	—	0.8	V

DC OPERATING CHARACTERISTICS (V_{CC}=5V±10%)

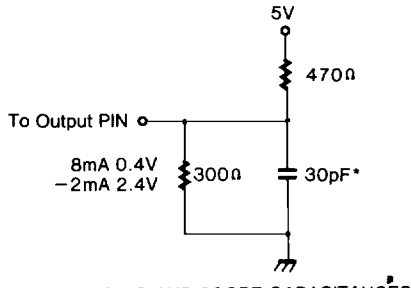
Parameter	Symbol	Min	Typ	Max	Unit
Active Supply Current[1,2]	I_{CC}	—	—	60	mA
Standby Current-TTL[1] (All inputs=V_{IH})	I_{SB1}	—	—	15	mA
Standby Current-CMOS[1] (All inputs=V_{CC}-0.2V)	I_{SB2}	—	—	5	mA
Input Leakage Current[3]	I_{IL}	−1	—	1	μA
Output Leakage Current[4]	I_{OL}	−10	—	10	μA
Output High Voltage Level (I_{OH}=−2mA)	V_{OH}	2.4	—	—	V
Output Low Voltage Level (I_{OL}=8mA)	V_{OL}	—	—	0.4	V

NOTES: 1. I_{CC} and I_{SB} measurements are made with outputs open.
2. Active supply current is 60mA for −50ns, 100mA for −35ns and 120mA for −25ns and −20ns.
3. Measurements with GND≤V_{IN}≤V_{CC}
4. $\overline{R}$≥V_{IH}, GND≤V_{OUT}≤V_{CC}.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

Figure 1. Output Load



* INCLUDES JIG AND SCOPE CAPACITANCES

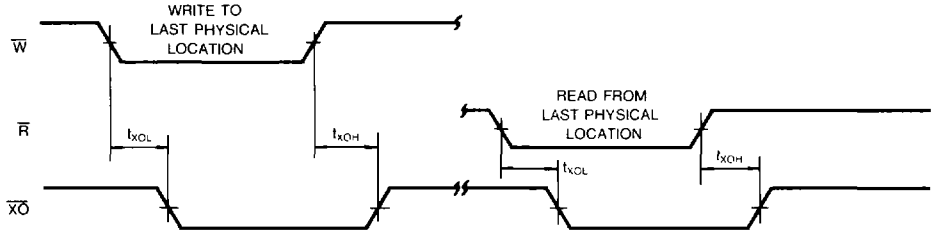
CAPACITANCE (T_A=+25°C, f=1.0 MHz)

Symbol	Parameter[1]	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	7	pF

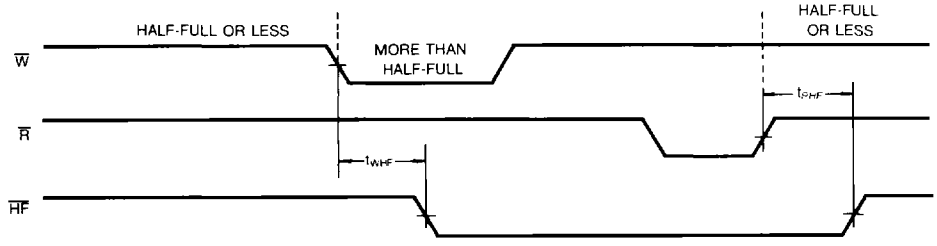
NOTE: This parameter is sampled and not 100% tested.

NOTE: Generating $\overline{R}/\overline{W}$ Signals—When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important not to have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements); although the minimum pulse width low for the R and $\overline{W}$ are specified in tens of nanosecond, a glitch of 3ns can affect the read or write pointer and cause it to increment.

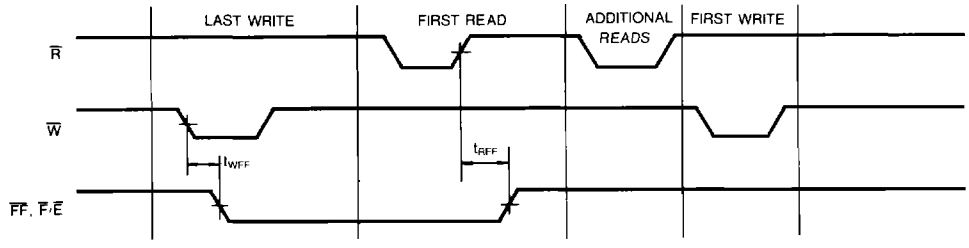
Expansion-Out Timing Diagram



Half Full Flag Timing (Configured or nonconfigured mode)



Full Flag timing (Pin 8 or 20)



AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%, T_A=0°C to +70°C) (Non-Configured Mode)

Symbol	Parameter	75C103A-20		75C103A-25		75C103A-35		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	30		35		45		ns
t_A	Access Time		20		25		35	ns
t_{RR}	Read Recovery Time	10		10		10		ns
t_{RPW}	Read Pulse Width[2]	20		25		35		ns
t_{DV}	Data Valid after $\overline{R}$ High	5		5		5		ns
t_{RHZ}	$\overline{R}$ High to Data Bus at High Z[3]		15		20		20	ns
t_{WC}	Write Cycle Time	30		35		45		ns
t_{WPW}	Write Pulse Width[2]	20		25		35		ns
t_{WR}	Write Recovery Time	10		10		10		ns
t_{DS}	Data Setup Time	12		15		18		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{RHRS}	$\overline{R}$ High Before RS Low	0		0		0		ns
t_{WHRS}	$\overline{W}$ High Before RS Low	0		0		0		ns
t_{RSC}	Reset Cycle Time	30		35		45		ns
t_{RS}	Reset Pulse Width[2]	20		25		35		ns
t_{RSR}	Reset Recovery Time	10		10		10		ns
t_{RSFV}	Reset to Flag Output Valid (All Flags)		30		35		45	ns
t_{RTC}	Retransmit Cycle Time	30		35		45		ns
t_{RT}	Retransmit Pulse Width[2]	20		25		35		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		ns
t_{EFL}	Reset to Empty Flag Low		20		25		30	ns
$t_{HFH, FFH}$	Reser to Half & Full Flag High		20		25		30	ns
t_{REF}	Read Low to Empty Flag Low		20		25		30	ns
t_{RFF}	Read high to Full Flag High		20		25		30	ns
t_{WEF}	Write High to Empty Flag High		20		25		30	ns
t_{WFF}	Write Low to Full Flag Low		20		25		30	ns
t_{WHF}	Write Low to Half-Full Flag Low		30		35		45	ns
t_{RHF}	Read High to Half-Full Flag High		30		35		45	ns
t_{XOL}	Expansion Out Low Delay from Clock		20		25		35	ns
t_{XOH}[4]	Expansion Out High Delay from Clock		20		25		35	ns
t_{PXI}	$\overline{XI}$ Pulse Width	20		25		35		ns
t_{XIR}	$\overline{XI}$ Recovery Time	10		10		10		ns
t_{XIS}	$\overline{XI}$ Set-Up to Write or Clock	12		15		15		ns

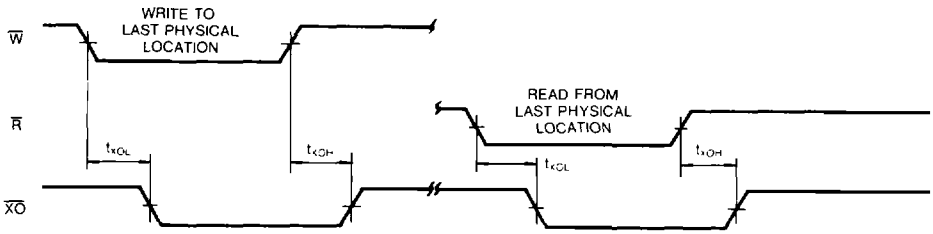
5

AC ELECTRICAL CHARACTERISTICS (Configured Mode)

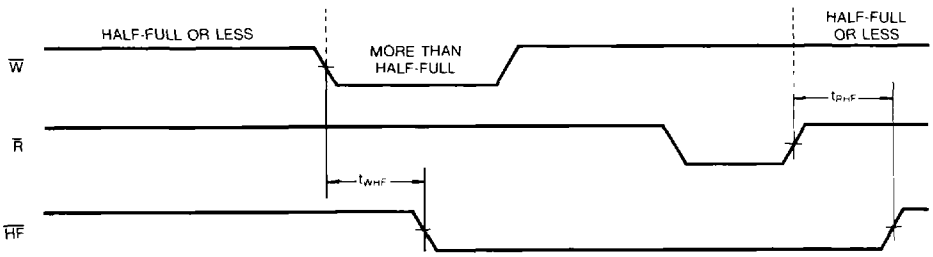
Symbol	Parameter	75C103A-20		75C103A-25		75C103A-35		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	30		35		45		ns
t_A	Access Time		20		25		35	ns
t_{RR}	Read Recovery Time	10		10		10		ns
t_{RPW}	Read Pulse Width[2]	20		25		35		ns
t_{DV}	Data Valid After $\overline{R}$ High	5		5		5		ns
t_{RHZ}	$\overline{R}$ High to Data Bus at High Z[3]		15		15		15	ns
t_{WC}	Write/Load Cycle Time	30		35		45		ns
t_{WPW}	Write/Load Pulse Width	20		25		35		ns
t_{WR}	Write/Load Recovery Time	10		10		10		ns
t_{DS}	Data Setup Time	12		15		18		ns
t_{RHRS}	$\overline{R}$ High Before $\overline{RS}$ Low	0		0		0		ns
t_{WHRS}	$\overline{W}$ High Before $\overline{RS}$ Low	0		0		0		ns
t_{RS}	Reset Pulse Width or Reset to $\overline{R}$ Low	20		25		35		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{RSC}	Reset Cycle Time(NO Register Programming)	30		35		45		ns
t_{RSPC}	Reset and Register Programming Cycle Time	100		115		145		ns
t_{RDV}	$\overline{R}$ Low to DIR Valid (Register Load Cycle)	5		5		5		ns
t_{RW}	$\overline{R}$ Low to Register Load	10		10		10		ns
t_{RSR}	Reset/Register programming Recovery Time	10		10		10		ns
t_{RTC}	Retransmit Cycle Time	30		35		45		ns
t_{RT}	Retransmit Pulse Width	20		25		35		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		ns
t_{RSFV}	Reset to Flag Output Valid (All flags)		15		15		15	ns
t_{REF}	Read Low to Empty Flag Low		20		25		30	ns
t_{RAEF}	Read Low to almost Empty Flag Low		30		35		45	ns
t_{RFF}	Read High to Full Flag High		20		25		30	ns
t_{RAFF}	Read High to Almost Full Flag High		30		35		45	ns
t_{WEF}	Write High to Empty Flag High		20		25		30	ns
t_{WAEF}	Write High to Almost Empty Flag High		30		35		45	ns
t_{WFF}	Write Low to Full Flag Low		20		25		30	ns
t_{WAFF}	Write Low to Almost Full Flag Low		30		35		45	ns
t_{WHF}	Write Low to Half-Full Flag Low		30		35		45	ns
t_{RHF}	Read High to Half-Full Flag High		30		35		45	ns
t_{XOL}	Expansion Out low Delay From Clock		20		25		35	ns
t_{XOH}[4]	Expansion Out High Delay From Clock		20		25		35	ns
t_{PXI}	$\overline{XI}$ Pulse Width	20		25		35		ns
t_{XIR}	$\overline{XI}$ Recovery Time	10		10		10		ns
t_{XIS}	$\overline{XI}$ Set-up to Write or Clock	12		15		15		ns

NOTES: 1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. t_{XOH} is guaranteed to be greater than or equal to t_{XOL} under all conditions.

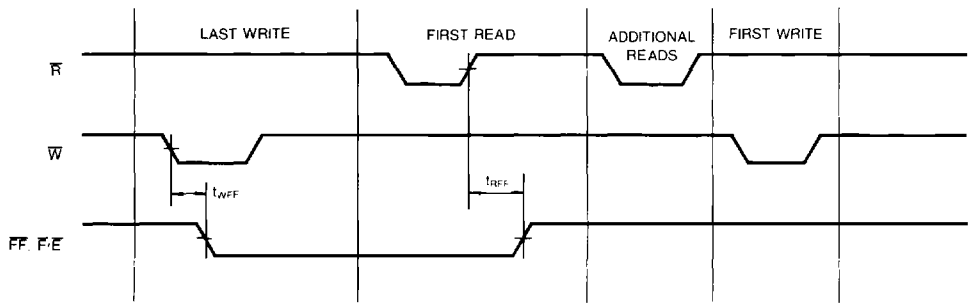
Expansion-Out Timing Diagram



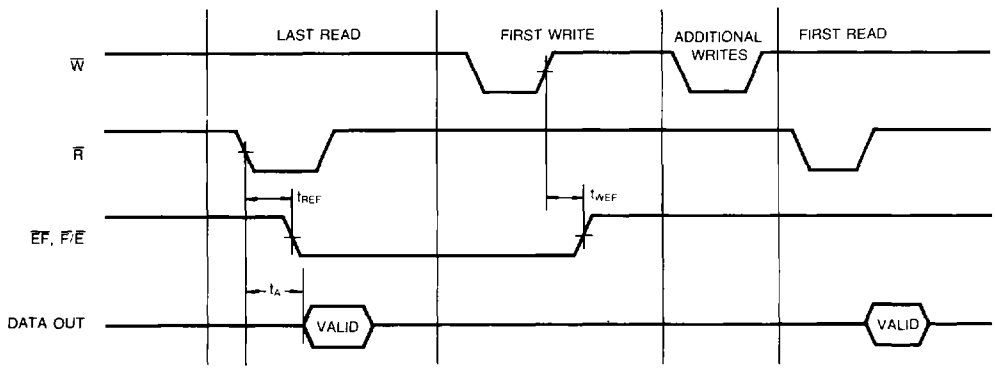
Half Full Flag Timing (Configured or nonconfigured mode)



Full Flag timing (Pin 8 or 20)

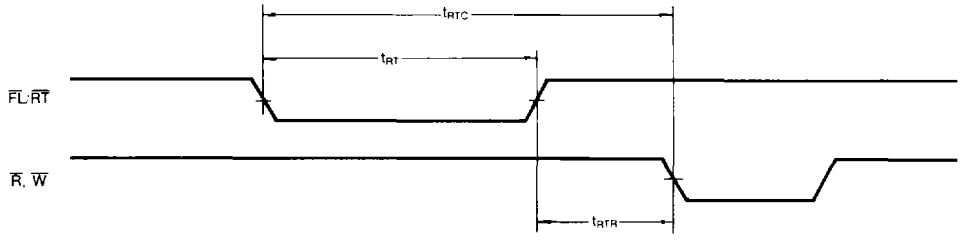


Empty Flag Timing (Pin 20 or 21)



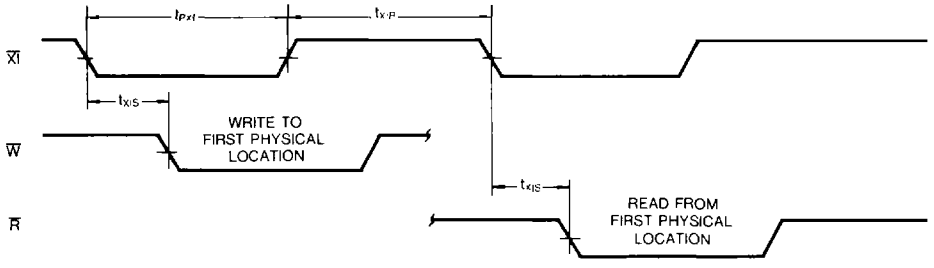
5

Retransmit

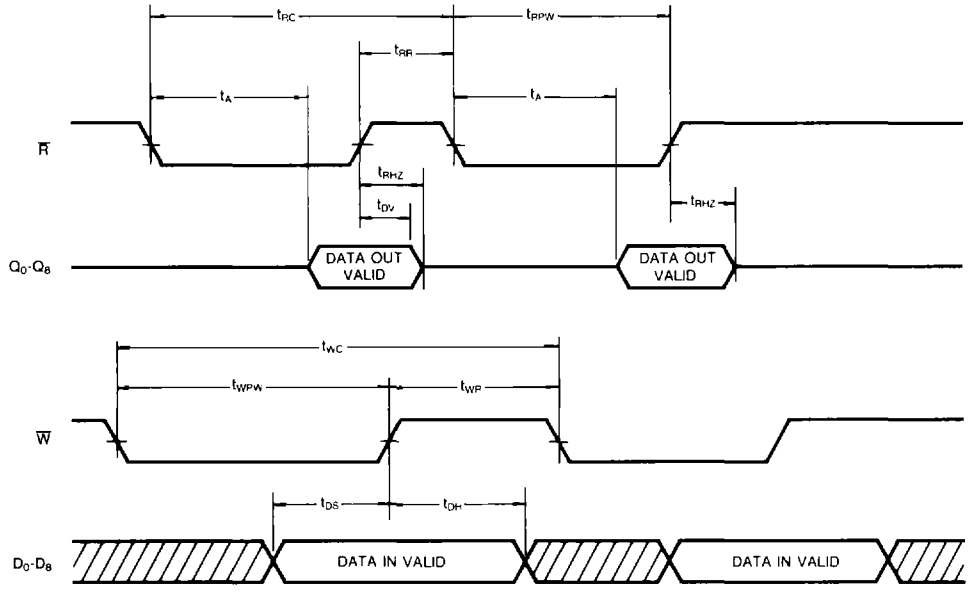


NOTES:
1. EF, HF, and FF may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

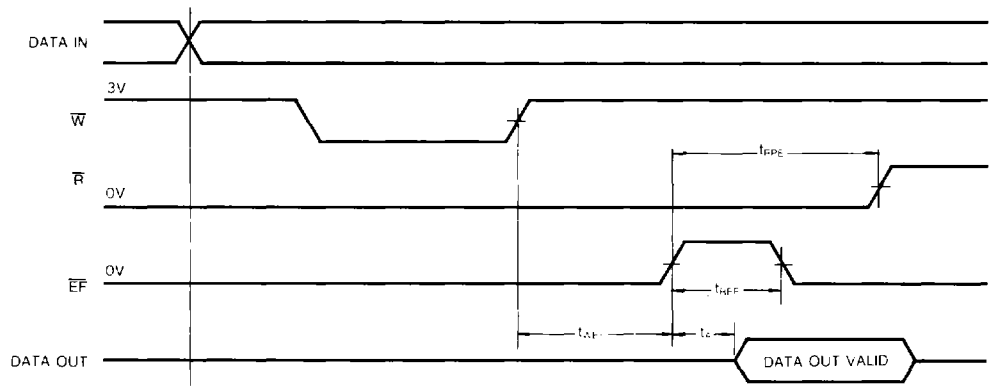
Expansion-In Timing Diagram



Asynchronous Write and Read Operation

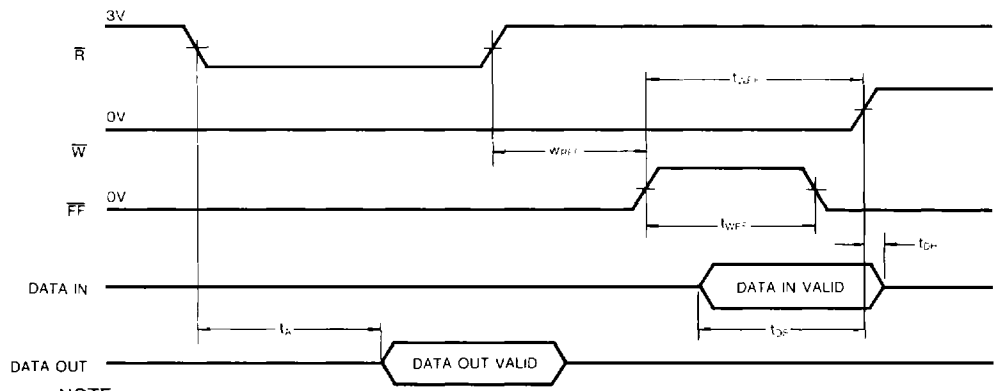


Read Data Flow Through Mode



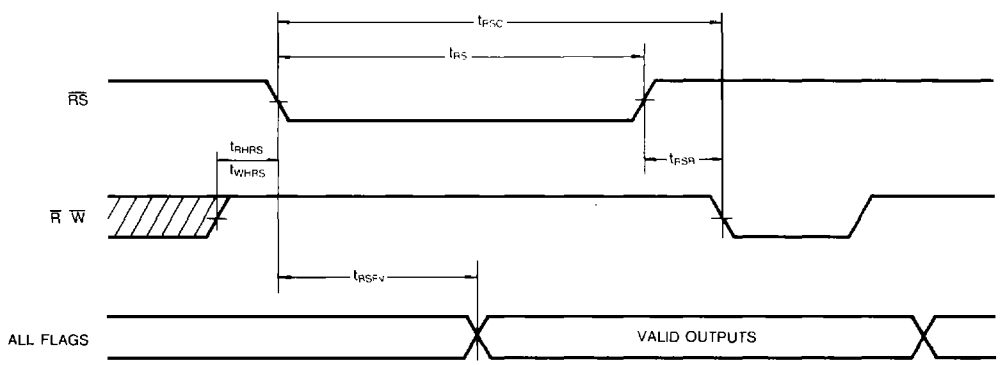
NOTE:
1. ($t_{RPE}=t_{RPW}$)

Write Data Flow Through Mode

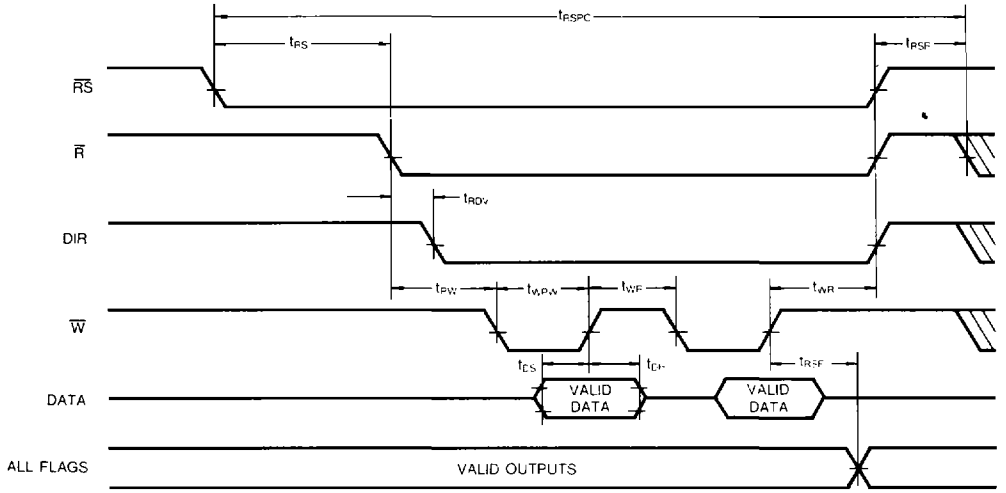


NOTE:
1. ($t_{WPF}=t_{WPW}$)

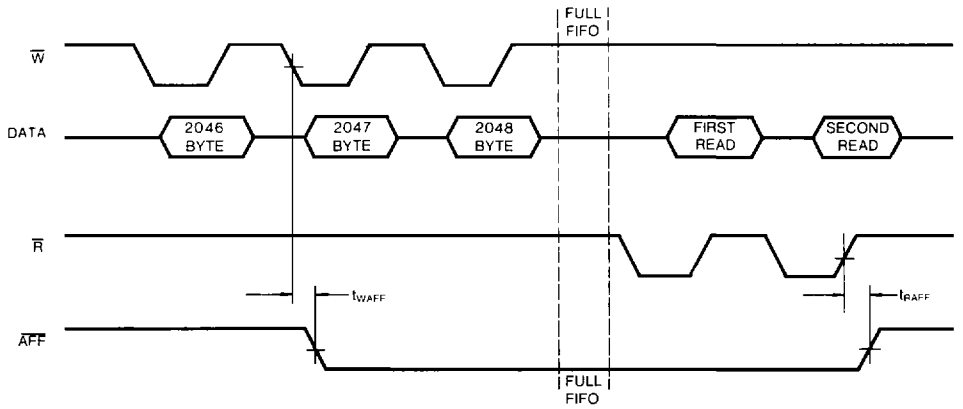
Device Reset Timing (No Register Programming)



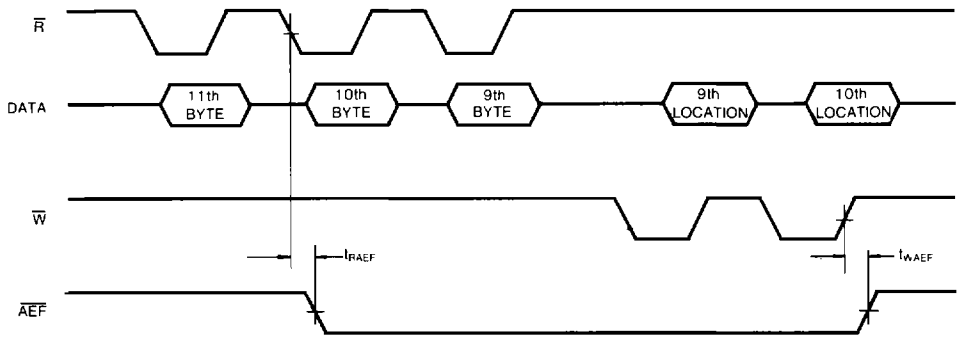
Reset/Register Programming Cycle Timing



Almost Full Flag Timing (2-Byte Offset)



Almost Empty Flag Timing (10-Byte Offset)



OPERATING MODES

The 75C103A has several modes of operation. These are:

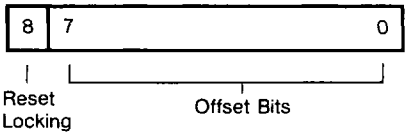
1. Device Reset Mode
The 75C103A can be reset by lowering the Reset ($\overline{RS}$) pin with both Read ($\overline{R}$) and Write ($\overline{W}$) inputs high. In this mode, all internal pointers and registers are cleared. A reset is required upon power up to insure correct device operation. After reset, all flags are set to appropriate states.

2. Register Load Mode
This mode of operation is used to reset the device and program the internal flag registers. This yields an Almost Full and an Almost Empty flag (pins 8 and 21 respectively) and a Half-Full or F/E flag.

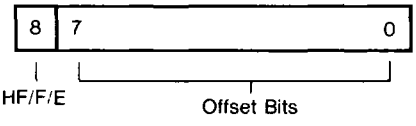
Two 9-bit internal registers have been provided for flag configuration. One is the Almost Full Flag Register (AFFR) and the other is the Almost Empty Flag Register (AEFR). Bit configurations of the two registers are shown below.

Register Set for KM75C103A

Almost Empty Flag Regiser (AEFR)



Almost Full Flag Register (AFFR)



Note that bits 0-7 are used for offset setting. The offset value ranges from 1 to 255 words. For each offset increment, a two byte offset is added in the FIFO providing 512 bytes of offset.

Bit 8 of the AFFR is used for configuration of pin 20 (28-pin DIP package). When this bit is set low, pin 20 is a $\overline{HF}$ Flag output. When it is set high, pin 20 is a $\overline{F/E}$ flag output.

The 8th bit of the AEFR is used for reset locking. When this bit is set low, subsequent device reset or register loading cycle resets the device. When the bit is programmed high, subsequent reset cycles are ignored. In this mode, the flag registers can be reconfigured without device reset. The part can be reset again by writing a 0 into this location followed by a device reset (or register loading) or by repowering up the device.

Flag registers are loaded by bringing $\overline{RS}$ low followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought low t_{RS} after the $\overline{RS}$ low. The registers can then be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first write loads the AFFR while the second write loads the AEFR. This loading order is fixed.

3. Array Read/Write Mode
Reading and writing into the FIFO is accomplished via Read ($\overline{R}$) and Write ($\overline{W}$) pins. The part can be written or read simultaneously through the input or the output ports respectively. The read cycle is initiated on the falling edge of the $\overline{R}$ input. After the rising edge of $\overline{R}$, the outputs will return to a high impedance state until the next read cycle. If the FIFO is empty, and read attempt is ignored (i.e. the read pointer stays intact and the outputs stay in three-state).

A write cycle is initiated by asserting the W input low. Data is stored in the memory sequentially, independent of any read operation in progress. When the FIFO is full, additional write attempts are ignored and thememory contents stay intact.

4. Retransmit Mode
Often it is necessary to retransmit data that was previously stored in the FIFO. Instead of reloading the FIFO, the retransmit feature can be used. When in single device mode ($\overline{XI}$ input low), a low on $\overline{FL}/\overline{RT}$/DIR input with $\overline{R}$ and $\overline{W}$ high resets the read pointer back to zero. The write pointer is unaffected. Then, the system can resend the same packet. This is beneficial in communication applications where transmission errors are more likely to occur.

5. Expansion Mode
The KM75C103A facilitates expansion in width and depth. The part can be configured for depth expansion by lowering pin 23 ($\overline{FL}/\overline{RT}$/DIR) for the first device in the daisy chain or by asserting it high if it is not the first device. The Expansion In ($\overline{XI}$) pin should be connected to Expansion Out ($\overline{XO}$) pin of the previous device. In this way, a signal can be passed to the next device when the current device is full. Note that the retransmit feature is not available in this mode.

OPERATING MODES (Continued)

The KM75C103A can be used for width expansion. Word width may be increased simply by connecting the corresponding input control signals of multiple devices. In this mode, the $\overline{XI}$ input must be grounded. Status Flags ($\overline{HF}$, $\overline{EF}$, $\overline{FF}$, $\overline{AFF}$ or $\overline{AEF}$) of any one of the devices can be used for system interrupt.

The two expansion techniques described above can be applied together to achieve deep FIFO with wide word width.

6. Bidirectional Mode

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two KM75C103A's. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Flag Timing

A total of 3 flag outputs are provided in either configured or non-configured mode. In the non-configured mode, the three flags are $\overline{HF}$ flag, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO is full. The flag goes inactive when the FIFO is half full or less.

The Full and Empty Flags go active when the last byte is written into or read out of the FIFO respectively. The flags are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO. All three flag outputs are active low.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a read/write cycle initiation of the location corresponding to the programmed offset value. For example if the AEFR register is programmed with a 10 byte offset (loading a Hex value of 05H), the $\overline{AEF}$ flag goes active during reading the 10th location before FIFO empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion and deassertion timing of the $\overline{AFF}$ is the same.

The third flag in the program mode is either $\overline{HF}$ or $\overline{F/E}$ flag depending on the state of the 9th bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in non-programmed mode. If the device is configured for $\overline{F/E}$ flag, it functions like $\overline{FF}$ or $\overline{EF}$ of the non configured mode. The pin goes active at the last FIFO read or FIFO write. The output is active low.

Data Flow-Through Modes

This section describes two special conditions when the FIFO is full, or when it is empty. For the read flow-through mode, the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in $(t_{WEF}+t_A)$ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ input is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ}ns. The $\overline{EF}$ will output a pulse showing temporary deassertion and then will be asserted. In the interval of time that $\overline{R}$ was low, additional data can be written into the FIFO (the subsequent writes after the first write edge would de-assert the empty flag); however, the same world (written on the first write edge) is presented to the output bus while $\overline{R}$ is still low. The read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, additional data is retrieved.

In the write flow-through mode, the FIFO permits the writing of a single byte of data immediately after reading one byte of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of new data. The new data is loaded into the FIFO on the rising edge of the $\overline{W}$ control pin. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted in order to write new data into the FIFO and to increment the write pointer.

Table 1. Reset and Retransmit—Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE:
1. Pointer will increment if flag is high.

Table 2. Reset and First Load Truth Table-Depth Expansion/Compound Expansion Mode

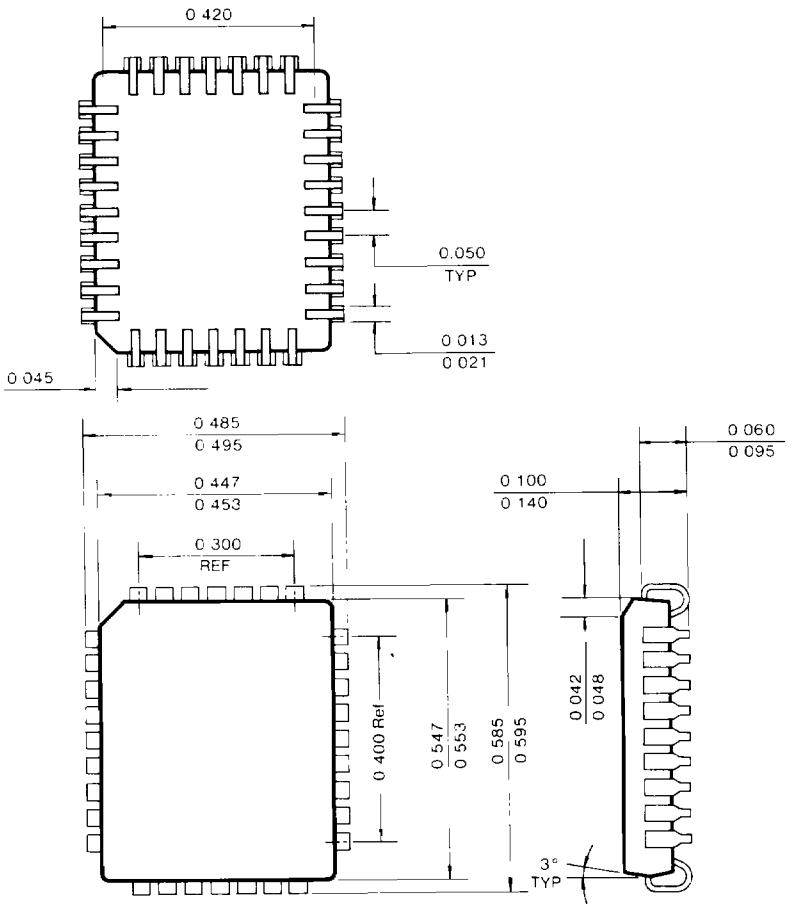
Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all other devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
$\overline{RS}$=Reset Input. $\overline{FL}$ $\overline{RT}$=First Load Retransmit. $\overline{EF}$=Emply Flag Output. $\overline{FF}$=Full Flag Output.
$\overline{XI}$=Expansion Input. $\overline{HF}$=Half-Full Flag Output.

PACKAGE DIMENSIONS

32-Pin Plastic Leaded Chip Charrier (PLCC)

Unit (inches)



5

PACKAGE DEMENSIONS (Continued)

28 Pin Plastic DIP

Unit (inches)