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LR40981A Pulse Dialer CMOS LSI

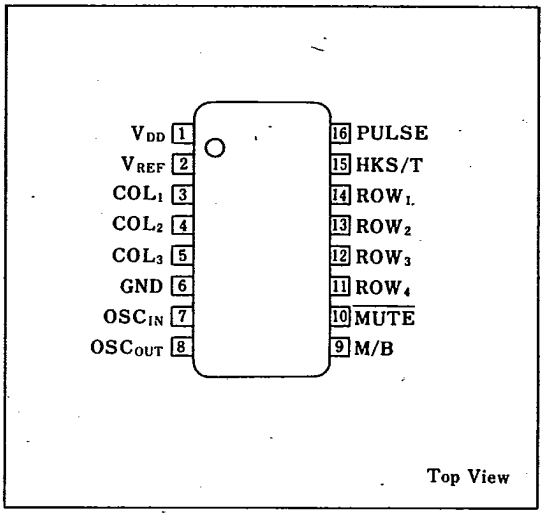
Description

The LR40981A is a CMOS LSI for pulse dialer with redial which integrates a ceramic resonator as a frequency reference.

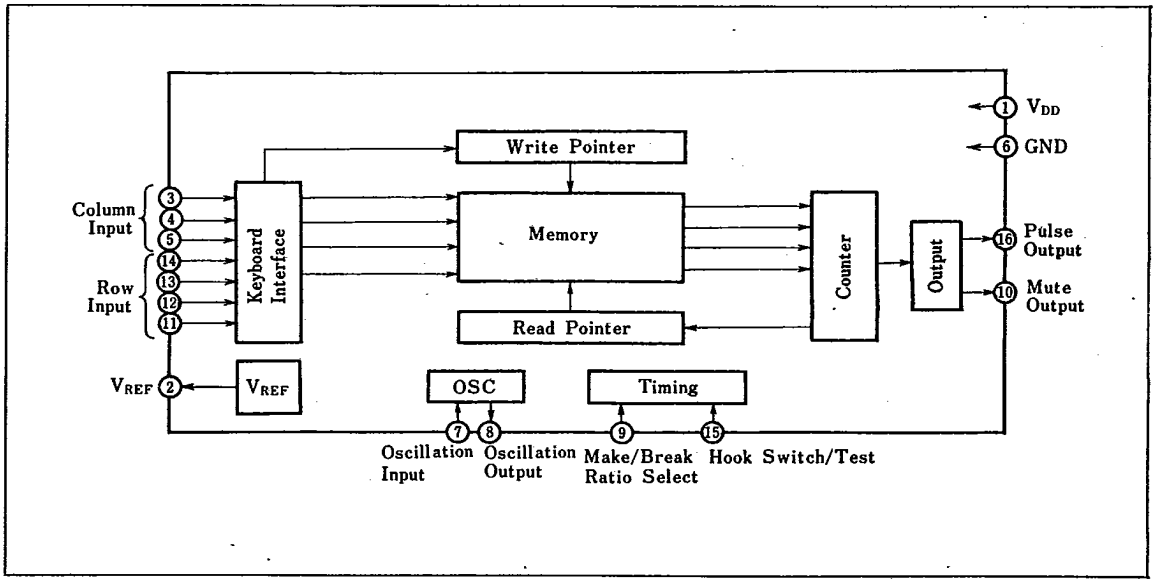
Features

1 Make ratio: 33/39% pin-selectable
2 Pulse output: "1" true
3 Mute output: "0" true
4 17-digit redial with either * or # input
5 Uses a ceramic oscillator as a frequency reference
6 Direct telephone line operation
7 Uses either a standard 2-of-7 matrix keyboard or a single contact keyboard
8 Mute signal generated on pulse signal
9 16-pin dual-in-line package

Pin Connections



Block Diagram



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■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{DD}	−0.3 to +6.2	V	1
Operating temperature	T_{opr}	−30 to +60	℃	
Storage temperature	T_{stg}	−55 to +150	℃	
Maximum power dissipation	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=25℃.
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Recommended Operating Conditions

Parameter	Symbol	Specified value	Unit
Supply voltage	V_{DD}	2.5 to 6.0	V

■ DC Characteristics

(Ta=−30 to +60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Key contact resistance	R_{KI}				1	kΩ	
Keyboard capacitance	C_{KI}				30	pF	
Input voltage	K_{IH}	2-of-7 input mode	$0.8V_{DD}$		V_{DD}	V	1
	K_{IL}		GND		$0.2V_{DD}$	V	1
Key pull-up resistance	K_{IRU}	V_{DD}=6.0V, V_{IN}=4.8V		4		kΩ	
Key pull-down resistance	K_{IRD}			100		kΩ	
$\overline{\text{MUTE}}$ sink current	I_M	V_{DD}=2.5V, V_{OUT}=0.5V	500			μA	2
Pulse output sink current	I_P	V_{DD}=2.5V, V_{OUT}=0.5V	1.0			mA	3
V_{DD}-V_{RFF} value	V_{REF}	I_{SUPPLY}=150 μA	1.5	2.5	3.5	V	4
Memory retention current	I_{MR}	All outputs in no-load state		0.7		μA	
Operating current	I_{OP}	All outputs in no-load state		100	150	μA	
$\overline{\text{MUTE}}$, PULSE leakage	I_{LKG}	V_{DD}=6.0V, V_{OUT}=6.0V		0.001	1	μA	2,3

Note 1 : Applies to key input pins (ROW_1-ROW_4, COL_1-COL_3).
Note 2 : Applies to $\overline{\text{MUTE}}$ output pin.
Note 3 : Applies to PULSE output pin.
Note 4 : Applies to V_{REF} pin.

■ AC Characteristics

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Notes
Oscillator frequency		f_{osc}		480		kHz	1
Keyboard debounce time		t_{DB}		10		ms	
Time for valid key entry		t_{KD}	40			ms	
Oscillator start-up time		t_{os}		6		ms	2
Pulse rate		P_R		10		pps	
Break Time	Pin 9 tied to V+	t_B		61		ms	
	Pin 9 tied to V−	t_B		67		ms	
Inter-digital pause		t_{IDP}		800		ms	

Note 1: Typical values are exact with a nominal 480 kHz frequency reference (except for oscillator start-up time).
Note 2: Ceramic resonator should have the following equivalent values: R<20Ω, RA≧70kΩ, C_O≦500pF.

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Functional Description

The LR40981A is a monolithic CMOS integrated circuit that converts keyboard inputs into pulse signal outputs which simulate a rotary telephone dial. It is designed to operate with a telephone line and can be interfaced so as to meet specifications of systems utilizing loop-disconnect signalling. Two outputs, one to pulse the telephone line and one to mute the receiver, are provided to implement the pulse dialer function. Accurate timing is accomplished by using a ceramic resonator as the frequency reference for the on-chip oscillator.

Keyboard logic is totally static so that the LR40981A will not introduce noise into the telephone system. Two outputs, one to pulse the telephone line and one to mute the receiver, are provided to implement the pulse dialer function.

When Off-Hook, the LR40981A senses a key down condition, verifies that only one key is depressed and then enters the key's code into an on-chip memory.

The FIFO (First In First Out) memory will store up to 17 digits, and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit starts a pre-digital pause counter and clears the memory buffer. At the end of the pre-digital pause, outpulsing begins. As digits are entered during the outpulsing period they will also be stored in the memory. Outpulsing will continue until all entered digits have been dialed. The first 17 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either # or *, provided that the receiver has been On-Hook for the minimum t_{OH} (refer to the AC Characteristics section).

When On-Hook, key inputs will not be recognized because the oscillator is disabled. This oscillator inhibit prevents the circuit from drawing excessive current when On-Hook.

An on-chip "Power-Up-Clear" circuit ensures reliable operation of the LR40981A. If the circuit power weakens, causing a possible loss of memory data integrity (see the electrical specifications), a "Power-Up-Clear" will occur when the proper supply level is restored. This function prevents "Redial" and the spontaneous outpulsing of incorrect data. A new number sequence may then be reentered in normal fashion.

Pin Functions

V_{DD} (Pin 1)

This is the positive supply input and is measured relative to GND (pin 6). The voltage on this pin must be regulated to less than 6 volts, using either the on-chip reference circuitry or an external form of regulation.

V_{REF} (Pin 2)

The V_{REF} output provides a reference voltage that tracks internal parameters of the LR40981A. V_{REF} provides a negative voltage reference to the V_{DD} supply. Its magnitude will be approximately 0.6 volts greater than the minimum operating voltage of each particular LR40981A.

The typical application would be to connect the V_{REF} pin to the GND pin (pin 6). The supply to the V_{DD} pin (pin 1) should then be regulated to 150 μA (I_{OP} max). With this amount of supply current, proper operation of the LR40981A is guaranteed.

The internal circuit of the V_{REF} function is shown in Figure 1 with its associated I-V characteristics.

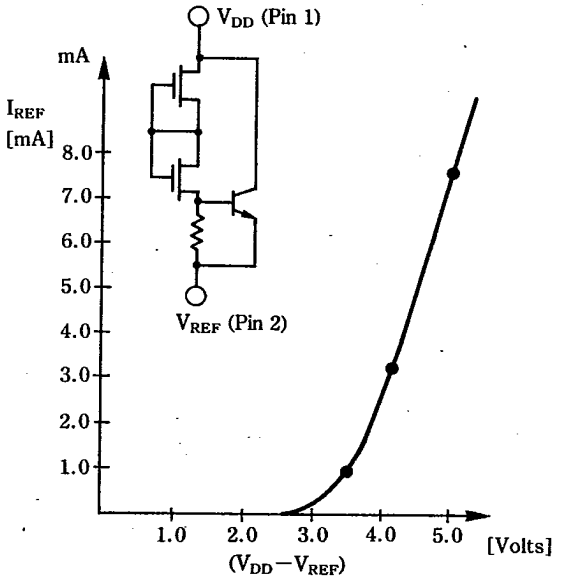


Fig. 1 V_{REF} typical I-V characteristics

Keyboard Inputs (Pins 3, 4, 5, 11, 12, 13, 14)

The LR40981A incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with positive true common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Figure 2.

A valid key entry is defined by either a single row being connected to a single column, or by V_{DD} being simultaneously presented to both a row and a column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted, thus preventing any accidental key contacts from causing excessive current flow.

When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the row and columns are alternately scanned (pulled high, then low) to verify that the input is valid. To be accepted, the input must remain valid continuously for 10ms of debounce time.

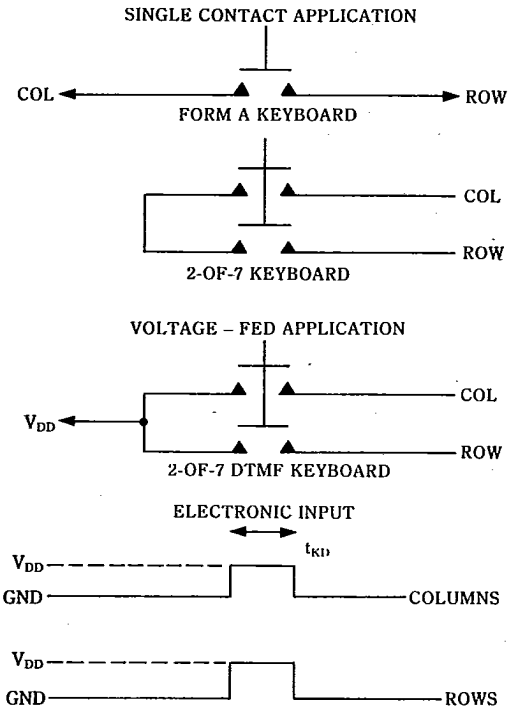


Fig. 2 Keyboard configuration

Oscillator (Pins 7 and 8)

The LR40981A contains an on-chip inverter with sufficient gain to provide oscillation when used with a low-cost 480kHz ceramic resonator (anti-resonant mode). In addition to the resonator, two external capacitors are required. Suggested equivalent values for the resonator are given in the AC Characteristics section. These values will insure proper oscillator operation in the specified voltage range. The LR40981A may be driven externally with a 480 kHz signal on pin 7.

GND (Pin 6)

This is the negative supply pin to which V_{REF} is normally tied (see V_{REF} paragraph).

Make/Break Select (Pin 9)

The Make/Break ratio may be selected by connecting pin 9 to either the V_{DD} or GND supply. Table 1 indicates the two popular ratios from which the user can choose.

Table 1 Make/Break ratio selection

Input to Make/Break Pin	Pulse Output	
	MAKE	BREAK
V_{DD} (Pin 1)	39%	61%
GND (Pin 6)	33%	67%

$\overline{\text{Mute}}$ Output (Pin 10)

The $\overline{\text{Mute}}$ output consists of an open-drain N-channel transistor. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. A typical method of interfacing this output pin is shown in the System Configuration diagram.

On-Hook/Test (Pin 15)

The "Test" or "On-Hook" input of the LR40981A has a pull-up to the positive supply. A V_{DD} input or allowing the pin to float puts the circuit into On-Hook or test mode, while a GND input puts it into Off-Hook or normal Mode. Any digits to be tested while in On-Hook/Test mode, however, must be entered while the circuit is Off-Hook.

When Off-Hook, the LR40981A will accept key inputs and outpulse the digits in normal fashion. When the last digit has been outpulsed, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the LR40981A to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 times the normal rate (the M/B ratio is then 50/50). This feature provides a means of

rapidly testing the device and is also an efficient way to reset the circuitry. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is de-activated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the DC Characteristics).

Upon returning to Off-Hook mode, a negative transistion on the Mute Output will insure that the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

Pulse Output (Pin 16)

The Pulse Output is an open-drain N-channel transistor designed to drive an external bipolar transistor. These transistors would normally be used to pulse the telephone line by controlling the loop current through the network.

Typical Application

The System Configuration schematic diagram shows one method which can be used to interface the pulse dialer with a telephone line. In the approach shown, the pulse dialer circuitry is in series with the speech network.

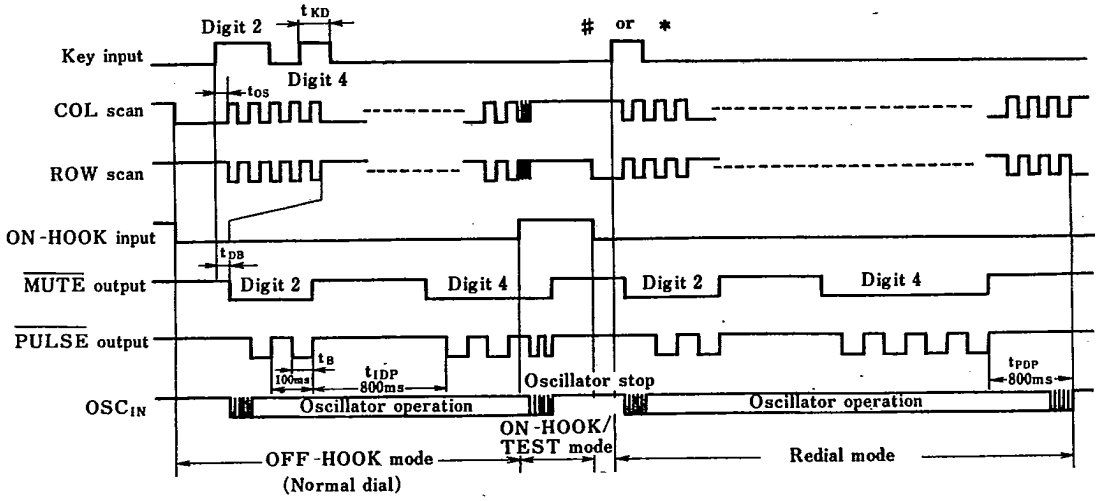
Some type of current source is needed that will provide a high impedance to the telephone line and deliver sufficient current to power the LR40981A (>150μA). The current source shown is constructed with two components, Q2 and R1. The current is regulated by the negative feedback provided by R1 to the gate of Q2. Several other implementations can be considered, such as a constant current diode or a configuration using bipolar transistors.

The purpose of transistor Q1 is to take the place of an additional hookswitch contact. When S1 closes, Q1 is turned on and HKS/T (Pin 15) is pulled to V_{DD}. This puts the LR40981A into normal mode so that it is ready to accept key inputs.

When going On-Hook, S1 is opened, causing Q1 to be turned off. An on-chip resistor pulls pin 15 to V_{DD} and the current source is disabled. The purpose of D1 is to limit any reverse current flow through the current source. A large-value resistor, R3, permits the small amount of current needed to maintain the LR40981A memory.

To return to Off-Hook mode, S1 is closed, causing Q1 to be turned on and the HKS/T pin to be tied to GND. The Pulse and Mute outputs drive external transistors to perform the outpulsing function. The receiver is connected through transistor Q6 to the speech network. Mute causes the transistor to be held on until outpulsing begins. When Mute goes low, the receiver is removed from the speech network. The pops caused by breaking the line are then isolated from the receiver. The Pulse output drives transistors Q3 and Q5 to make and break the line until the digit has been completely outpulsed. Mute then goes high again, returning the receiver to the speech network.

Timing Diagram



■ Test Circuit

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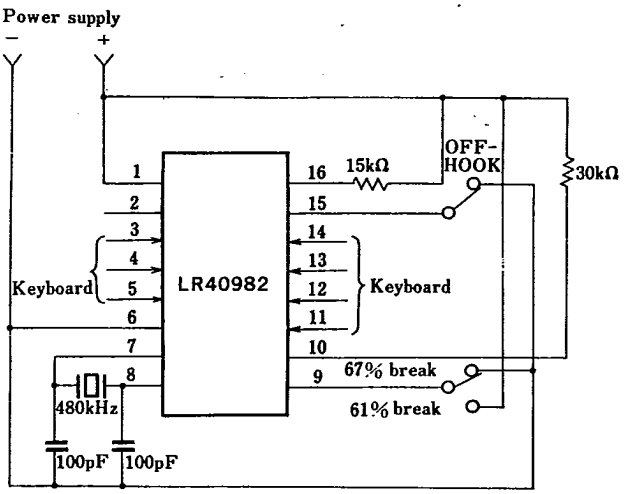
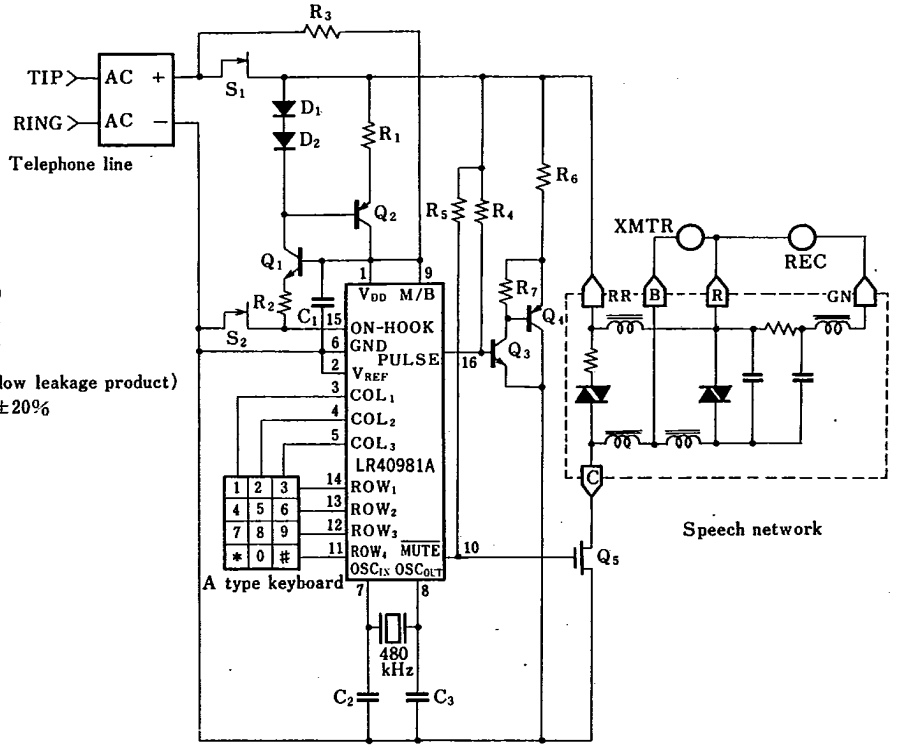


■ System Configuration Example



Q_1, Q_3 : 2N5550
Q_2, Q_4 : 2N5401
Q_5 : 2N6661
D_1, D_2 : 1N914
C_1 : 20μF (low leakage product)
C_2, C_3 : 100pF±20%
R_1 : 2.7kΩ
R_2 : 75kΩ
R_3 : 22MΩ
R_4 : 390kΩ
R_5 : 1MΩ
R_6 : 150Ω
R_7 : 100kΩ