TELEDYNE COMPONENTS

WIDEBAND, HIGH SLEW RATE OPERATIONAL AMPLIFIER

FEATURES

- **Low Cost**
- **Fast Settling ..... 0.1% in 200 ns typ.**
- **Slew Rate 120V/μsec**
- **Full Power Bandwidth ..... 1.6 MHz**
- **Open Loop Gain ..... 84 dB**
- **Gain Bandwidth Product ..... 20 MHz**

APPLICATIONS

- **High-Frequency Amplifiers**
- **Current-to-Voltage Converters**
- **Video Amplifiers**
- **Differential Amplifiers**
- **Line Drivers**
- **Wideband Precision**

GENERAL DESCRIPTION

The 1322 is a high-speed, fast-settling operational amplifier designed for a wide variety of high-speed signal processing tasks. Its fast, accurate settling performance (200 ns to 0.1% accuracy for a 10V step) and good DC specifications (84 dB open loop gain, 10 mV offset voltage) make the 1322 eminently suitable for high speed 8- and 10-bit data conversion applications. In addition, its high slew rate (120V/μs) serves it well in high-speed pulse circuits, signal generators, or other circuits where full output swings at signal frequencies as high as 1.6 MHz are required.

This device is internally compensated for stable operation in circuits operating at closed loop gains of 3 or above. For operation at lower closed loop gains, an external compensation capacitor is required from Pin 8 to ground (or the alternate stabilizing scheme shown in Figure 1 may be used).

The standard 1322 is housed in a small outline, metal TO-99 case and is specified for 0°C to +75°C operation.

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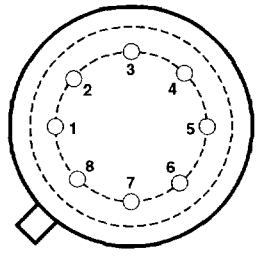
PIN CONFIGURATION

Pin No.	Designation
1	OFFSET ADJUST
2	-IN
3	+IN
4	$-V_{CC}$
5	OFFSET ADJUST
6	OUTPUT
7	$+V_{CC}$
8	BANDWIDTH CONTROL



BOTTOM VIEW

1322

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage ..... ±20V
V_{IDF} Differential Input Voltage ..... ±15V
T_C Operating Temperature Range (Case)
1322 ..... 0°C to +75°C
T_{STG} Storage Temperature Range ..... –65°C to +150°C

ELECTRICAL CHARACTERISTICS: T_C = +25°C, $\pm V_{CC}$ = ±15V, R_L = 2 kΩ unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
I_b	Input Bias Current		—	±125	±250	nA
		T_{MIN} to T_{MAX}	—	—	±500	nA
IOS	Input Offset Current		—	±20	±50	nA
		T_{MIN} to T_{MAX}	—	—	±100	nA
VOS	Input Offset Voltage	Without external trim	—	±5	±10	mV
VOS TC	VOS vs Temperature		—	±30	—	µV/°C
PSRR	Input Offset vs Power Supply		—	90	—	dB
V_{ICM}	Common Mode	For DC linear operation	±10	—	—	V
CMRR	Common Mode Rejection Ratio	@ DC	—	90	—	dB
Z_{ID}	Differential Input Impedance	@ DC	40	100	—	MΩ
Output						
VO	Voltage		±10	±12	—	V
IO	Current		±10	±20	—	mA
Voltage Gain						
AOL	Open Loop Voltage Gain	@ DC	77	84	—	dB
ACL	Closed Loop Gain	Stable operation w/o compensation	10	—	—	dB
Frequency Response						
GBWP	Gain Bandwidth Product	ACL = 10, f = 10 kHz	10	20	—	MHz
FPBW	Full Power Bandwidth	ACL ≥ 3, C_C = 0	1.2	1.6	—	MHz
Time Response						
ts	Settling Time	10V step to 0.1%	—	200	—	ns
sr	Slew Rate	ACL = 3, C_C = 0	±80	±120	—	V/µs
Noise (Referenced to Input)						
en	Wideband (10 Hz to 1 kHz)		—	1	—	μV_{RMS}
Power Supplies						
V_{CC}	Power Supply Voltage		—	±15	±20	V
I_{CC}	Quiescent Supply Current	V_{CC} = ±15V	—	±4	±6	mA

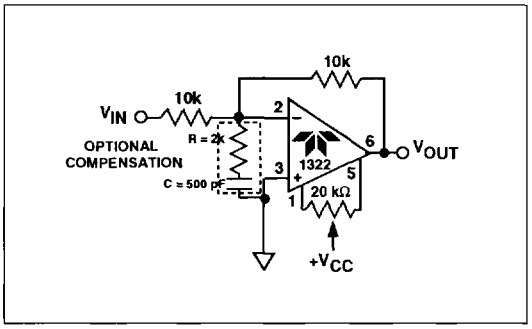


Figure 1. Optional Stabilizing Scheme
(for unity gain stability at high speed)

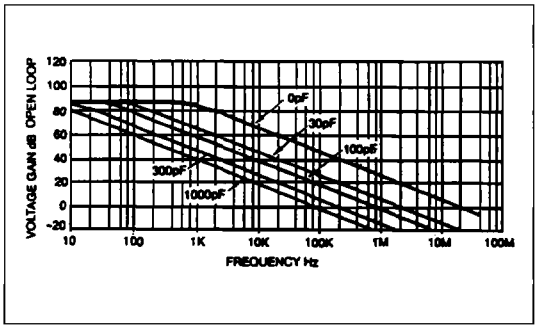


Figure 2. Bode Plot

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