128Mb E-die DDR SDRAM Specification

Revision 1.0

SAMSUNG ELECTRONICS

128Mb E-die Revision History

Revision 1.0 (December, 2002)

- First release

Key Features

- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Four banks operation
- Differential clock inputs(CK and $\overline{CK}$)
- DLL aligns DQ and DQS transition with CK transition
- MRS cycle with address key programs
  - -. Read latency 2, 2.5 (clock)
  - -. Burst length (2, 4, 8)
  - -. Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK)
- Data I/O transactions on both edges of data strobe
- Edge aligned data output, center aligned data input
- LDM,UDM for write masking only (x16)
- DM for write masking only (x4, x8)
- Auto & Self refresh
- 15.6us refresh interval(4K/64ms refresh)
- Maximum burst refresh cycle : 8
- 66pin TSOP II package

Ordering Information

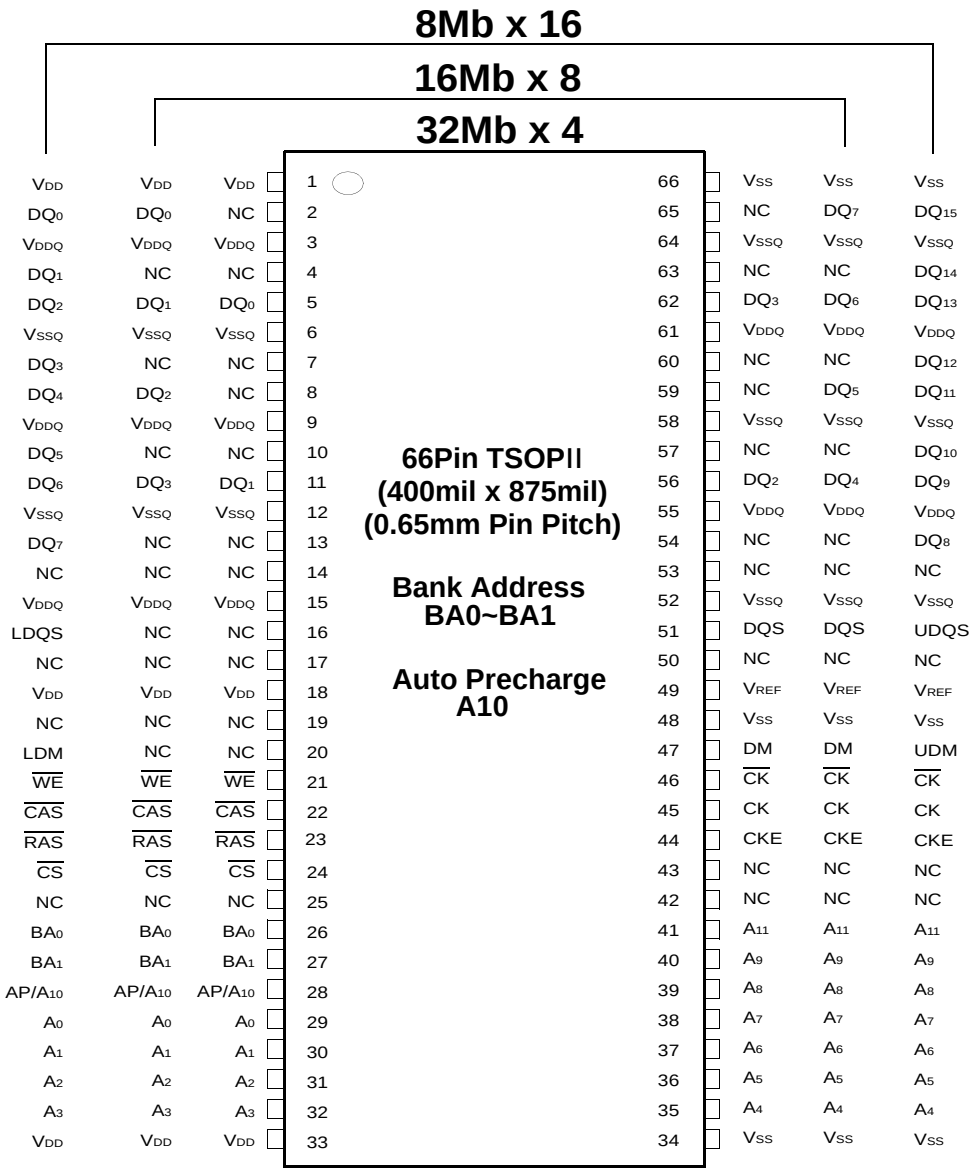
Part No.	Org.	Max Freq.	Interface	Package
K4H280438E-TC/LB3	32M x 4	B3(DDR333@CL=2.5)	SSTL2	66pin TSOP II
K4H280438E-TC/LA2		A2(DDR266@CL=2)		
K4H280438E-TC/LB0		B0(DDR266@CL=2.5)		
K4H280438E-TC/LA0		A0(DDR200@CL=2)		
K4H280838E-TC/LB3	16M x 8	B3(DDR333@CL=2.5)	SSTL2	66pin TSOP II
K4H280838E-TC/LA2		A2(DDR266@CL=2)		
K4H280838E-TC/LB0		B0(DDR266@CL=2.5)		
K4H280838E-TC/LA0		A0(DDR200@CL=2)		
K4H281638E-TC/LB3	8M x 16	B3(DDR333@CL=2.5)	SSTL2	66pin TSOP II
K4H281638E-TC/LA2		A2(DDR266@CL=2)		
K4H281638E-TC/LB0		B0(DDR266@CL=2.5)		
K4H281638E-TC/LA0		A0(DDR200@CL=2)		

Operating Frequencies

	- B3(DDR333@CL=2.5)	- A2(DDR266@CL=2)	- B0(DDR266@CL=2.5)	- A0(DDR200@CL=2)
Speed @CL2	133MHz	133MHz	100MHz	100MHz
Speed @CL2.5	166MHz	133MHz	133MHz	-

*CL : CAS Latency

Pin Description



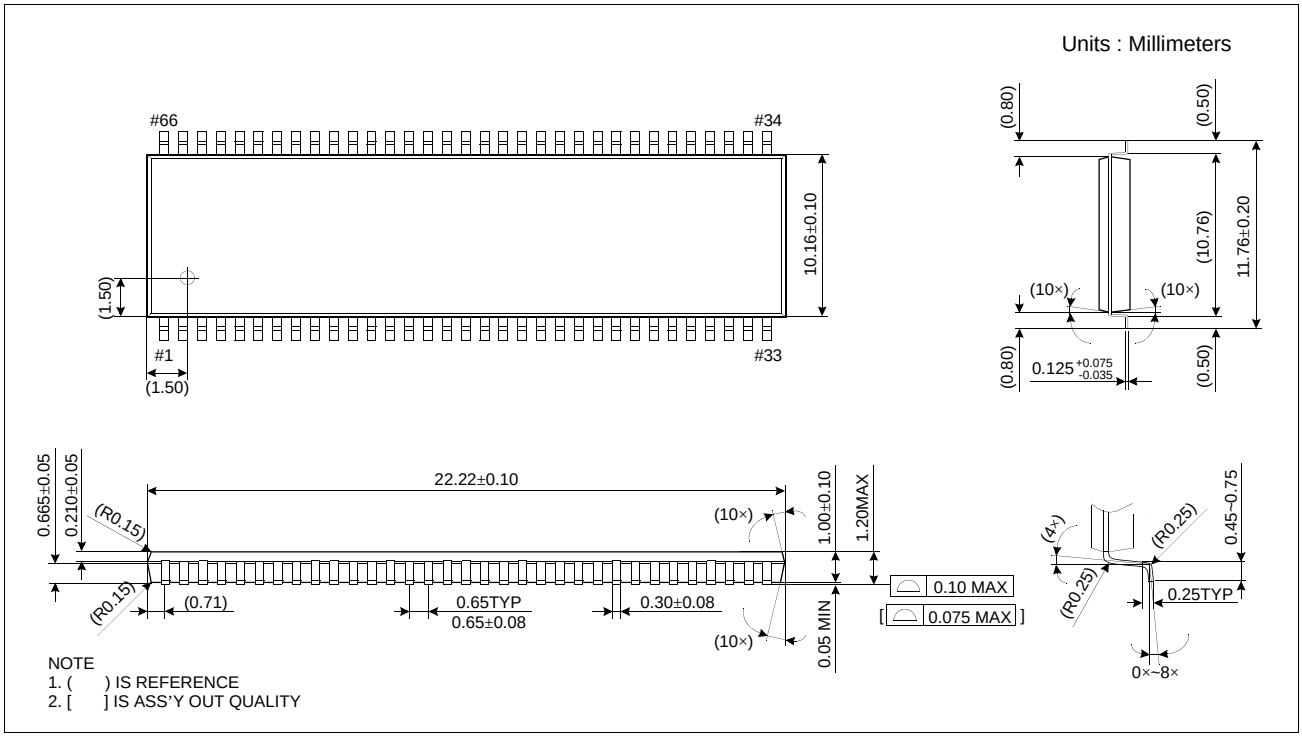
128Mb Package Pinout

Organization	Row Address	Column Address
32Mx4	A0~A11	A0-A9, A11
16Mx8	A0~A11	A0-A9
8Mx16	A0~A11	A0-A8

DM is internally loaded to match DQ and DQS identically.

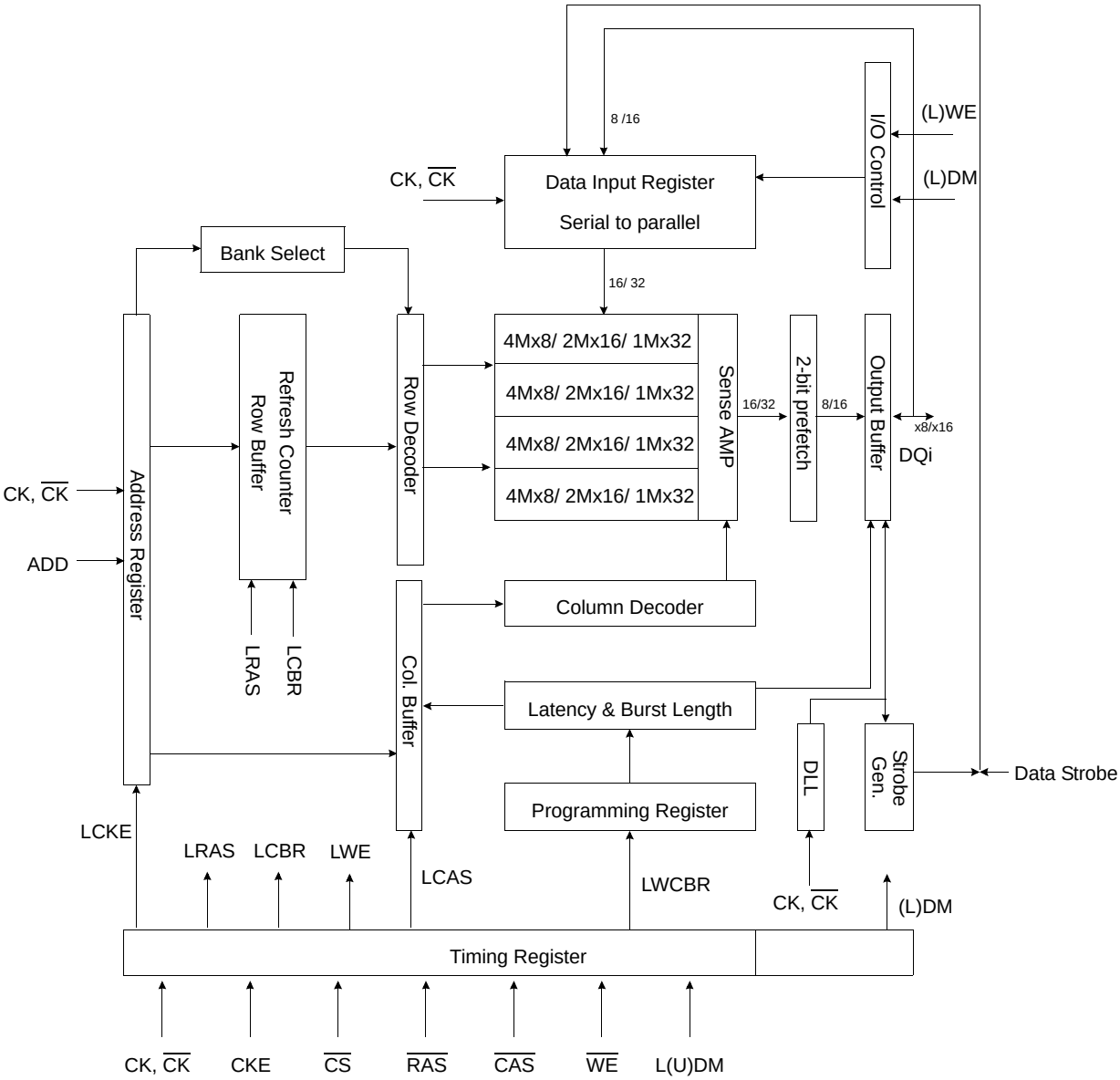
Row & Column address configuration

Package Physical Demension



66pin TSOPII / Package dimension

Block Diagram (8Mbx4 / 4Mbx8 / 2Mbx16 I/O x 4 Banks)



Input/Output Function Description

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock : CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/$\overline{CK}$.
CKE	Input	Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognize an LVCMOS LOW level prior to VREF being stable on power-up.
$\overline{CS}$	Input	Chip Select : $\overline{CS}$ enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
LDM,(UDM)	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0~D7 ; UDM corresponds to the data on DQ8~DQ15. DM may be driven high, low, or floating during READs.
BA0, BA1	Input	Bank Addres Inputs : BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [0 : 11]	Input	Address Inputs : Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS). A12 & A13 are used on device densities of 256Mb and greater, and A13 is used only on 1Gb decices.
DQ	I/O	Data Input/Output : Data bus
LDQS,(U)DQS	I/O	Data Strobe : Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0~D7 ; UDQS corresponds to the data on DQ8~DQ15
NC	-	No Connect : No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply : +2.5V ± 0.2V.
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply : +2.5V ± 0.2V (device specific).
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A0 ~ A9, A11	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM(UDM/LDM for x16 only)			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

Note : 1. OP Code : Operand Code. A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@EMRS/MRS)

2. EMRS/MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM(x4/8) sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
   UDM/LDM(x16 only) sampled at the rising and falling edges of the UDQS/LDQS and Data-in are masked at the both edges (Write UDM/LDM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

8M x 4Bit x 4 Banks / 4M x 8Bit x 4 Banks / 2M x 16Bit x 4 Banks Double Data Rate SDRAM

General Description

The K4H280438E / K4H280838E / K4H281638E is 134,217,728 bits of double data rate synchronous DRAM organized as 4x 8,388,608 / 4x 4,194,304 / 4x 2,097,152 words by 4/ 8/16bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 333Mb/s per pin. I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.5	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7		
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	0.49*VDDQ	0.51*VDDQ	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(DC)	0.36	V_{DDQ}+0.6	V	3
V-I Matching: Pullup to Pulldown Current Ratio	VI(Ratio)	0.71	1.4	-	4
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} - 0.45V	I_{OL}	9		mA	

Note : 1.VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on VREF may not exceed +/-2% of the dc value.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1/7 for device drain to source voltages from 0.1 to 1.0.

DDR SDRAM Spec Items & Test Conditions

Conditions	Symbol
Operating current - One bank Active-Precharge; tRC=tRCmin; tCK=10ns for DDR200, 7.5ns for DDR266, 6ns for DDR333; DQ,DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	**IDD0**
Operating current - One bank operation ; One bank open, BL=4, Reads - Refer to the following page for detailed test condition	**IDD1**
Percharge power-down standby current; All banks idle; power - down mode; CKE = <VIL(max); tCK=10ns for DDR200,7.5ns for DDR266, 6ns for DDR333; Vin = Vref for DQ,DQS and DM.	**IDD2P**
Precharge Floating standby current; CS# > =VIH(min);All banks idle; CKE > = VIH(min); tCK=10ns for DDR200, 7.5ns for DDR266, 6ns for DDR333; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ,DQS and DM	**IDD2F**
Precharge Quiet standby current; CS# > = VIH(min); All banks idle; CKE > = VIH(min); tCK=10ns for DDR200, 7.5ns for DDR266, 6ns for DDR333; Address and other control inputs stable at >= VIH(min) or =<VIL(max); Vin = Vref for DQ ,DQS and DM	**IDD2Q**
Active power - down standby current ; one bank active; power-down mode; CKE=< VIL (max); tCK=10ns for DDR200, 7.5ns for DDR266, 6ns for DDR333; Vin = Vref for DQ,DQS and DM	**IDD3P**
Active standby current; CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; tCK=10ns for DDR200, 7.5ns for DDR266, 6ns for DDR333; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	**IDD3N**
Operating current - burst read; Burst length = 2; reads; continguous burst; One bank active; address and control inputs changing once per clock cycle; CL=2 at tCK=10ns for DDR200, CL=2 at 7.5ns for DDR266(A2), CL=2.5 at 7.5ns for DDR266(B0), 6ns for DDR333; 50% of data changing on every transfer; lout = 0 m A	**IDD4R**
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL=2 at tCK= 10ns for DDR200, CL=2 at tCK=7.5ns for DDR266(A2), CL=2.5 at tCK=7.5ns for DDR266(B0), 6ns for DDR333; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	**IDD4W**
Auto refresh current; tRC = tRFC(min) - 8*tCK for DDR200 at tCK=10ns; 10*tCK for DDR266 at tCK=7.5ns; 12*tCK for DDR333 at tCK=6ns; distributed refresh	**IDD5**
Self refresh current; CKE =< 0.2V; External clock on; tCK = 10ns for DDR200, tCK=7.5ns for DDR266, 6ns for DDR333.	**IDD6**
Orerating current - Four bank operation ; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	**IDD7A**

Input/Output Capacitance

(V_{DD}=2.5, V_{DDQ}=2.5V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Delta	Unit	Note
Input capacitance (A0 ~ A11, BA0 ~ BA1, CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	CIN1	2	3	0.5	pF	4
Input capacitance(CK, $\overline{CK}$)	CIN2	2	3	0.25	pF	4
Data & DQS input/output capacitance	COUT	4	5	0.5	pF	1,2,3,4
Input capacitance(DM for x4/8, UDM/LDM for x16)	CIN3	4	5		pF	1,2,3,4

Note : 1.These values are guaranteed by design and are tested on a sample basis only.
2. Although DM is an input -only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS, and DM in the system.
3. Unused pins are tied to ground.
4. This parameteer is sampled. VDDQ = +2.5V +0.2V, VDD = +3.3V +0.3V or +2.5V+0.2V, f=100MHz, tA=25°C, Vout(dc) = VDDQ/2, Vout(peak to peak) = 0.2V. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).

DDR SDRAM I_{DD} spec table

(V_{DD}=2.7V, T = 10°C)

Symbol		32Mx4 (K4H280438E)			Unit	Notes
		B3(DDR333@CL=2.5)	A2(DDR266@CL=2.0) B0(DDR266@CL=2.5)	A0(DDR200@CL=2.0)		
IDD0		80	75	70	mA	
IDD1		105	95	90	mA	
IDD2P		3	3	3	mA	
IDD2F		20	18	16	mA	
IDD2Q		15	14	13	mA	
IDD3P		22	20	18	mA	
IDD3N		40	35	32	mA	
IDD4R		120	105	100	mA	
IDD4W		140	120	100	mA	
IDD5		160	150	140	mA	
IDD6	Normal	2	2	2	mA	
	Low power	1	1	1	mA	Optional
IDD7A		280	240	210	mA	

Symbol		16Mx8 (K4H280838E)			Unit	Notes
		B3(DDR333@CL=2.5)	A2(DDR266@CL=2.0) B0(DDR266@CL=2.5)	A0(DDR200@CL=2.0)		
IDD0		85	75	70	mA	
IDD1		110	100	95	mA	
IDD2P		3	3	3	mA	
IDD2F		22	20	18	mA	
IDD2Q		16	15	14	mA	
IDD3P		22	20	20	mA	
IDD3N		40	35	32	mA	
IDD4R		140	120	105	mA	
IDD4W		145	125	100	mA	
IDD5		165	155	145	mA	
IDD6	Normal	2	2	2	mA	
	Low power	1	1	1	mA	Optional
IDD7A		300	250	220	mA	

Symbol		8Mx16 (K4H281638E)			Unit	Notes
		B3(DDR333@CL=2.5)	A2(DDR266@CL=2.0) B0(DDR266@CL=2.5)	A0(DDR200@CL=2.0)		
IDD0		TBD	TBD	TBD	mA	
IDD1		TBD	TBD	TBD	mA	
IDD2P		TBD	TBD	TBD	mA	
IDD2F		TBD	TBD	TBD	mA	
IDD2Q		TBD	TBD	TBD	mA	
IDD3P		TBD	TBD	TBD	mA	
IDD3N		TBD	TBD	TBD	mA	
IDD4R		TBD	TBD	TBD	mA	
IDD4W		TBD	TBD	TBD	mA	
IDD5		TBD	TBD	TBD	mA	
IDD6	Normal	TBD	TBD	TBD	mA	
	Low power	TBD	TBD	TBD	mA	Optional
IDD7A		TBD	TBD	TBD	mA	

< Detailed test conditions for DDR SDRAM IDD1 & IDD7A >

IDD1 : Operating current: One bank operation

1. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA
2. Timing patterns
 - A0 (100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRCD = 2*tCK, tRAS = 5*tCK
   Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing
   *50% of data changing at every burst
 - B0 (133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
   Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
   *50% of data changing at every burst
 - A2 (133Mhz, CL=2) : tCK = 7.5ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
   Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
   *50% of data changing at every burst
 - B3(166Mhz,CL=2.5) : tCK=6ns, CL=2.5, BL=4, tRCD=10*tCK, tRAS=7*tCK
   Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
   *50% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

IDD7A : Operating current: Four bank operation

1. Typical Case : Vdd = 2.5V, T=25' C
2. Worst Case : Vdd = 2.7V, T= 10' C
3. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA
4. Timing patterns
 - A0 (100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRRD = 2*tCK, tRCD= 3*tCK, Read with autoprecharge
   Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing
   *100% of data changing at every burst

 - B0 (133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK
   Read with autoprecharge
   Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
   *100% of data changing at every burst

 - A2 (133Mhz, CL=2) : tCK = 7.5ns, CL2=2, BL=4, tRRD = 2*tCK, tRCD = 3*tCK,Read with autoprecharge
   Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
   *100% of data changing at every burst

 - B3(166Mhz,CL=2.5) : tCK=6ns, CL=2.5, BL=4, tRRD=2*tCK, tRCD=3*tCK,Read with autoprecharge
   Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
   *100% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

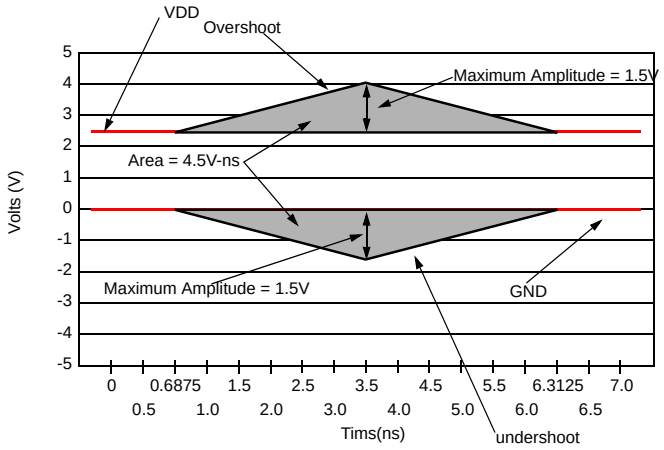
AC Operating Conditions

Parameter/Condition	Symbol	Min	Max-10	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Notes :
1. VID is the magnitude of the difference between the input level on CK and the input level on /CK.
2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.

AC Overshoot/Undershoot specification for Address and Control Pins

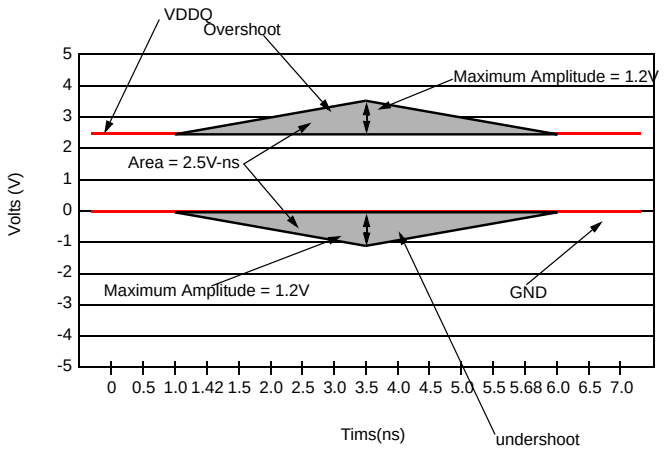
Parameter	Specification	
	DDR333	DDR200/266
Maximum peak amplitude allowed for overshoot	TBD	1.5 V
Maximum peak amplitude allowed for undershoot	TBD	1.5 V
The area between the overshoot signal and VDD must be less than or equal to	TBD	4.5 V-ns
The area between the undershoot signal and GND must be less than or equal to	TBD	4.5 V-ns



AC overshoot/Undershoot Definition

Overshoot/Undershoot specification for Data, Strobe, and Mask Pins

Parameter	Specification	
	DDR333	DDR200/266
Maximum peak amplitude allowed for overshoot	TBD	1.2 V
Maximum peak amplitude allowed for undershoot	TBD	1.2 V
The area between the overshoot signal and VDD must be less than or equal to	TBD	2.4 V-ns
The area between the undershoot signal and GND must be less than or equal to	TBD	2.4 V-ns



DQ/DM/DQS AC overshoot/Undershoot Definition

AC Timming Parameters & Specifications

Parameter		Symbol	B3 (DDR333@CL=2.5		A2 (DDR266@CL=2.0		B0 (DDR266@CL=2.5		A0 (DDR200@CL=2.0		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
Row cycle time		tRC	60		65		65		70		ns	
Refresh row cycle time		tRFC	72		75		75		80		ns	
Row active time		tRAS	42	70K	45	120K	45	120K	48	120K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	18		20		20		20		ns	
Row precharge time		tRP	18		20		20		20		ns	
Row active to Row active delay		tRRD	12		15		15		15		ns	
Write recovery time		tWR	15		15		15		15		ns	
Last data in to Read command		tWTR	1		1		1		1		tCK	
Col. address to Col. address delay		tCCD	1		1		1		1		tCK	
Clock cycle time	CL=2.0	tCK	7.5	12	7.5	12	10	12	10	12	ns	
	CL=2.5		6	12	7.5	12	7.5	12			ns	
Clock high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.45	-	0.5	-	0.5	-	0.6	ns	12
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		0		0		ns	3
DQS-in hold time		tWPRE	0.25		0.25		0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		0.35		0.35		tCK	
DQS-in cycle time		tDSC	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time(fast)		tIS	0.75		0.9		0.9		1.1		ns	i,5.7~9
Address and Control Input hold time(fast)		tIH	0.75		0.9		0.9		1.1		ns	i,5.7~9
Address and Control Input setup time(slow)		tIS	0.8		1.0		1.0		1.1		ns	i, 6~9
Address and Control Input hold time(slow)		tIH	0.8		1.0		1.0		1.1		ns	i, 6~9
Data-out high impedence time from CK/$\overline{CK}$		tHZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	1
Data-out low impedence time from CK/$\overline{CK}$		tLZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	1
Input Slew Rate(for input only pins)		tSL(I)	0.5		0.5		0.5		0.5		V/ns	
Input Slew Rate(for I/O pins)		tSL(IO)	0.5		0.5		0.5		0.5		V/ns	
Output Slew Rate(x4,x8)		tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	
Output Slew Rate Matching Ratio(rise to		tSLMR	0.67	1.5	0.67	1.5	0.67	1.5	0.67	1.5		

Parameter	Symbol	B3 (DDR333@CL=2.5))		A2 (DDR266@CL=2.0)		B0 (DDR266@CL=2.5))		A0 (DDR200@CL=2.0)		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	12		15		15		16		ns	
DQ & DM setup time to DQS	tDS	0.45		0.5		0.5		0.6		ns	j, k
DQ & DM hold time to DQS	tDH	0.45		0.5		0.5		0.6		ns	j, k
Control & Address input pulse width	tIPW	2.2		2.2		2.2		2.5		ns	8
DQ & DM input pulse width	tDIPW	1.75		1.75		1.75		2		ns	8
Power down exit time	tPDEX	6		7.5		7.5		10		ns	
Exit self refresh to non-Read command	tXSNR	75		75		75		80		ns	
Exit self refresh to read command	tXSRD	200		200		200		200		tCK	
Refresh interval time	tREFI	15.6		15.6		15.6		15.6		us	4
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	11
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	10, 11
Data hold skew factor	tQHS		0.55		0.75		0.75		0.8	ns	11
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	2
Active to Read with Auto precharge command	tRAP	18		20		20		20			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/ tCK) + (tRP/tCK)		tCK	13

System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR333, DDR266 & DDR200 devices to ensure proper system performance. these characteristics are for system simulation purposes and are guaranteed by design.

Table 1 : Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS		DDR333		DDR266		DDR200			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	TBD	TBD	TBD	TBD	0.5	4.0	V/ns	a, m

Table 2 : Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	tIS	tIH	UNITS	NOTES
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate

Input Slew Rate	tDS	tDH	UNITS	NOTES
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	tDS	tDH	UNITS	NOTES
+/- 0.0 V/ns	0	0	ps	j
+/- 0.25 V/ns	+50	+50	ps	j
+/- 0.5 V/ns	+100	+100	ps	j

Table 5 : Output Slew Rate Characteristice (X4, X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	NOTES
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	1.0	4.5	b,c,d,f,g,h

Table 6 : Output Slew Rate Characteristice (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	NOTES
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	0.7	5.0	b,c,d,f,g,h

Table 7 : Output Slew Rate Matching Ratio Characteristics

AC CHARACTERISTICS	DDR266A		DDR266B		DDR200		
PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	NOTES
Output Slew Rate Matching Ration (Pullup to Pulldown)	TBD	TBD	TBD	TBD	0.67	1.5	e,m

Component Notes

1. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. these parameters are not referenced to a specific voltage level but specify when the device output in no longer driving (HZ), or begins driving (LZ).

2. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but sys tem performance (bus turnaround) will degrade accordingly.

3. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previ ously in progress on the bus, DQS will be tran sitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.

4. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.

5. For command/address input slew rate $\geq$ 1.0 V/ns

6. For command/address input slew rate $\geq$ 0.5 V/ns and $<$ 1.0 V/ns

7. For CK & $\overline{CK}$ slew rate $\geq$ 1.0 V/ns

8. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

9. Slew Rate is measured between VOH(ac) and VOL(ac).

10. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

11. tQH = tHP - tQHS, where:
    tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one tansition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

12. tDQSQ
    Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

13. tDAL = (tWR/tCK) + (tRP/tCK)
    For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR266B at CL=2.5 and tCK=7.5ns tDAL = (15 ns / 7.5 ns) + (20 ns/ 7.5ns) = (2) + (3)
    tDAL = 5 clocks

System Notes :

a. Pullup slew rate is characteristized under the test conditions as shown in Figure 1.

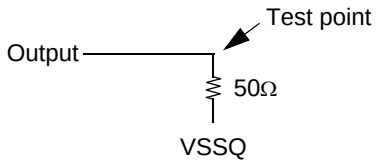


Figure 1 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 2.

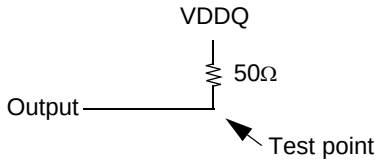


Figure 2 : Pulldown slew rate test load

c. Pullup slew rate is measured between (VDDQ/2 - 320 mV +/- 250 mV)
Pulldown slew rate is measured between (VDDQ/2 + 320 mV +/- 250 mV)
Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.
Example : For typical slew rate, DQ0 is switching
For minmum slew rate, all DQ bits are switching from either high to low, or low to high.
The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions
Typical : 25 °C (T Ambient), VDDQ = 2.5V, typical process
Minimum : 70 °C (T Ambient), VDDQ = 2.3V, slow - slow process
Maximum : 0 °C (T Ambient), VDDQ = 2.7V, fast - fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOPII package divces only.

h. Only intended for operation up to 266 Mbps per pin.

i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns as shown in Table 2. The Input slew rate is based on the lesser of the slew rates detemined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
The delta rise/fall rate is calculated as:
{1/(Slew Rate1)} - {1/(Slew Rate2)}

For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

k. Table 3 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser on the lesser of the AC ~ AC slew rate and the DC- DC slew rate. The inut slew rate is based on the lesser of the slew rates deter mined by either VIH(ac) to VIL(ac) or VIH(DC) to VIL(DC), and similarly for rising transitions.

m. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transi tions through the DC region must be monotonic.