M5M27C512AK-15I

524288-BIT (65536-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M27C512AK-15I is a high-speed 524288-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C512AK-15I is fabricated by N-channel double polisilicon gate and CMOS technology for peripheral circuits, and is available in a 28-pin DIP with a transparent lid.

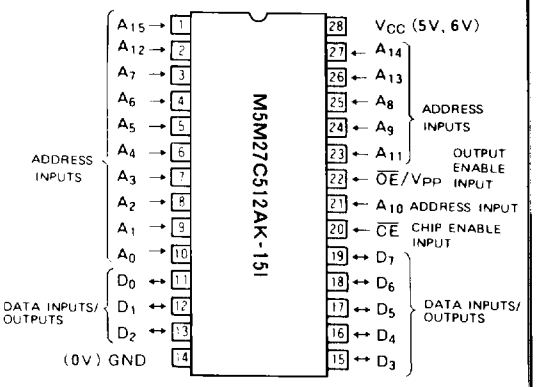
FEATURES

- 65536 Word x 8 bit organization
- Access time M5M27C512AK-15I . . . 150 ns (max)
- Programming voltage: 12.5V
- Two line control $\overline{OE}$, $\overline{CE}$
- Lower power current (I_{CC}): Active . . . 50 mA (max)
  Stand-by . . . 1 mA (max)
- Single 5V power supply (read operation)
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP
- Fast programming algorithm
- Wide temperature range: −40°C ~ +85°C

APPLICATION

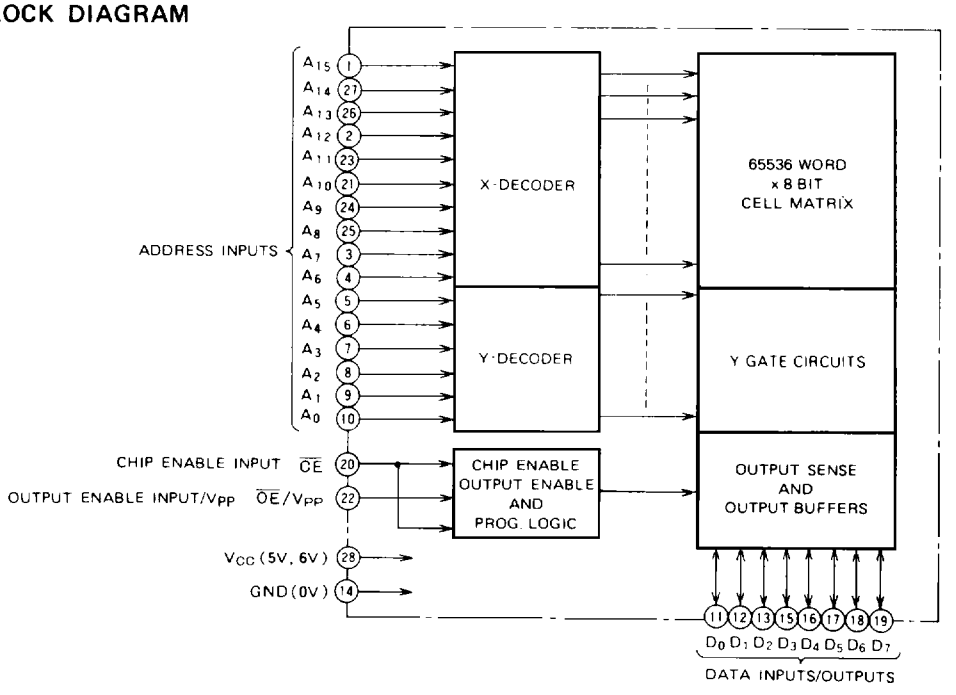
Microcomputer systems and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 28K4

BLOCK DIAGRAM



524288-BIT (65536-WORD BY 8-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}/V_{PP}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}/V_{PP}$ and address signals to the address inputs ($A_0 \sim A_{15}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}/V_{PP}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signals is high, the device is in the standby mode or power-down mode.

Programming

(Fast programming algorithm)

First set V_{CC} = 6V, $\overline{OE}/V_{PP}$ = 12.5V and then set an address to first address to be programmed. After applying 1ms program pulse ($\overline{CE}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1ms program pulse. The programmer continues 1ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1ms pulses applied to that address in register X. And then applied a program pulse 3 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of appoximately 15WS/cm^2. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	Outputs (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	5 V	Data out
Output disable	V_{IL}	V_{IH}	5 V	Floating
Stand by	V_{IH}	X*	5 V	Floating
Program	V_{IL}	12.5V	6 V	Data in
Program inhibit	V_{IH}	12.5V	6 V	Floating

*: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Ratings	Unit
T_{opr}	Operating temperature	−50 ~ 95	°C
T_{stg}	Storage temperature	−65 ~ 125	°C
V_{I1}	All input or output voltage (Note 2)	−0.6 ~ 7.0	V
V_{I2}	$\overline{OE}/V_{PP}$ supply voltage (Note 2)	−0.6 ~ 14.0	V
V_{I3}	A9 input voltage (Note 2)	−0.6 ~ 13.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

MITSUBISHI ELECTRIC

READ OPERATION

DC ELECTRICAL CHARACTERISTICS ($Ta = -40 \sim 85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$V_{IN} = 0 \sim V_{CC}$			10	μA
I_{LO}	Output leakage current	$V_{OUT} = 0 \sim V_{CC}$			10	μA
I_{SB1}	V_{CC} current stand-by	$\overline{CE} = V_{IH}$			1	mA
I_{SB2}		$\overline{CE} = V_{CC}$		1	100	μA
I_{CC1}	V_{CC} current active	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$, DC, $I_{OUT} = 0mA$			50	mA
I_{CC2}		$\overline{CE} = V_{IL}$, f=6.7MHz, $I_{OUT} = 0mA$			50	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V

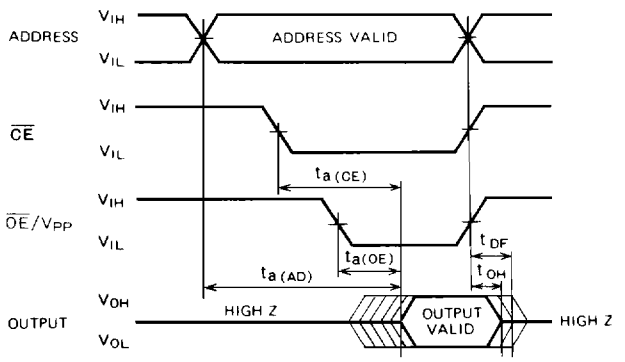
Note 3: Typical values are at Ta = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS ($Ta = -40 \sim 85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		150	ns
$t_{a(CE)}$	$\overline{CE}$ to output delay	$\overline{OE}/V_{PP} = V_{IL}$		150	ns
$t_{a(OE)}$	$\overline{OE}$ to output delay	$\overline{CE} = V_{IL}$		60	ns
t_{DF}	$\overline{OE}$ high to output float	$\overline{CE} = V_{IL}$	0	50	ns
t_{OH}	Output hold from $\overline{CE}$, $\overline{OE}$ or address	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$	0		ns

Note 4: V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$

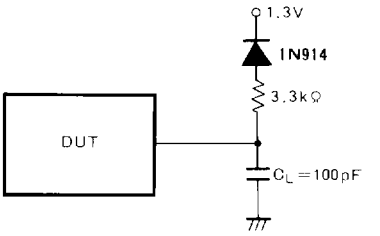
AC WAVEFORMS



Test conditions for A.C characteristics
Input voltage: $V_{IL} = 0.45V$, $V_{IH} = 2.4V$
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: 1.5V

Output load: 1TTL gate + C_L (100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance	Ta = 25°C, f = 1MHz, $V_I = V_O = 0V$		4	6	pF
C_{OUT}	Output capacitance			8	12	pF
$C_{\overline{OE}/V_{PP}}$	$\overline{OE}/V_{PP}$ input capacitance			25	30	pF

PROGRAM OPERATION

FAST PROGRAMMING ALGORITHM

DC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$, unless otherwise noted)

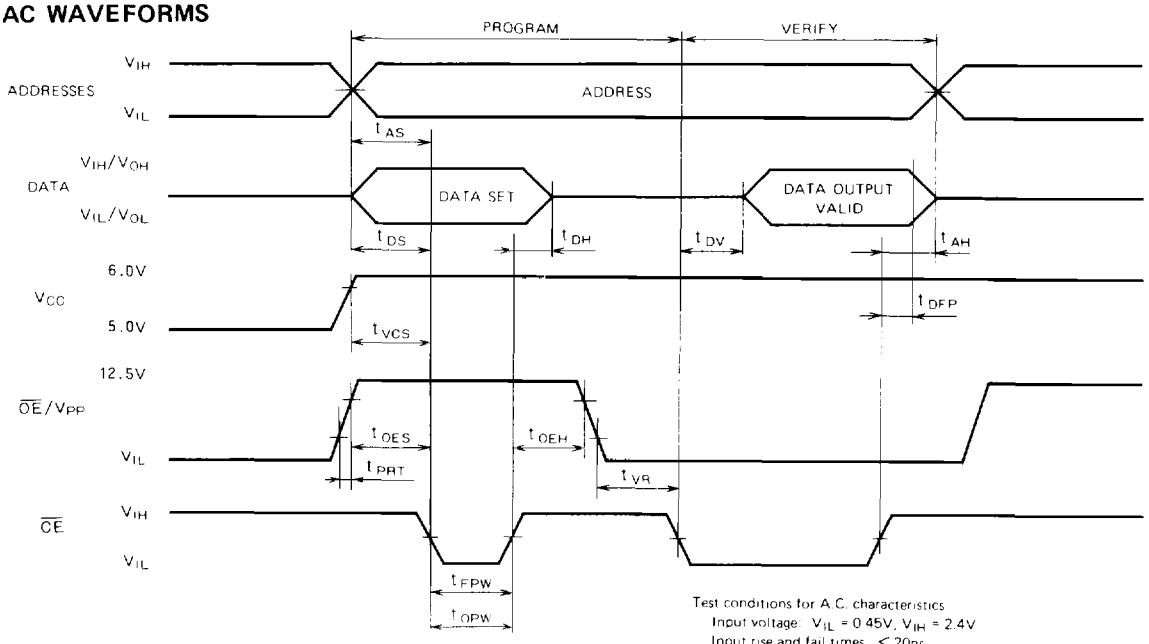
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$V_{IN} = 0 \sim V_{CC}$			10	μA
V_{OL}	Output low voltage (verify)	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	Output high voltage (verify)	$I_{OH} = -400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC2}	V_{CC} supply current				50	mA
I_{PP2}	$\overline{OE}/V_{PP}$ supply current	$\overline{CE} = V_{IL}$			50	mA

AC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}/V_{PP}$ setup time		2			μs
t_{OEH}	$\overline{OE}/V_{PP}$ hold time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	$\overline{CE}$ to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{FPW}	$\overline{CE}$ initial program pulse width		0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ over program pulse width		2.85		78.75	ms
t_{DV}	Data valid from $\overline{CE}$				1	μs
t_{VR}	$\overline{OE}/V_{PP}$ recovery time		2			μs
t_{PRT}	$\overline{OE}/V_{PP}$ pulse rise time during program		50			ns

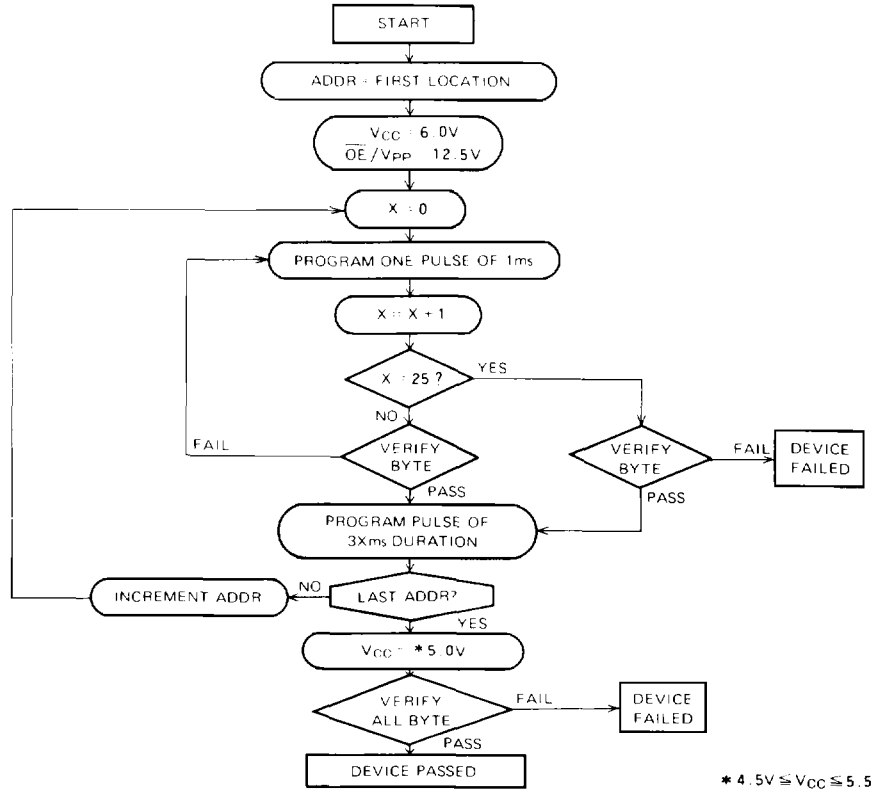
Note 5 V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$

FAST PROGRAMMING AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times ≦ 20ns
Reference voltage at timing measurement : 1.5V

FAST PROGRAMMING ALGORITHM FLOW CHART



* 4.5V ≦ V_{CC} ≦ 5.5V

DEVICE IDENTIFIER MODE

The Device Identifier Mode allows the reading of a binary code from the EPROM that identifies the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

M5M27C512AK-15I DEVICE IDENTIFIER CODE

Pin / Code	A_0 (10)	D_7 (19)	D_6 (18)	D_5 (17)	D_4 (16)	D_3 (15)	D_2 (13)	D_1 (12)	D_0 (11)	Hex data
Manufacturer code	V_{IH}	0	0	0	1	1	1	0	0	1C
Device code	V_{IL}	0	0	0	0	0	1	1	1	07

Note 6. $V_{CC}=5V\pm10\%$, $A_9=12.0\pm0.5V$, $A_1\sim A_8$, $A_{10}\sim A_{15}$, $\overline{CE}$, $\overline{OE}/V_{PP}=V_{IL}$