MC145415

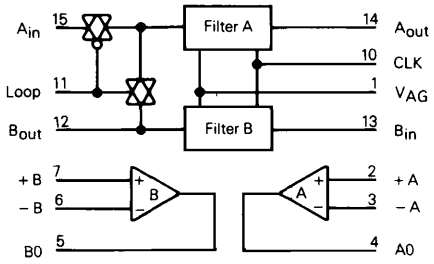
Advance Information

DUAL TUNABLE LINEAR PHASE LOW-PASS SAMPLED DATA FILTERS

The MC145415 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two uncommitted comparators for use elsewhere in the system.

- Two Linear Phase 5th Order Low-Pass Filters
- Low Operating Power Consumption — 20 mW (Typical)
- ±2.5 to ±8 Volt Power Supply Ranges
- CMOS Compatible Inputs Using V_{DG} Pin
- Two Comparators Available to Reduce Component Count
- Useful in High Speed Data Modem Applications
- Pass-Band Edges Tunable With Clock Frequency from 1.25 kHz to 10 kHz

BLOCK DIAGRAM

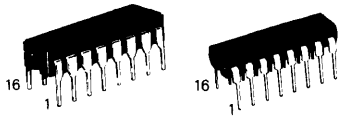


V_{DG} = Pin 9
V_{DD} = Pin 16
V_{SS} = Pin 8

This document contains information on a new product. Specifications and information herein are subject to change without notice.

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

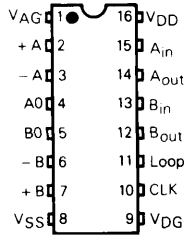
DUAL TUNABLE
LINEAR PHASE LOW-PASS
SAMPLED DATA FILTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



ORDERING INFORMATION

MC14XXXX
- L Ceramic Package
- P Plastic Package

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MAXIMUM RATINGS (V_{SS} = 0)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	4.5	5	16	V
Clock Frequency*	CLK	50	128	400	kHz

*Filter frequency response may degrade slightly as clock frequency is increased above 200 kHz.

DIGITAL ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{SS} = 0 V, V_{AG} = V_{DD}/2, T_A = −40 to 85°C)

Characteristic	Symbol	Min	Max	Unit
Operating Current	I_{DD}	–	4	mA
Input Capacitance	C_{in}	–	10	pF
Input Low Voltage (Pins 10, 11)	V_{IL}	–	V_{DG} + 0.3 (V_{DD} − V_{DG})	V
Input High Voltage (Pins 10, 11)	V_{IH}	V_{DD} − 0.3 (V_{DD} − V_{DG})	–	V
Input Leakage Current (Pins 10, 11)	I_{IL}	–	2.5	μA
V_{DG} Reference Voltage (Pin 9)	V_{DG}	V_{SS}	V_{DD} − 4.5	V

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V, V_{SS} = 0, V_{AG} = V_{DD}/2, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	A_{in}, B_{in}	I_{in}	–	±0.00001	±10	μA
Input Current	V_{AG}	I_{in}	–	±0.00001	±50	μA
AC Input Impedance (1 kHz)	A_{in}, B_{in}	Z_{in}	–	2	–	MΩ
Input Common Mode Voltage Range	A_{in}, B_{in}, +A, −A, +B, −B	V_{ICR}	2.0	–	10.0	V
Input Offset Current	+A to −A, +B to −B	I_{ID}	–	±10	–	nA
Input Bias Current	+A, −A, +B, −B	I_{IB}	–	±0.10	±1.0	nA
Input Offset Voltage	+A to −A, +B to −B	V_{ID}	–	±10	±70	mV
Output Voltage Range	A_{out}, B_{out}	V_{OR}				V
(R_L = 20 kΩ to V_{AG}, R_B = ∞)			1.5	–	10.5	
(R_L = 900 Ω to V_{AG}, R_B = 1.8 kΩ to V_{DD})			2.5	–	9.0	
(R_L = 600 Ω to V_{AG}, R_B = 1.6 kΩ to V_{DD})			3.0	–	8.3	
Small Signal Output Impedance (1 kHz)	A_{out}	Z_o	–	50	–	Ω
	B_{out}		–	50	–	
Output Current						
(V_O = 10.5 V)	A_{out}, B_{out}	I_{OH}	−200	−400	–	μA
(V_O = 1.5 V)	A_{out}, B_{out}	I_{OL}	5	7.5	–	mA
Comparator Output Current	A0, B0					
(V_O = 9.5 V)		I_{OH}	−1.1	−2.25	–	mA
(V_O = 0.5 V)		I_{OL}	3.0	8.8	–	

FILTER A SPECIFICATIONS (V_{DD} − V_{SS} = 12 V, Clock = 153.6 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 0.875 V p-p, T_A = −40 to 85°C)

Characteristic	Min	Typ	Max	Unit
Gain (300 Hz)	17	18	19	dB
Responses (Ref. 300 Hz)				dB
2400 Hz	−3.6	−3.0	−2.4	
4800 Hz	−16	−13.8	−12.8	
Idle Noise (A_{in} = V_{AG}, Ref. to 600 Ω)	–	13	24	dBrnc
Dynamic Range (Full Scale Output/Idle Noise)	76	87	–	dB
Deviation From Linear Phase dc to 2400 Hz	–	2.5	–	deg
Power Supply Rejection Ratio (V_{DD} = 12 V +0.1 V_{RMS} @ 1 kHz)	–	36	–	dB
Crosstalk (A_{in} = V_{AG}, B_{in} = 0 dBm0, Output at A_{out} at 3 kHz)	–	76	–	dB

FILTER B SPECIFICATIONS (V_{DD} − V_{SS} = 12 V, Clock = 153.6 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 7 V p-p, T_A = −40 to 85°C)

Characteristic	Min	Typ	Max	Unit
Gain (300 Hz)	−0.7	±0.15	+0.7	dB
Response (Ref. 300 Hz)				dB
2400 Hz	−3.6	−3.0	−2.4	
4800 Hz	−16	−14.1	−12.8	
Idle Noise (B_{in} = V_{AG}, Ref. to 600 Ω)	–	9	24	dBrnc
Dynamic Range (Full Scale Output/Idle Noise)	76	91	–	dB
Deviation From Linear Phase (dc to 2400 Hz)	–	2.5	–	deg
Power Supply Rejection Ratio (V_{DD} = 12 V +0.1 V_{RMS} @ 1 kHz)	–	36	–	dB
Crosstalk (B_{in} = V_{AG}, A_{in} = 0 dBm0 @ 2 kHz, Output at B_{out})	–	76	–	dB

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS} = 12$ V, $T_A = -40$ to 85°C)

Characteristics	Symbol	Min	Typ	Max	Units
Input Rise Time (Pin 10)	t_{TLH}	–	–	4	μs
Input Fall Time (Pin 10)	t_{THL}	–	–	4	μs
Pulse Width (Pin 10)	t_{WH}	200	–	–	ns
Clock Pulse Frequency (Pin 10)	f_{CL}	50	–	400	kHz
Clock Duty Cycle (Pin 10)	–	40	–	60	%

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FUNCTIONAL DESCRIPTION OF PINS

V_{DD} (PIN 16)
Positive supply pin.

V_{SS} (PIN 8)
This is the most negative supply pin.

V_{AG}, ANALOG GROUND (PIN 1)
This pin should be held at approximately $(V_{DD} - V_{SS})/2$. All analog inputs and outputs are referenced to this pin.

+A (PIN 2)
Non-inverting input of comparator A.

–A (PIN 3)
Inverting input of comparator A.

A0 (PIN 4)
Output of comparator A. This is a standard 'B' series CMOS output.

B0 (PIN 5)
Output of comparator B. This is a standard 'B' series CMOS output.

–B (PIN 6)
Inverting input of comparator B.

+B (PIN 7)
Non-inverting input of comparator B.

V_{DG}, DIGITAL GROUND (PIN 9)
This pin is logic ground reference for the CLK and LOOP pins.

CLK, CLOCK (PIN 10)
This is the clock input that determines the location of the cutoff frequency of the filters as given below:

$$-3 \text{ dB frequency} = f_{CLK} \div 64$$

LOOP (PIN 11)
When this pin is high, the input to filter A is disconnected from the pad and shorted to the filter B output pin. With this pin low, the loop back mode is disabled.

B_{out}, LOW-PASS FILTER B OUTPUT (PIN 12)
This is the output from Filter B.

B_{in}, LOW-PASS FILTER B INPUT (PIN 13)
This is the input to filter B.

A_{out}, LOW-PASS FILTER A OUTPUT (PIN 14)
This pin is the output from Filter A.

A_{in}, LOW-PASS FILTER A INPUT (PIN 15)
This is the input to Filter A.

NOTE: V_{AG} is a high-impedance input.

FILTER DESCRIPTION

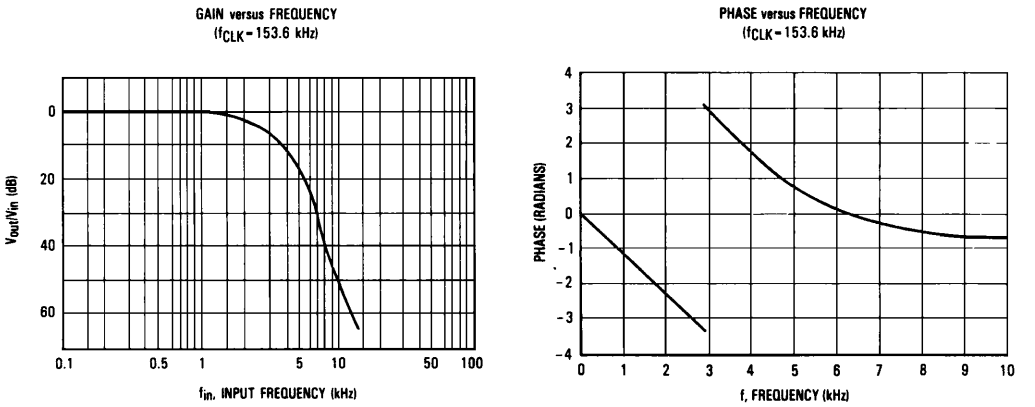
FILTER A DESCRIPTION

Filter A of the MC145415 is a 5-pole tunable linear phase low-pass filter operation at a sampling rate determined by the clock. The break frequency, which is a function of the clock, is calculated by dividing the input clock frequency by 64. With a 128 kHz clock, the band limiting frequency is 2 kHz. By dividing the clock in half to 64 kHz the band limiting frequency is cut in half to 1 kHz. Likewise, by doubling the clock, the cutoff point with double in frequency. The clock frequency can be varied from 50 kHz to 400 kHz. Filter A, unlike filter B, has a gain of 18 dB. Because the MC145415 is a switch capacitance filter, the sampled output signal will have switching components present near multiples of the switching frequency and inputs to these filters should be band-limited to under ~3/4 f_{CLK} to prevent aliasing.

FILTER B DESCRIPTION

Filter B in the MC145415 consists of a 5-pole tunable linear phase low-pass filter operating at a sampled rate determined by the clock. Filter B is functionally similar to filter A, except filter B has unity gain.

FIGURE 1 — FILTER A AND B LOW-PASS CHARACTERISTICS



NOTES: 1. Break frequency is equal to the clock frequency ÷ 64.
2. Figure 1 illustrates Filter B performance.
Filter A would be 18 dB higher.

FIGURE 2 — TEST CIRCUIT