MC145432

Advance Information

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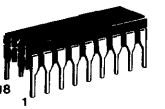
2600 Hz TONE SIGNALLING FILTER

This device contains a bypassable 6 pole 2600 Hz notch filter, a 2600 Hz band-pass filter and a 2600 Hz sinewave generator for SF signalling/detection applications.

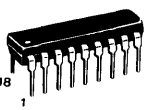
- ±5 V to ±8 V Single or Split Supply Operation
- Low Power Consumption, 80 mW @ 10 V
  200 mW @ 15 V
- On-Board Crystal Oscillator or External Clocks
- Notch Filter Gain Adjustable
- Uncommitted Op Amp Capable of Driving 600 Ω Loads
- TTL or CMOS Compatible Inputs
- 18-Pin Package

CMOS
(LOW-POWER COMPLEMENTARY MOS)

2600 Hz TONE SIGNALLING FILTER

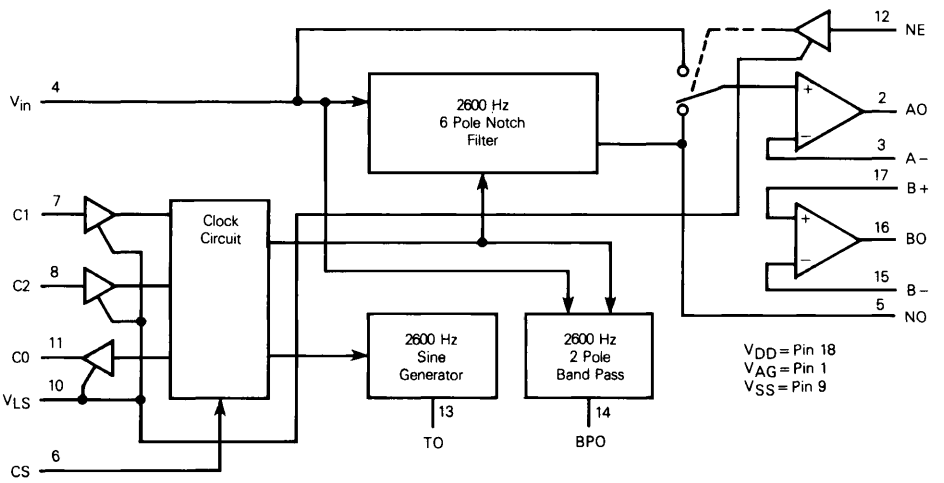


L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

BLOCK DIAGRAM

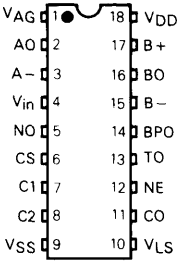


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain Per Pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	9.5	15	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, V_{DD} = 10 V, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current (CMOS Mode) @ 2.048 MHz		I_{DD}	–	8.0	10	mA
(TTL Mode) @ 2.048 MHz			–	12	15	
Input Capacitance		Cin	–	5.0	7.5	pF
MODE CONTROL LOGIC LEVELS						
V_{LS} (TTL Mode)		–	V_{SS}	–	$V_{DD}-4$	V
V_{LS} (CMOS Mode)		V_{IH}	$V_{DD}-0.5$	–	V_{DD}	V
Clock Select (CS), $V_{AG}=(V_{DD}-V_{SS})/2$	State 1	V_{IH}	$V_{DD}-0.5$	–	V_{DD}	V
	State 2	V_{IM}	$V_{AG}-0.5$	–	$V_{AG}+0.5$	
	State 3	V_{IL}	V_{SS}	–	$V_{SS}+0.5$	
TTL LOGIC LEVELS (V_{LS} = 0 V, V_{SS} = 0 V)						
Input Current (C1, C2, CS, NE)	"1" Level	I_{IH}	–	–	±0.3	μA
	"0" Level	I_{IL}	–	–	±0.3	
Input Voltage (C1, C2, CS, NE)	"1" Level	V_{IH}	$V_{LS}+2.0$	–	–	V
	"0" Level	V_{IL}	–	–	$V_{LS}+0.8$	
Output Voltage (CO) I_O = 8 mA	"1" Level	V_{OH}	2.4	–	–	V
I_O = 2.5 mA	"0" Level	V_{OL}	–	–	0.8	
CMOS LOGIC LEVELS ($V_{LS}=V_{DD}$, V_{SS} = 0 V)						
Input Current (C1, C2, CS, NE)	"1" Level	I_{IH}	–	–	±0.3	μA
	"0" Level	I_{IL}	–	–	±0.3	
Input Voltage (C1, C2, CS, NE)	"1" Level	V_{IH}	7.5	5.6	–	V
	"0" Level	V_{IL}	–	4.4	3.0	
Output Current (CO)	V_{OH} = 9.5 V	I_{OH}	−1.3	−2.25	–	mA
	V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

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ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})		I_I	–	–	±50	μA
DC Input Current (V_{in})		I_I	–	–	±10	μA
AC Input Impedance (1 kHz) (V_{in})		Z_{in}	0.2	0.1	–	MΩ
Input Voltage Range (V_{in})		V_{in}	V_{SS} + 1.5	–	V_{DD} – 1.5	V
Output Drive Current (TO, BPO, NO)	V_{OH} = V_{DD} – 1.2 V V_{OL} = V_{SS} + 1.2 V	I_{OH} I_{OL}	–0.4 +0.9	– –	– –	mA

OP AMP PERFORMANCE (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, NE = V_{SS}, V_{LS} = V_{DD}, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Offset Voltage (AO, BO)		V_{IO}	–50		+50	mV
Open Loop Gain (AO, BO)	Z_L = 600 Ω + 200 pF to V_{AG}	A_{OL}	–	45		dB
Input Bias Current (V_{in}, A–, B–, B+)		I_{IB}	–	±0.1	–	μA
Output Voltage Range (AO, BO) (R_L = 20 kΩ to V_{AG}) (R_L = 900 Ω to V_{AG}) (R_L = 600 Ω to V_{AG})		V_O	 1.0 1.1 1.8	 – – –	 9.0 8.9 8.2	V
Output Current (AO, BO)	V_{OH} = V_{DD} – 1.2 V VOL = V_{SS} + 1.2 V	I_{OH} I_{OL}	–5 +5	– –	– –	mA
Output Noise (AO, BO), 900 Ω		P_N	–	3	–	dBrnc
Slew Rate (AO, BO)		S_R	–	2	–	V/μs

NOTCH FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0 V, T_A = 0 to 70°C, NE = V_{DD})

Characteristics	Min	Max	Unit
Input Overload Voltage	–	7.0	Vpp
Gain (+2 dBm into 900 Ω @ 1 kHz)	–0.5	+0.5	dB
Idle Noise, V_{in} = V_{AG}, 900 Ω	–	25	dBrnC
Pass-Band Gain, Ref. 1 kHz Note Figure 1 300 Hz to 2 kHz 2 kHz to 2.2 kHz 2.2 kHz to 2.4 kHz 2.8 kHz to 3 kHz 3 kHz to 3.38 kHz 3.38 kHz to 4 kHz	 –0.25 –0.5 –5.0 –5.0 –0.5 –0.5	 +0.25 +0.5 +0.5 +0.5 +0.5 +0.5	dB
Rejection, Ref. 1 kHz 2.58 kHz to 2.59 kHz 2.59 kHz to 2.61 kHz 2.61 kHz to 2.62 kHz	 –45 –55 –45	 – – –	dB
Output Offset	–500	+500	mV

BY-PASS CHARACTERISTICS (V_{in} to AO, NE Low, V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Gain, 400 Hz to 4 kHz	−0.1	+0.1	dB
Noise, V_{in} = V_{AG}, 900 Ω	–	23	dBrnC
Output Offset	−50	+50	mV

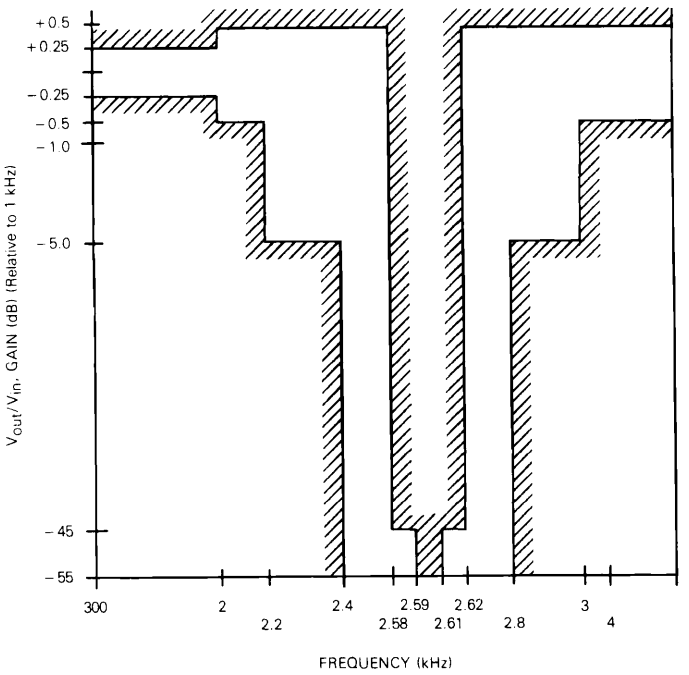
BAND-PASS CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Center Frequency, f_o	2590	2610	Hz
Q	20	23	–
Gain (+2 dBm into 900 Ω @ 2.6 kHz)	−0.5	+0.5	dB
Idle Noise, V_{in} = V_{AG}, 900 Ω	–	45	dBrnC
Output Offset	−500	+500	mV

TONE OUT CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Center Frequency	2598	2602	Hz
Output Level	0.40	0.725	Vp-p
Output Offset	−300	+300	mV

FIGURE 1 — NOTCH RESPONSE PARAMETER



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PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 18)
Most positive supply.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 9)
Most negative supply.

V_{AG}, ANALOG GROUND (PIN 1)
This pin is a high impedance input which serves as analog ground reference. This pin is nominally held at $(V_{DD}-V_{SS})/2$.

AO, OP-AMP OUT (PIN 2)
A−, OP-AMP IN (PIN 3)
These pins are for the output buffer amp which is capable of driving 600 Ω loads. A− is the inverting input of this amp while AO is its output. This amp buffers either the output of the notch filter or the input signal at V_{in} depending on the state of the NE pin.

V_{in}, INPUT (PIN 4)
This pin is the input to the notch filter, band-pass filter, and notch by-pass switch.

NO, NOTCH OUTPUT (PIN 5)
This pin is the output of the notch filter and can drive 20 kΩ loads.

NE, NOTCH ENABLE (PIN 12)
When high (see V_{LS} pin) the notch filter output is applied to the line buffer output amp. When held low (see V_{LS} pin) the input at V_{in} is applied to this op amp.

TO, TONE OUTPUT (PIN 13)
A 2600 Hz sine wave is output at this pin. This pin can drive a 20 kΩ load.

BPO, BAND-PASS OUT (PIN 14)
This pin is the output of the 2600 Hz band-pass filter and can drive a 20 kΩ load.

B+, OP-AMP NONINVERTING INPUT (PIN 17)
This pin is the noninverting input to the uncommitted op-amp provided on the circuit.

B−, OP-AMP INVERTING INPUT (PIN 15)
This pin is the inverting input of the uncommitted op-amp provided on the circuit.

BO, OP-AMP OUTPUT (PIN 16)
This pin is the output of the uncommitted op-amp provided on the circuit.

CS, CLOCK SELECT (PIN 6)
C1, C2, CLOCK INPUTS (PINS 7 AND 8)
When held at V_{DD}, CS selects the internal crystal oscillator clock mode. A 3.579545 MHz crystal is connected between pins C1 and C2. A 10 MΩ resistor should be tied across C1 and C2 along with 20 pF capacitors to V_{SS} to insure stable oscillator operation. When tied to V_{SS}, a 2.048 MHz external clock should be applied to C2. When tied to V_{AG}, a 1.536 MHz external clock should be applied to C2. In both external clock modes, C1 should be tied to V_{SS}.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 10)
This pin determines CMOS or TTL level compatibility for C1, C2, NE and CO. If tied to V_{DD}, CMOS device levels are expected; if tied to a voltage less than $V_{DD}-4$ V, TTL levels are expected with V_{LS} equal to logic ground.

CO, CLOCK OUTPUT (PIN 11)
A 128 kHz square wave is available at this pin. This is the sample clock of both the notch and band-pass filters.

FIGURE 2A — FREQUENCY SELECTION TABLE

Clock Select (CS)	Clock Source	Filter Switching Frequency f_s	Notch/Bandpass Center Frenquency f_c	Digital Clock Out (CO)
V_{DD}	Crystal (C1, C2)	$\frac{\text{Clock (Hz)}}{28}$	$\frac{\text{Clock (Hz)}}{1376}$	f_s
V_{AG}	External (C1 = V_{SS})	$\frac{\text{Clock (Hz)}}{12}$	$\frac{\text{Clock (Hz)}}{590}$	f_s
V_{SS}	External (C1 = V_{SS}	$\frac{\text{Clock (Hz)}}{16}$	$\frac{\text{Clock (Hz)}}{787.7}$	f_s

NOTE: Switching Frequency (f_s) Range = 10 kHz to 256 kHz

FIGURE 2B — FREQUENCY SELECTION TABLE

Clock Select (CS)	Clock Source	Filter Switching Frequency	Clock Out (CO)	Tone Out (TO)
V_{DD}	Crystal (C1, C2)	3.579 MHz	127.8 kHz	2601 Hz
V_{AG}	External (C1 = V_{SS})	1.536 MHz	128 KHz	2603.4 Hz
V_{SS}	External (C1 = V_{SS})	2.048 MHz	128 kHz	2599 Hz

FIGURE 3 — TEST CIRCUIT

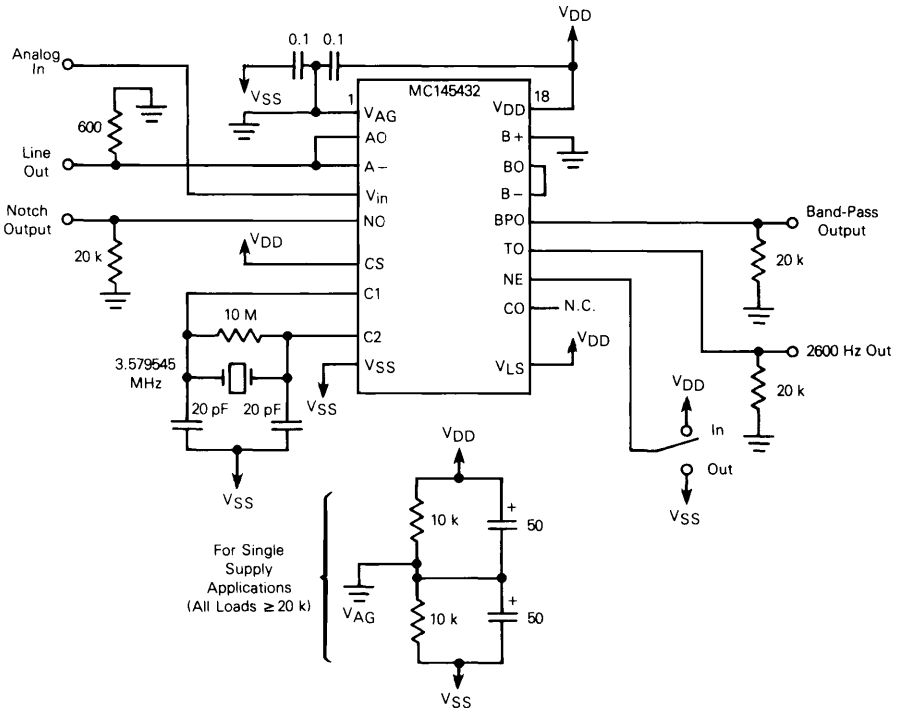
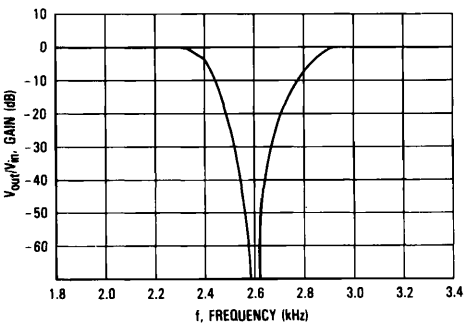


FIGURE 4—TYPICAL RESPONSE CURVES

NOTCH FREQUENCY RESPONSE



BAND-PASS FREQUENCY RESPONSE