OKI Semiconductor

MSM5238

32-DOT COMMON DRIVER

GENERAL DESCRIPTION

The MSM5238 is a dot matrix LCD common driver LSI which is fabricated by low power CMOS metal gate technology. The scanning signal in one matrix display frame can be divided into up to 1/32 duty. This LSI consists of 32-bit shift register, 32-bit level shifter and 32-bit 4-level driver.

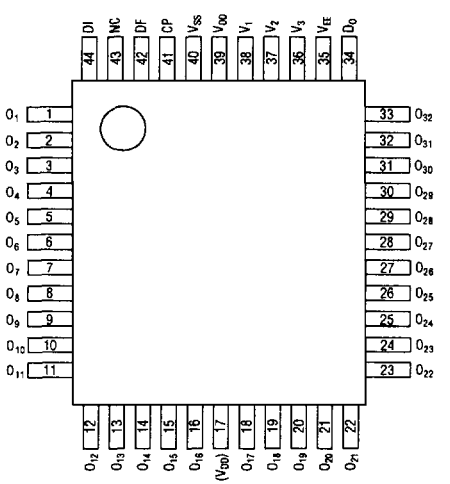
This LSI can drive a variety of LCD panel because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from external source.

FEATURES

- Supply voltage: 3 ~ 7V
- LCD driving voltage: 3 ~ 16V
- Applicable LCD duty: 1/32 ~ 1/64
  (Two chips of MSM5238 are required to drive 1/64 duty LCD panel).
- Bias voltage can be supplied externally
- 44-pin plastic QFP (QFP44-P-910-K)
- 44-pin plastic QFP (QFP44-P-910-L)
- 44-pin V plastic QFP (QFP44-P-910-VK)

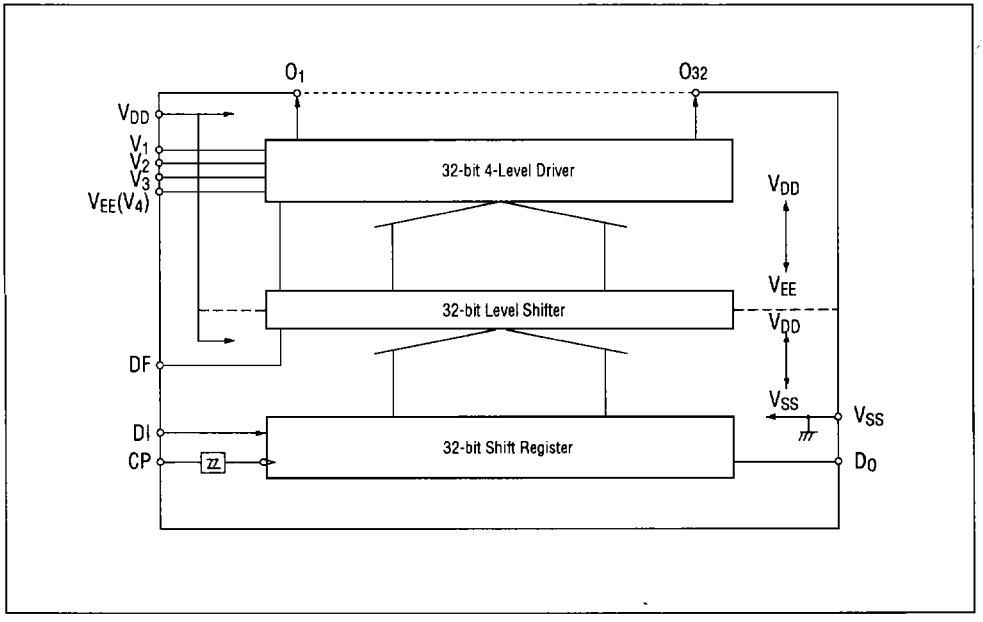
PIN CONFIGURATION (TOP VIEW)

(Top view) 44-pin plastic QFP



* Pin 17 is an auxiliary pin. It shall be connected to the power supply or disconnected to any other terminal.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Patameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta = 25°C	-0.3 ~ 7	V
Supply Voltage	$V_{DD} - V_{EE}$		0 ~ 16	V
Input Voltage	V_I		-0.3 ~ V_{DD}	V
Storage Tempeature	T_{stg}	–	-55 ~ +150	°C

- **Operating Range**

Patameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	–	3 ~ 7	V
Supply Voltage	$V_{DD} - V_{EE}$	–	3 ~ 16	V
Operation Temperature	T_{opr}	–	-40 ~ +85	°C
Fan-Out	N	MOS load	5	–

$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4$ (VEE)

• DC Characteristics

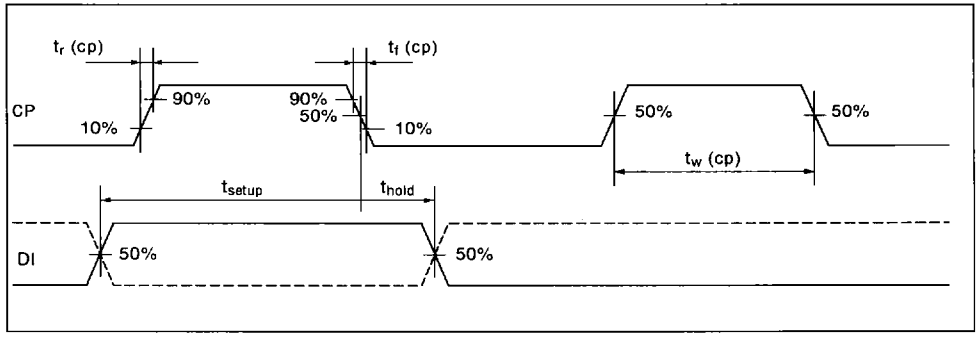
Parameter	Symbol	Condition				Min.	Typ.	Max.	Unit
		V_{DD} (V)	V_{SS} (V)	V_{EE} (V)					
"H" Input Voltage	*1 V_{IH_1}/ V_{IH_2}	5	0	0 ~ -9	–	3.6/ 4.2	–	–	V
		7	0	0 ~ -7	–	5.2/ 6.0	–	–	
"L" Input Voltage	*1 V_{IL_1}/ V_{IL_2}	5	0	0 ~ -9	–	–	–	0.8/ 0.4	V
		7	0	0 ~ -7	–			1.1/ 0.5	
Input Voltage	I_{IH}	7	0	-7	V_I = 7V	–	–	1	µA
	I_{IL}	7	0	-7	V_I = 0V	–	–	-1	
"H" Output Voltage	*2 V_{OH}	5	0	0 ~ -9	I_{OD} = -40µA	4.2	–	–	V
		7	0	0 ~ -7	I_{OD} = -56µA	5.8	–	–	
"L" Output Voltage	*2 V_{OL}	5	0	0 ~ -9	I_{OD} = 0.2mA	–	–	0.4	V
		7	0	0 ~ -7	I_{OD} = 0.3mA	–	–	0.4	
ON Resistance	R_{ON} (V_1, V_4)	5	0	0	V_O: DRV output $V_O - V_1$ = 0.25V $V_1 = V_{EE}$ ~ (V_{DD} – 0.25V) $V_O - V_4$ = 0.25V V_4 (V_{EE}): MAX 0V	–	500	2000	Ω
			0	-5		–	250	1000	
		7	0	0		–	350	1400	
			0	-7		–	200	800	
	R_{ON} (V_2, V_3)	5	0	0	$V_N = V_2$ or V_3 V = DRV output $V_O - V_N$ = 0.25V $V_N = V_{EE}$ ~ (V_{DD} – 0.25V)	–	800	3200	Ω
			0	-5		–	450	1800	
		7	0	0		–	550	2200	
			0	-7		–	350	1400	
OFF Leak Current	I_{OFF}	5	0	-9	–	–	–	±5	µA
		7	0	-7	–	–	–	±5	
Power Supply Current	I_{DD}	5	0	-9	–	–	–	0.5	mA
		7	0	-7	–	–	–	1.0	
Input Capacitance	C_I	-	-	-	–	–	5	–	pF

*1 V_{IH_1} and V_{IL_1} are input pins for DI and DF, while V_{IH_2} and V_{IL_2} are input pins for CP.

*2 V_{OH} and V_{OL} are output pins for D_0.

- **Switching Characteristics**

Parameter	Symbol	V_{DD} (V)	Condition	Min.	Typ.	Max.	Unit
Maximum Clock Frequency	$f_{(cp)}$	5	–	400	–	–	kHz
		7	–	550	–	–	
Clock Pulse Width	$t_{w(cp)}$	5	–	400	–	–	ns
		7	–	300	–	–	
Data Setup Time (DATAIN → CP)	t_{setup}	5	–	100	–	–	ns
		7	–	50	–	–	
Data Hold Time (DATAIN → CP)	t_{hold}	5	–	800	–	–	ns
		7	–	500	–	–	
Clock Pulse Rising/Falling Time	$t_{r(cp)}$	5	–	–	–	0.5	ms
	$t_{f(cp)}$	7	–	–	–	0.1	



PIN DESCRIPTION

- **DI**
  The data from LCD controller LSI is input to a 32-bit shift register from DI. (Positive logic) This LSI is applicable up to 1/32 duty LCD panel because this LSI consists of the 32-bit shift register.

- **CP**
  Clock pulse input pin for the 32-bit shift register. The data is shifted to the 32-bit level shifter at the falling edge of the clock pulse. A data set up time (t_{setup}) and data hold time (t_{hold}) is required between DI and CP signal. (Refer to SWITCHING CHARACTERISTICS.) Schmit circuit is included in CP input circuit.

- **DF**
  Alternate signal input pin for LCD driving waveform.

- **V_{DD}, V_{SS}**
  V_{DD} is a supply voltage pin. Usually it is used at V_{DD} = 3.0 ~ 7.0V. V_{SS} is a ground pin. (V_{SS} = 0V)

- **O_1 ~ O_{32}**
  Display data output pins which correspond to each data bit in the latch. One of V_1, V_2, V_3 and V_4 is selected as a display driving voltage source according to the combination of latched data level and DF signal. Refer to the truth table and Time Chart. O_1 ~ O_{32} are connected to the common side of the LCD panel.

Latched data	DF	Display data output level
L	L	V_2
	H	V_3
H	L	V_4
	H	V_1

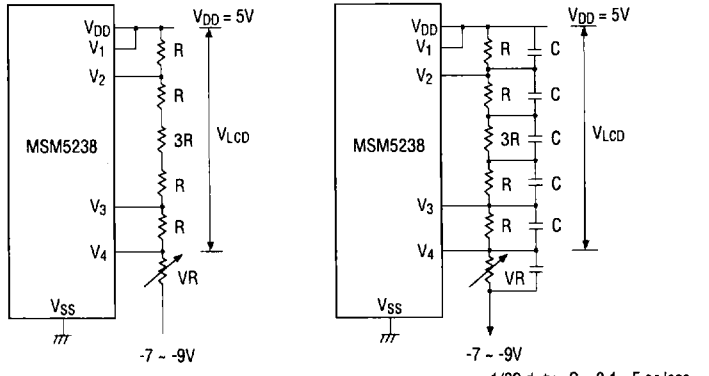


Figure 1

* The value of R should be decided according to the power consumption and LCD panel size.

- **V_1, V_2, V_3, V_4**
  Bias supply voltage pin to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source.
  Figure 1 shows the case when the bias voltage, which determines the LCD driving voltage, is supplied from the external source.

- **D_O**
  Shift register contents output pin. The data which was input from DI is output from D_O with 32 bits delay, synchronized with the clock pulse. By connecting D_O with next MSM5238GS's DI, this LSI is applicable to the LCD, the duty of which is 1/64. Refer to the Figure 2 below.

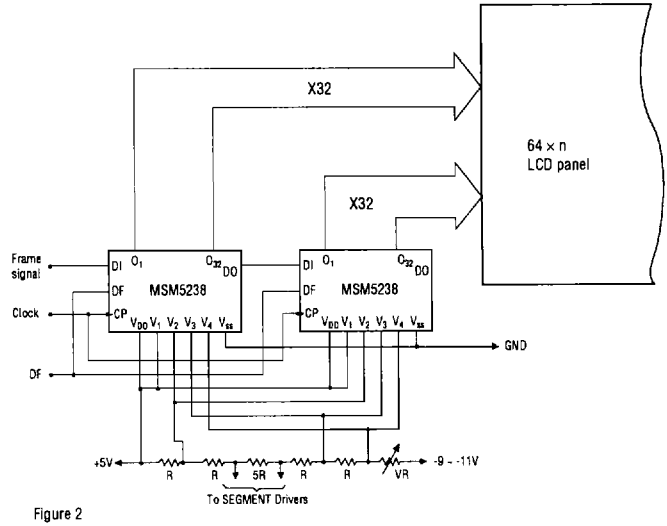


Figure 2

TIMING CHART (1/32 duty, 1/7 bias)