

T-46-13-25

PRELIMINARY



NMC27C020

NMC27C020**2,097,152-Bit (256k x 8) UV Erasable CMOS PROM****General Description**

The NMC27C020 is a high-speed 2048k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

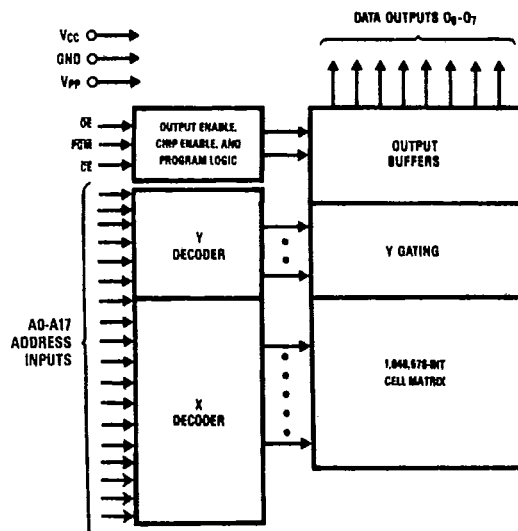
The NMC27C020 is designed to operate with a single +5V power supply with $\pm 10\%$ tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

The NMC27C020 is packaged in a 32-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
 - Active power: 110 mW max
 - Standby power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C020QE), -40°C to $+85^{\circ}\text{C}$ and military temperature range (NMC27C020QM), -55°C to $+125^{\circ}\text{C}$, available
- Pin compatible with NMOS byte-wide 2 meg EPROMs
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram**Pin Names**

A0-A17	Addresses
CE	Chip Enable
OE	Output Enable
O0-O7	Outputs
PGM	Program

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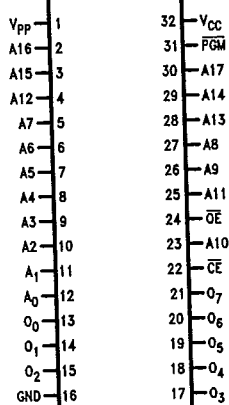
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NMC27C020

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Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C64 2764	27C010 27010
A15	V _{PP}	V _{PP}	V _{PP}	V _{PP}
A12	A12	A12	A12	A12
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O ₀	O ₀	O ₀	O ₀	O ₀
O ₁	O ₁	O ₁	O ₁	O ₁
O ₂	O ₂	O ₂	O ₂	O ₂
GND	GND	GND	GND	GND

NMC27C020Q
Dual-In-Line Package

27C010 27010	27C64 2764	27C128 27128	27C256 27256	27C512 27512
V _{CC}				
PGM				
NC	V _{CC}	V _{CC}	V _{CC}	V _{CC}
A14	PGM	PGM	A14	A14
A13	NC	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
A11	A11	A11	A11	A11
OE	OE	OE	OE	OE/V _{PP}
A10	A10	A10	A10	A10
CE	CE	CE	CE/PGM	CE
O ₇	O ₇	O ₇	O ₇	O ₇
O ₆	O ₆	O ₆	O ₆	O ₆
O ₅	O ₅	O ₅	O ₅	O ₅
O ₄	O ₄	O ₄	O ₄	O ₄
O ₃	O ₃	O ₃	O ₃	O ₃

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Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C020 pins.

Order Number NMC27C020Q
See NS Package Number J32AQCommercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC27C020Q150	150
NMC27C020Q170	170
NMC27C020Q200	200
NMC27C020Q250	250

Extended Temperature Range (-40°C to +85°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC27C020QE170	170
NMC27C020QE200	200
NMC27C020QE200	200

Military Temperature Range (-55°C to +125°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC27C020QM170	170
NMC27C020QM200	200

COMMERCIAL TEMPERATURE RANGE

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NMC27C020

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to -0.6V
All Output Voltages with Respect to Ground (Note 10)	$V_{CC} + 1.0V$ to GND - 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to -0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to -0.6V

Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (MIL Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	5V \pm 10%

READ OPERATION**DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, $f = 5$ MHz Inputs = V_{IH} or V_{IL} , $I/O = 0$ mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE} = GND$, $f = 5$ MHz Inputs = V_{CC} or GND, $I/O = 0$ mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		-0.2		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.40	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA	3.5			V
V_{OL2}	Output Low Voltage	$I_{OL} = 10$ μA			0.1	V
V_{OH2}	Output High Voltage	$I_{OH} = -10$ μA	$V_{CC} - 0.1$			V

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AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C020								Units
			Q150		Q170		Q200		Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $PGM = V_{IH}$		150		170		200		250	ns
t _{CE}	\overline{CE} to Output Delay	$\overline{OE} = V_{IL}, PGM = V_{IH}$		150		170		200		250	ns
t _{OE}	\overline{OE} to Output Delay	$\overline{CE} = V_{IL}, PGM = V_{IH}$		60		75		75		100	ns
t _{DF}	\overline{OE} High to Output Float	$\overline{CE} = V_{IL}, PGM = V_{IH}$	0	50	0	55	0	55	0	60	ns
t _{CF}	\overline{CE} High to Output Float	$\overline{OE} = V_{IL}, PGM = V_{IH}$	0	50	0	55	0	55	0	60	ns
t _{OH}	Output Hold from Addresses, \overline{CE} or \overline{OE} , Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $PGM = V_{IH}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE**T-46-13-25****Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias Operating Temp. Range
Storage Temperature -65°C to $+150^{\circ}\text{C}$

All Input Voltages except A9 with Respect to Ground (Note 10) $+6.5\text{V}$ to -0.6V

All Output Voltages with Respect to Ground (Note 10): $V_{CC} + 1.0\text{V}$ to $\text{GND} - 0.6\text{V}$

V_{PP} Supply Voltage and A9 with Respect to Ground During Programming $+14.0\text{V}$ to -0.6V

V_{CC} Supply Voltage with Respect to Ground $+7.0\text{V}$ to -0.6V

Power Dissipation 1.0W

Lead Temperature (Soldering, 10 sec.) 300°C

ESD Rating (Mil Spec 883C, Method 3015.2) 2000V

Operating Conditions (Note 7)

Temperature Range
NMC27C020QE120, 150, 200 -40°C to $+85^{\circ}\text{C}$
NMC27C020QM150, 200 -55°C to $+125^{\circ}\text{C}$

V_{CC} Power Supply $5\text{V} \pm 10\%$

READ OPERATION**DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, $f = 5\text{ MHz}$ Inputs = V_{IH} or V_{IL} , I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE} = \text{GND}$, $f = 5\text{ MHz}$ Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		-0.2		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1\text{ mA}$			0.40	V
V_{OH1}	Output High Voltage	$I_{OH} = -1.6\text{ mA}$	3.5			V
V_{OL2}	Output Low Voltage	$I_{OL} = 10\text{ }\mu\text{A}$			0.1	V
V_{OH2}	Output High Voltage	$I_{OH} = 10\text{ }\mu\text{A}$	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C020Q						Units
			E150		E170, M170		E200, M200		
			Min	Max	Min	Max	Min	Max	
t _{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $PGM = V_{IH}$		150		170		200	ns
t _{CE}	\overline{CE} to Output Delay	$\overline{OE} = V_{IL}, PGM = V_{IH}$		150		170		200	ns
t _{OE}	\overline{OE} to Output Delay	$\overline{CE} = V_{IL}, PGM = V_{IH}$		60		75		75	ns
t _{DF}	\overline{OE} High to Output Float	$\overline{CE} = V_{IL}, PGM = V_{IH}$	0	50	0	55	0	55	ns
t _{CF}	\overline{CE} High to Output Float	$\overline{OE} = V_{IL}, PGM = V_{IH}$	0	50	0	55	0	55	ns
t _{OH}	Output Hold from Addresses, \overline{CE} or \overline{OE} , Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $PGM = V_{IH}$	0		0		0		ns

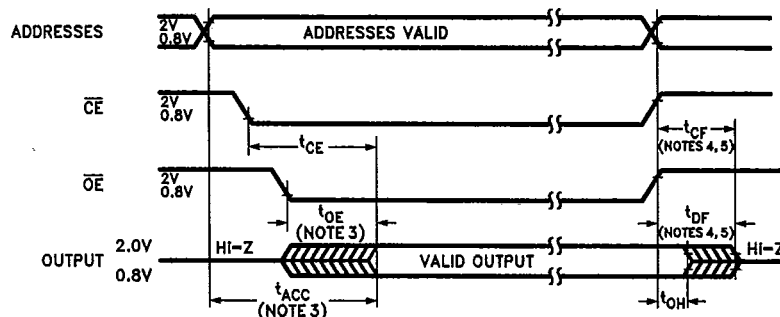
Capacitance $T_A = +25^\circ\text{C}$, $f = 1\text{ MHz}$ (Note 2)

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Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	12	15	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100\text{ pF}$ (Note 8)	Timing Measurement Reference Level	
Input Rise and Fall Times	$\leq 5\text{ ns}$	Inputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V	Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)

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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of \overline{CE} without impacting t_{ACC} .

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) $- 0.10\text{V}$;

Low to TRI-STATE, the measured V_{OL1} (DC) $+ 0.10\text{V}$.

Note 5: TRI-STATE may be attained using \overline{OE} or \overline{CE} .

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a $0.1\text{ }\mu\text{F}$ ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0\text{V}$ to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6\text{ mA}$, $I_{OH} = -400\text{ }\mu\text{A}$.

C_L : 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

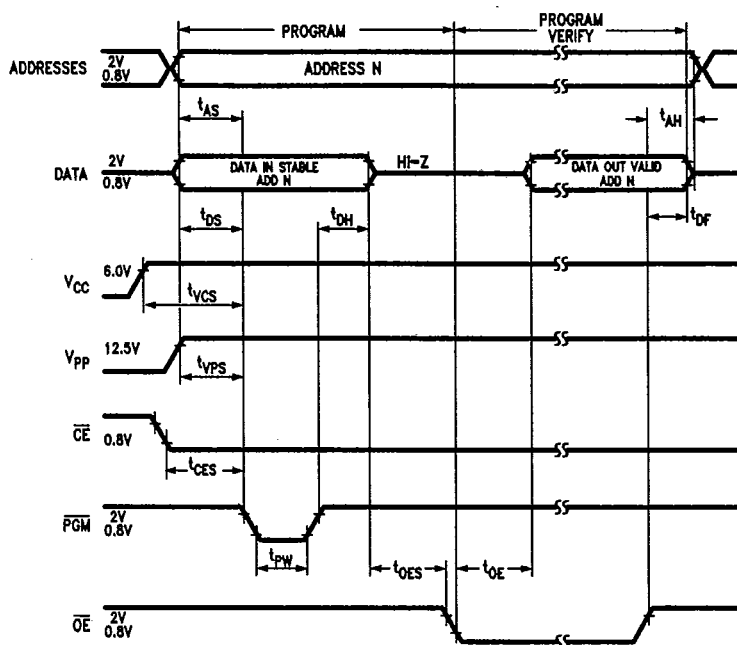
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Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _{AS}	Address Setup Time		1			μs
t _{OES}	\overline{OE} Setup Time		1			μs
t _{CES}	\overline{CE} Setup Time		1			μs
t _{DS}	Data Setup Time		1			μs
t _{VPS}	V _{PP} Setup Time		1			μs
t _{VCS}	V _{CC} Setup Time		1			μs
t _{AH}	Address Hold Time		0			μs
t _{DH}	Data Hold Time		1			μs
t _{DF}	Output Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t _{PW}	Program Pulse Width		95	100	105	μs
t _{OE}	Data Valid from \overline{OE}	$\overline{CE} = V_{IL}$			100	ns
I _{PP}	V _{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ PGM = V _{IL}			30	mA
I _{CC}	V _{CC} Supply Current				10	mA
T _A	Temperature Ambient		20	25	30	°C
V _{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V _{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t _{FR}	Input Rise, Fall Time		5			ns
V _{IL}	Input Low Voltage			0.0	0.45	V
V _{IH}	Input High Voltage		2.4	4.0		V
t _{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t _{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)

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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μ F capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

NMC27C020

Fast Programming Algorithm Flow Chart

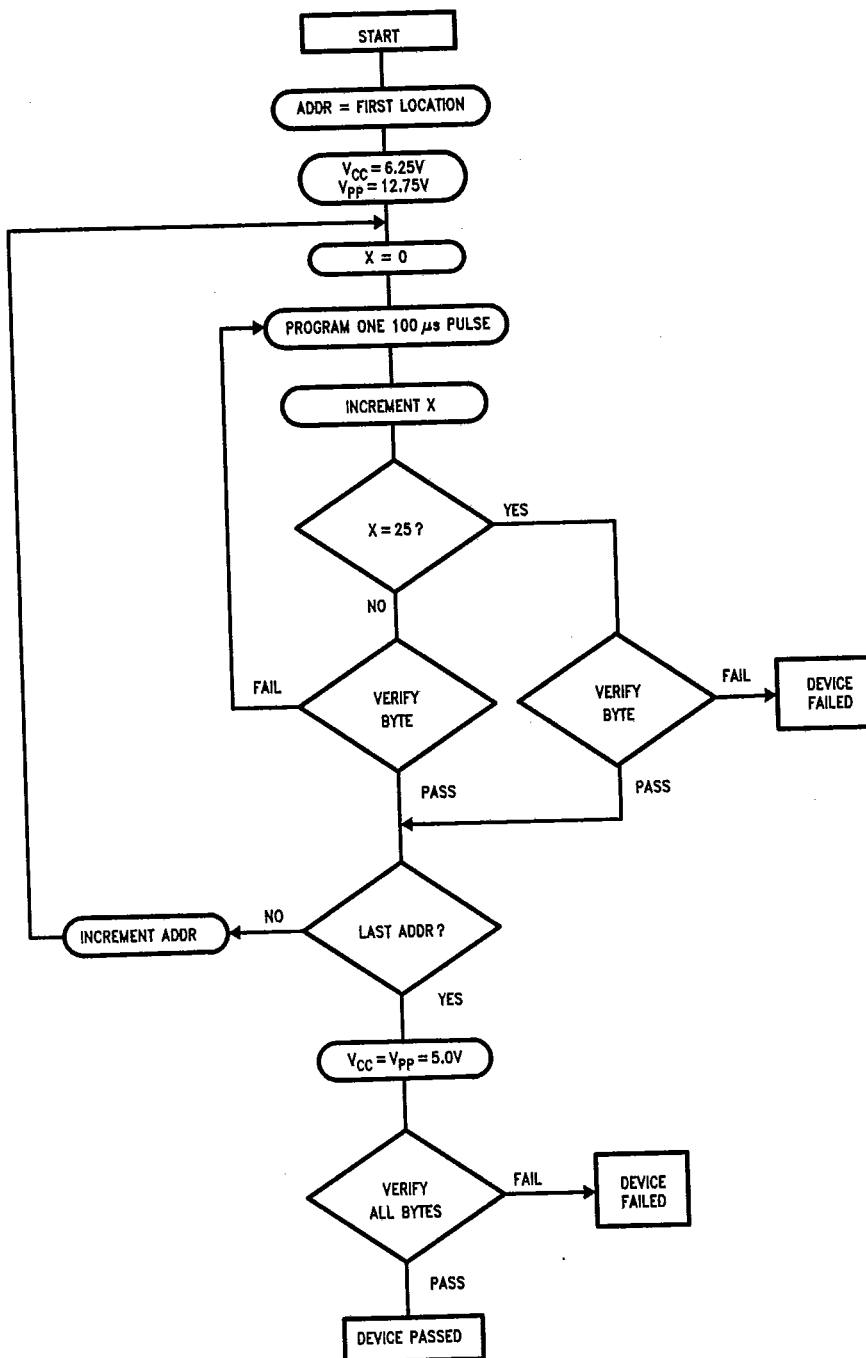


FIGURE 1

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NMC27C020

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C020 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP} . The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C020 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output Enable (\overline{OE}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of \overline{OE} , assuming that \overline{CE} has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C020 has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C020 are placed in the standby mode by applying a CMOS high signal to the \overline{CE} input. When in standby mode, the outputs are in a high impedance state, independent of the \overline{OE} input.

Output OR-Tying

Because NMC27C020s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

- the lowest possible memory power dissipation, and
- complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that \overline{CE} be decoded and used as the primary device selecting function, while \overline{OE} be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the NMC27C020.

Initially, and after each erasure, all bits of the NMC27C020 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C020 is in the programming mode when the V_{PP} power supply is at 12.75V and \overline{OE} is at V_{IH} . It is required that at least a 0.1 μ F capacitor be placed across V_{PP} , V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low TTL program pulse is applied to the \overline{PGM} input. A program pulse must be applied at each address location to be programmed. The NMC27C020 is programmed with the Fast Programming Algorithm shown in Figure 1. Each address is programmed with a series of 100 μ s pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μ s pulse. The NMC27C020 must not be programmed with a DC signal applied to the \overline{PGM} input.

Programming multiple NMC27C020s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel NMC27C020s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the \overline{PGM} input programs the paralleled NMC27C020s.

Program Inhibit

Programming multiple NMC27C020s in parallel with different data is also easily accomplished. Except for \overline{CE} , all like inputs (including \overline{OE} and \overline{PGM}) of the parallel NMC27C020s may be common. A TTL low level program pulse applied to an NMC27C020 \overline{PGM} input with \overline{CE} at V_{IL} and V_{PP} at 12.75V will program that NMC27C020. A TTL high level \overline{CE} input inhibits the other NMC27C020s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC27C020 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

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Functional Description (Continued)

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TABLE I. Mode Selection

Pins Mode	\overline{CE} (22)	\overline{OE} (24)	PGM (31)	V_{PP} (1)	V_{CC} (32)	Outputs (13-15, 17-21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	1	1	1	07

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NMC27C020 is "8F07", where "8F" designates that it is made by National Semiconductor, and "07" designates a 2 Megabit byte-wide part.

The code is accessed by applying $12V \pm 0.5V$ to address pin A9. Addresses A1-A8, A10-A17, and all control pins are held at V_{IL} . Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0-O7. Proper code access is only guaranteed at $25^\circ C \pm 5^\circ C$.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C020 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (\AA). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 \AA -4000 \AA range.

After programming, opaque labels should be placed over the NMC27C020 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C020 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (\AA). The integrated dose (i.e., UV intensity \times exposure time) for erasure should be a minimum of 15W-sec/cm².

The NMC27C020 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C020 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of

4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC} , has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE III. NMC27C020
Minimum Erasure Time

Light Intensity (Micro-Watts/cm ²)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50