

Features

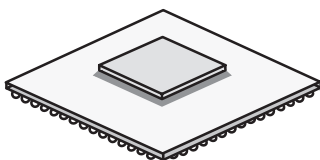
- 18.1SPECint95, estimates 12.3 SPECfp95 @400Mhz (PC755B)
- 15.7SPECint95, 9SPECfp95 @350Mhz (PC745B)
- 733 MIPS @ 400Mhz (PC755B) et 641 MIPS@350Mhz (PC745B)
- Selectable bus clock (12 CPU bus dividers up to 10x)
- P_D typical 6,4W @ 400Mhz, full operating conditions.
- Nap, doze and sleep modes for power savings
- Superscalar (3 instructions per clock cycle) (two instruction + branch)
- 4 PetaByte virtual memory, 4 Gigabytes of physical memory.
- 64-bit data and 32-bit address bus interface.
- 32KB instruction and data cache.
- Six independent execution units.
- Write-back and write-through operations.
- f_{int} max = 400Mhz (TBC)
- f_{bus} max = 100Mhz
- Voltage I/O 1,8V/3,3V ; voltage int 2.0 V

Description

PC755B and PC745B PowerPC microprocessors are high-performance, low-power, 32-bit implementations of the PowerPC Reduced Instruction Set Computer (RISC) architecture, specially enhanced for embedded applications.

PC755B and PC745B microprocessors differ only in that the PC755B features an enhanced, dedicated L2 cache interface with on-chip L2 tags. The PC755B is a drop-in replacement for the award winning PowerPC 750™ microprocessor and is footprint and user software code compatible with the MPC7400 microprocessor with AltiVec™ technology. The PC745B is a drop-in replacement for the PowerPC 740™ microprocessor and is also footprint and user software code compatible with the PowerPC 603e™ microprocessor. PC755B/745B microprocessors provide on-chip debug support and are fully JTAG-compliant.

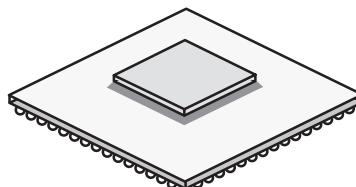
The PC745B microprocessor is pin compatible with the TSPC603e family.



ZF suffix

PBGA255

Flip-Chip Plastic Ball Grid Array



ZF suffix

PBGA360

Flip-Chip Plastic Ball Grid Array

Screening

This product is manufactured in full compliance with :

- CBGA upscreenings based upon ATMEL-Grenoble standards
- Full military temperature range (T_j= -55°C,+125°C)
industrial temperature range (T_j= -40°C,+110°C)



PowerPC755B/745B RISC MICROPRO- CESSOR

Preliminary Specification α-site

PC755B/745B

September 2000





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A. GENERAL DESCRIPTION

1. SIMPLIFIED BLOCK DIAGRAM

The PC755B is targeted for low power systems and supports the following power management features-doze, nap, sleep, and dynamic power management. The PC755B consists of a processor core and an internal L2 Tag combined with a dedicated L2 cache interface and a 60x bus.

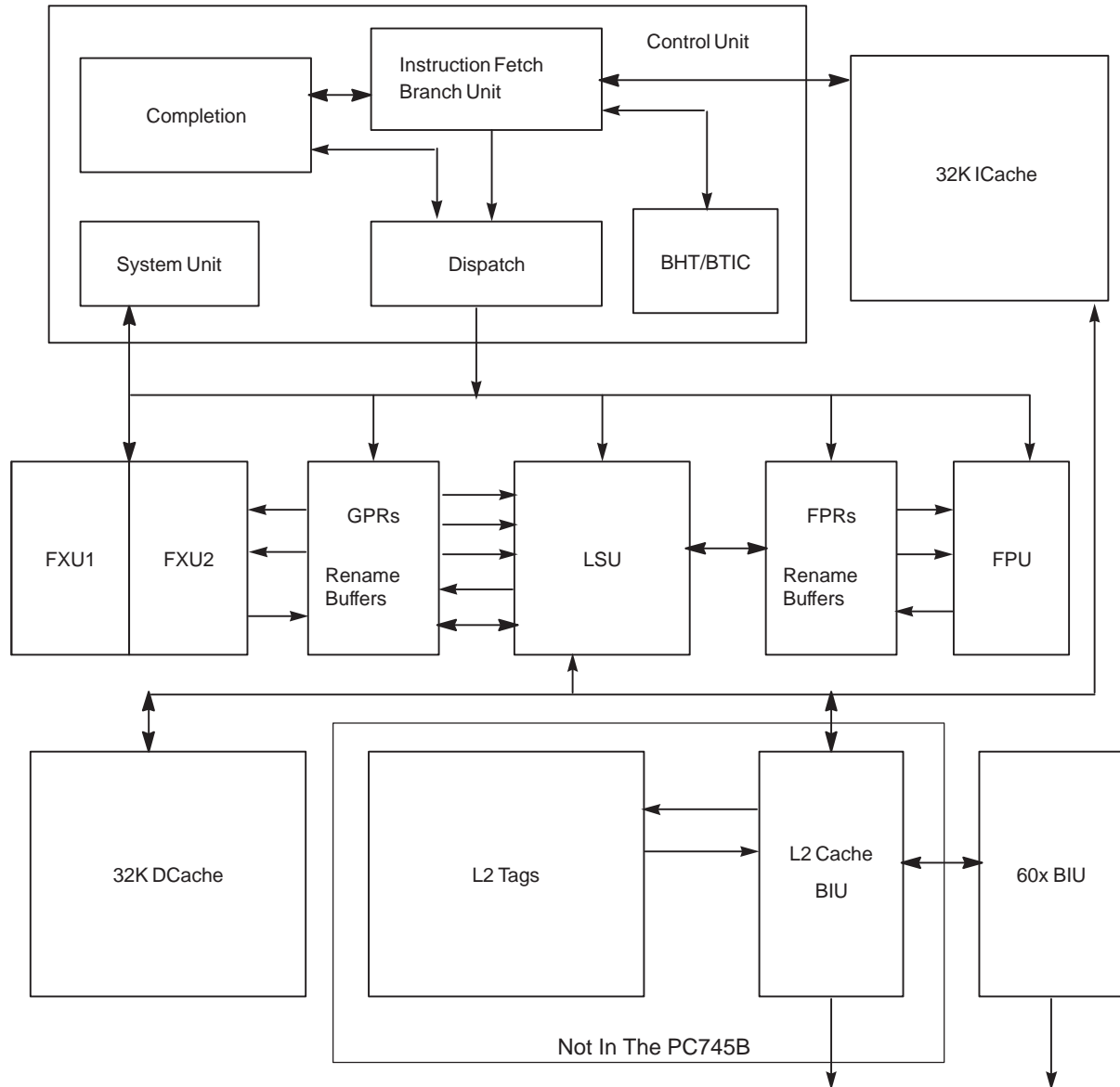


Figure 1 : PC755B Block Diagram

1.1. General parameters

The following list provides a summary of the general parameters of the PC755B:

Technology	0.22 μ m CMOS, six-layer metal
Die size	6.61 mm x 7.73 mm (51 mm ²)
Transistor count	6.75 million
Logic design	Fully-static Packages
PC745B:	Surface mount 255 plastic ball grid array (PBGA)
PC755B:	Surface mount 360 plastic ball grid array (PBGA)
Core power supply:	2.0V 100 mV dc (nominal; see table 5 for recommended operating conditions)
I/O power supply	1.8V 100 mV dc or 2.0V 100 mV dc or 3.3V 165mV dc (input thresholds are configuration pin selectable)

1.2. Features

This section summarizes features of the PC755B's implementation of the PowerPC architecture. Major features of the PC755B are as follows:

- Branch processing unit
 - Four instructions fetched per clock
 - One branch processed per cycle (plus resolving 2 speculations)
 - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
 - 512-entry branch history table (BHT) for dynamic prediction
 - 64-entry, 4-way set associative Branch Target Instruction Cache (BTIC) for eliminating branch delay slots
- Dispatch unit
 - Full hardware detection of dependencies (resolved in the execution units)
 - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
 - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
 - Register file access
 - Forwarding control
 - Partial instruction decode
- Completion
 - 6 entry completion buffer
 - Instruction tracking and peak completion of two instructions per cycle
 - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization and all instruction flow changes
- Fixed Point Units (FXUs) that share 32 GPRs for integer operands
 - Fixed Point Unit 1 (FXU1)-multiply, divide, shift, rotate, arithmetic, logical
 - Fixed Point Unit 2 (FXU2)-shift, rotate, arithmetic, logical
 - Single-cycle arithmetic, shifts, rotates, logical
 - Multiply and divide support (multi-cycle)
 - Early out multiply

- Floating-point unit and a 32-entry FPR file
 - Support for IEEE-754 standard single and double precision floating point arithmetic
 - Hardware support for divide
 - Hardware support for denormalized numbers
 - Single-entry reservation station
 - Supports non-IEEE mode for time-critical operations
- System unit
 - Executes CR logical instructions and miscellaneous system instructions
 - Special register transfer instructions
- Load/store unit
 - One cycle load or store cache access (byte, half-word, word, double-word)
 - Effective address generation
 - Hits under misses (one outstanding miss)
 - Single-cycle unaligned access within double word boundary
 - Alignment, zero padding, sign extend for integer register file
 - Floating point internal format conversion (alignment, normalization)
 - Sequencing for load/store multiples and string operations
 - Store gathering
 - Cache and TLB instructions
 - Big and Little-endian byte addressing supported
 - Misaligned Little-endian supported
- Level 1 Cache structure
 - 32K, 32-byte line, 8-way set associative instruction cache (iL1)
 - 32K, 32-byte line, 8-way set associative data cache (dL1)
 - Cache locking for both instruction and data caches, selectable by group of ways
 - Single-cycle cache access
 - Pseudo least-recently used (PLRU) replacement
 - Copy-back or Write Through data cache (on a page per page basis)
 - Supports all PowerPC memory coherency modes
 - Non-Blocking instruction and data cache (one outstanding miss under hits)
 - No snooping of instruction cache
- Level 2 (L2) Cache Interface (not implemented on PC745B)
 - Internal L2 cache controller and tags; external data SRAMs
 - 256K, 512K, and 1Mbyte 2-way set associative L2 cache support
 - Copyback or write-through data cache (on a page basis, or for all L2)
 - Instruction-only mode and data-only mode.
 - 64byte (256K/512K) or 128byte (1M) sectorized line size
 - Supports flow through (register-buffer) synchronous burst SRAMs, pipelined (register-register) synchronous burst SRAMs (3-1-1-1 or strobeless 4-1-1-1) and pipelined (register-register) late-write synchronous burst SRAMs
 - L2 configurable to direct mapped SRAM interface or split cache/direct mapped or private memory
 - Core-to-L2 frequency divisors of 1, 1.5, 2, 2.5, and 3 supported
 - 64 bit data bus
 - Selectable interface voltages of 1.8V/2.0V and 3.3V
 - Parity checking on both L2 address and data

- Memory Management Unit
 - 128 entry, 2-way set associative instruction TLB
 - 128 entry, 2-way set associative data TLB
 - Hardware reload for TLBs
 - Hardware or optional software tablewalk support
 - 8 instruction BATs and 8 data BATs
 - 8 SPRGs, for assistance with software tablewalks
 - Virtual memory support for up to 4 exabytes (2^{52}) of virtual memory
 - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Bus Interface
 - Compatible with 60X processor interface
 - 32-bit address bus
 - 64-bit data bus, 32-bit mode selectable
 - Bus-to-core frequency multipliers of 2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x supported
 - Selectable interface voltages of 3.3V and 1.8V/2.0V. Low voltage selection allows compatibility with either the 2.0V Vdd supply or with 1.8V supplies needed for peripheral devices.
 - Parity checking on both address and data busses
- Power management
 - Low-power design with thermal requirements very similar to PC740/750.
 - Selectable interface voltage of 1.8V/2.0V can reduce power in output buffers (compared to 3.3V)
 - Three static power saving modes: doze, nap, and sleep
 - Dynamic power management
- Testability
 - LSSD scan design
 - IEEE 1149.1 JTAG interface
- Integrated Thermal Management Assit Unit
 - One -ship thermal sensor and control logic
 - Thermal Management Interrrup for software regulation of junction temperature

2. PIN ASSIGNMENTS

Figure 2 (in part A) shows the pinout of the PC745B, 255PBGA package as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

Part A

Pinout of the PC745B, 255 PBGA Package as Viewed from the Top Surface

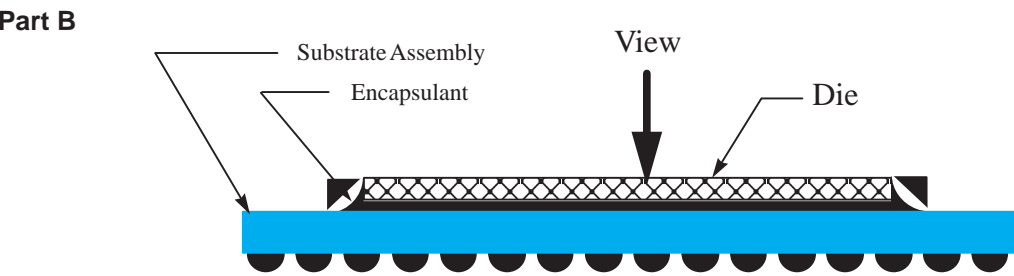
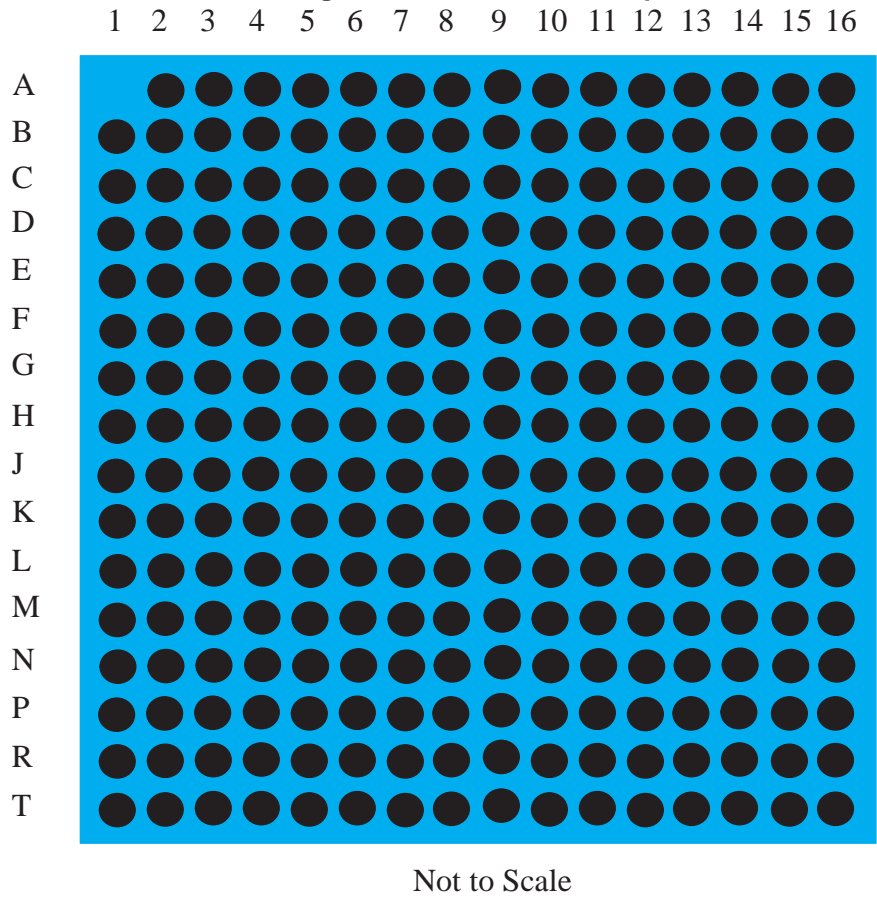
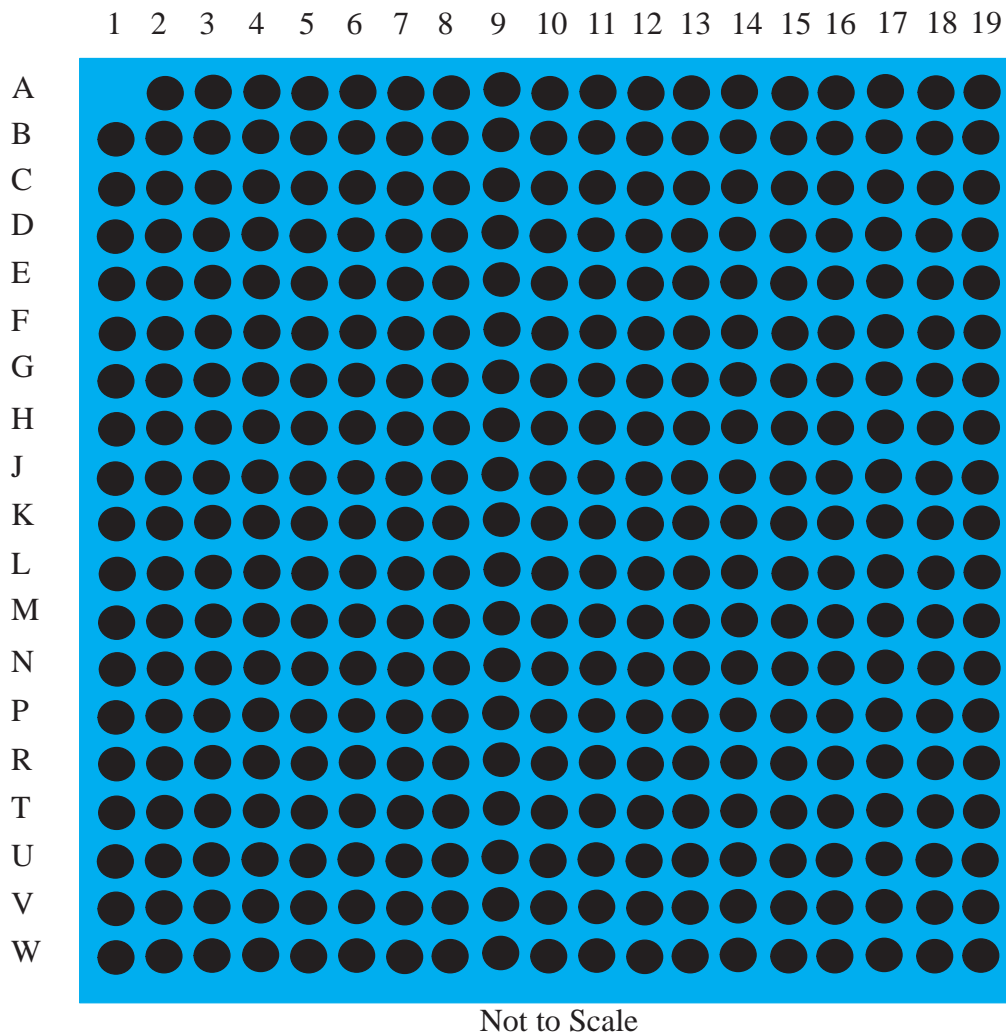


Figure 2 : Pinout of the PC745B, 255 PBGA Package as Viewed from the Top Surface

Figure 3 (in part A) shows the pinout of the PC755B, 360 PBGA packages as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

Part A



Part B

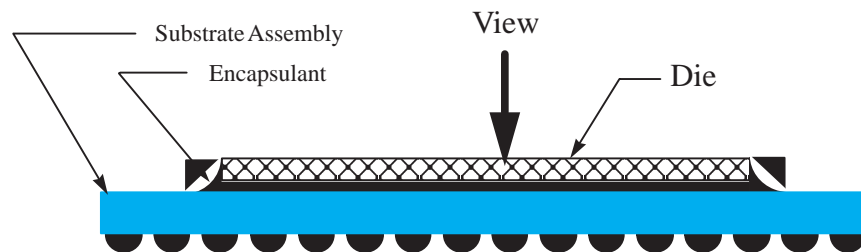


Figure 3 : Pinout of the PC755B, 360 PBGA Packages as Viewed from the Top Surface

2.1. PINOUT LISTINGS

2.1.1. Pinout listing for the PC745B, 255 PBGA

Table 1 provides the pinout listing for the PC745B, 255 PBGA package.

Table 1. Pinout Listing for the PC745B, 255 PBGA Package						
				I/F Voltages Supported ¹		
Signal Name	Pin Number	Active	I/O	1.8V/2.0V	3.3V	Notes
A[0–31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	—	—	
AACK	L2	Low	Input	—	—	
ABB	K4	Low	I/O	—	—	
AP[0–3]	C1, B4, B3, B2	High	I/O	—	—	
ARTRY	J4	Low	I/O	—	—	
AVDD	A10	—	—	2.0V	2.0V	
BG	L1	Low	Input	—	—	
BR	B6	Low	Output	—	—	
BVSEL	B1	High	Input	GND	3.3V	3, 4, 5
CI	E1	Low	Output	—	—	
CKSTP_IN	D8	Low	Input	—	—	
CKSTP_OUT	A6	Low	Output	—	—	
CLK_OUT	D7	—	Output	—	—	
DBB	J14	Low	I/O	—	—	
DBG	N1	Low	Input	—	—	
DBDIS	H15	Low	Input	—	—	
DBWO	G4	Low	Input	—	—	
DH[0–31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	—	—	
DL[0–31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	—	—	
DP[0–7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	—	—	
DRTRY	G16	Low	Input	—	—	
GBL	F1	Low	I/O	—	—	

Table 1. Pinout Listing for the PC745B, 255 PBGA Package

Signal Name	Pin Number	Active	I/O	1.8V/2.0V	3.3V	Notes
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12	—	—	GND	GND	
HRESET	A7	Low	Input	—	—	
INT	B15	Low	Input	—	—	
L1_TSTCLK	D11	High	Input	—	—	2
L2_TSTCLK	D12	High	Input	—	—	2
LSSD_MODE	B10	Low	Input	—	—	2
MCP	C13	Low	Input	—	—	
NC (No-Connect)	B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B5	—	—	—	—	
OVDD	C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10	—	—	1.8V/2.0V	3.3V	
PLL_CFG[0–3]	A8, B9, A9, D9	High	Input	—	—	
QACK	D3	Low	Input	—	—	
QREQ	J3	Low	Output	—	—	
RSRV	D1	Low	Output	—	—	
SMI	A16	Low	Input	—	—	
SRESET	B14	Low	Input	—	—	
SYSCLK	C9	—	Input	—	—	
TA	H14	Low	Input	—	—	
TBEN	C2	High	Input	—	—	
TBST	A14	Low	I/O	—	—	
TCK	C11	High	Input	—	—	
TDI	A11	High	Input	—	—	5
TDO	A12	High	Output	—	—	
TEA	H13	Low	Input	—	—	
TLBISYNC	C4	Low	Input	—	—	
TMS	B11	High	Input	—	—	5
TRST	C10	Low	Input	—	—	5
TS	J13	Low	I/O	—	—	
TSIZ[0–2]	A13, D10, B12	High	Output	—	—	

Table 1. Pinout Listing for the PC745B, 255 PBGA Package

Signal Name	Pin Number	Active	I/O	1.8V/2.0V	3.3V	Notes
TT[0–4]	B13, A15, B16, C14, C15	High	I/O	—	—	
WT	D2	Low	Output	—	—	
VDD 2	F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11	—	—	2.0V	2.0V	
VOLTDET	F3	High	Output	—	—	6

Notes:

1. OVdd supplies power to the processor bus, JTAG, and all control signals and Vdd supplies power to the processor core and the PLL (after filtering to become AVDD). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration of Table 4 and the voltage supplied. For actual recommended value of Vin or supply voltages see Table 3.
2. These are test signals for factory use only and must be pulled up to OVdd for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OVDD (selects 3.3V) or to OGND (selects 1.8V/2.0V).
4. Uses one of 15 existing no-connects in PC745's 255-bga package.
5. Internal pull up on die.
6. Internally tied to GND in the PC745B 255-bga package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.

2.1.2. Pinout listing for the PC755B, 360P PBGA package.

Table 2 provides the pinout listing for the PC755B, 360 PBGA.

Table 2. Pinout Listing for the PC755B, 360 PBGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported ¹		Notes
				1.8V/2.0V	3.3V	
A[0–31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	—	—	
$\overline{\text{AACK}}$	N3	Low	Input	—	—	
ABB	L7	Low	I/O	—	—	
AP[0–3]	C4, C5, C6, C7	High	I/O	—	—	
$\overline{\text{ARTRY}}$	L6	Low	I/O	—	—	
AVDD	A8	—	—	2.0V	2.0V	
$\overline{\text{BG}}$	H1	Low	Input	—	—	
$\overline{\text{BR}}$	E7	Low	Output	—	—	
BVSEL	W1	High	Input	GND	3.3V	3, 5, 6
$\overline{\text{CI}}$	C2	Low	Output	—	—	
CKSTP_IN	B8	Low	Input	—	—	

Table 2. Pinout Listing for the PC755B, 360 PBGA Package

Signal Name	Pin Number	Active	I/O	1.8V/2.0V	3.3V	Notes
CKSTP_OUT	D7	Low	Output	—	—	
CLK_OUT	E3	—	Output	—	—	
DBB	K5	Low	I/O	—	—	
DBDIS	G1	Low	Input	—	—	
DBG	K1	Low	Input	—	—	
DBW0	D1	Low	Input	—	—	
DH[0–31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	—	—	
DL[0–31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	—	—	
DP[0–7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	—	—	
DRTRY	H6	Low	Input	—	—	
GBL	B1	Low	I/O	—	—	
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—	GND	GND	
HRESET	B6	Low	Input	—	—	
INT	C11	Low	Input	—	—	
L1_TSTCLK	F8	High	Input	—	—	2
L2ADDR[0–16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	—	—	
L2AVDD	L13	—	—	2.0V	2.0V	
L2CE	P17	Low	Output	—	—	
L2CLKOUTA	N15	—	Output	—	—	
L2CLKOUTB	L16	—	Output	—	—	

Table 2. Pinout Listing for the PC755B, 360 PBGA Package

Signal Name	Pin Number	Active	I/O	1.8V/2.0V	3.3V	Notes
L2DATA[0–63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	—	—	
L2DP[0–7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	—	—	
L2OVDD	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	—	—	1.8V/2.0V	3.3V	
L2SYNC_IN	L14	—	Input	—	—	
L2SYNC_OUT	M14	—	Output	—	—	
L2_TSTCLK	F7	High	Input	—	—	2
L2VSEL	A19	High	Input	GND	3.3V	1, 3, 5, 6
L2WE	N16	Low	Output	—	—	
L2ZZ	G17	High	Output	—	—	
LSSD_MODE	F9	Low	Input	—	—	2
MCP	B11	Low	Input	—	—	
NC (No-Connect)	B3, B4, B5, W19, K9, K11 ⁴ , K19 ⁴	—	—	—	—	
OVDD	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—	1.8V/2.0V	3.3V	
PLL_CFG[0–3]	A4, A5, A6, A7	High	Input	—	—	
QACK	B2	Low	Input	—	—	
QREQ	J3	Low	Output	—	—	
RSRV	D3	Low	Output	—	—	
SMI	A12	Low	Input	—	—	
SRESET	E10	Low	Input	—	—	
SYSCLK	H9	—	Input	—	—	
TA	F1	Low	Input	—	—	
TBEN	A2	High	Input	—	—	
TBST	A11	Low	I/O	—	—	
TCK	B10	High	Input	—	—	

Table 2. Pinout Listing for the PC755B, 360 PBGA Package

Signal Name	Pin Number	Active	I/O	1.8V/2.0V	3.3V	Notes
TDI	B7	High	Input	—	—	6
TDO	D9	High	Output	—	—	
$\overline{\text{TEA}}$	J1	Low	Input	—	—	
$\overline{\text{TLBISYNC}}$	A3	Low	Input	—	—	
TMS	C8	High	Input	—	—	6
$\overline{\text{TRST}}$	A10	Low	Input	—	—	6
$\overline{\text{TS}}$	K7	Low	I/O	—	—	
TSIZ[0–2]	A9, B9, C9	High	Output	—	—	
TT[0–4]	C10, D11, B12, C12, F11	High	I/O	—	—	
$\overline{\text{WT}}$	C3	Low	Output	—	—	
VDD	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	—	—	2.0V	2.0V	
VOLTDET	K13	High	Output	—	—	7

Notes:

1. OVdd supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls ($\overline{\text{L2CE}}$, $\overline{\text{L2WE}}$, and $\overline{\text{L2ZZ}}$); L2OVDD supplies power to the L2 cache interface (L2ADDR[0-16], L2DATA[0-63], L2DP[0-7] and L2SYNC-OUT) and the L2 control signals; and Vdd supplies power to the processor core and the PLL and DLL (after filtering to become AVDD and L2AVDD respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 4 and the voltage supplied. For actual recommended value of Vin or supply voltages see Table 5.
2. These are test signals for factory use only and must be pulled up to OVdd for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OVDD (selects 3.3V) or to OGND (selects 1.8V/2.0V).
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of 9 existing no-connects in PC750's 360-bga package.
6. Internal pull up on die.
7. Internally tied to L2OVDD in the PC755B 360-bga package to indicate the power present at the L2 cache interface. This signal is not a power supply input.

Caution: This is different from the PC745B 255-bga package.

2.2. Signal description

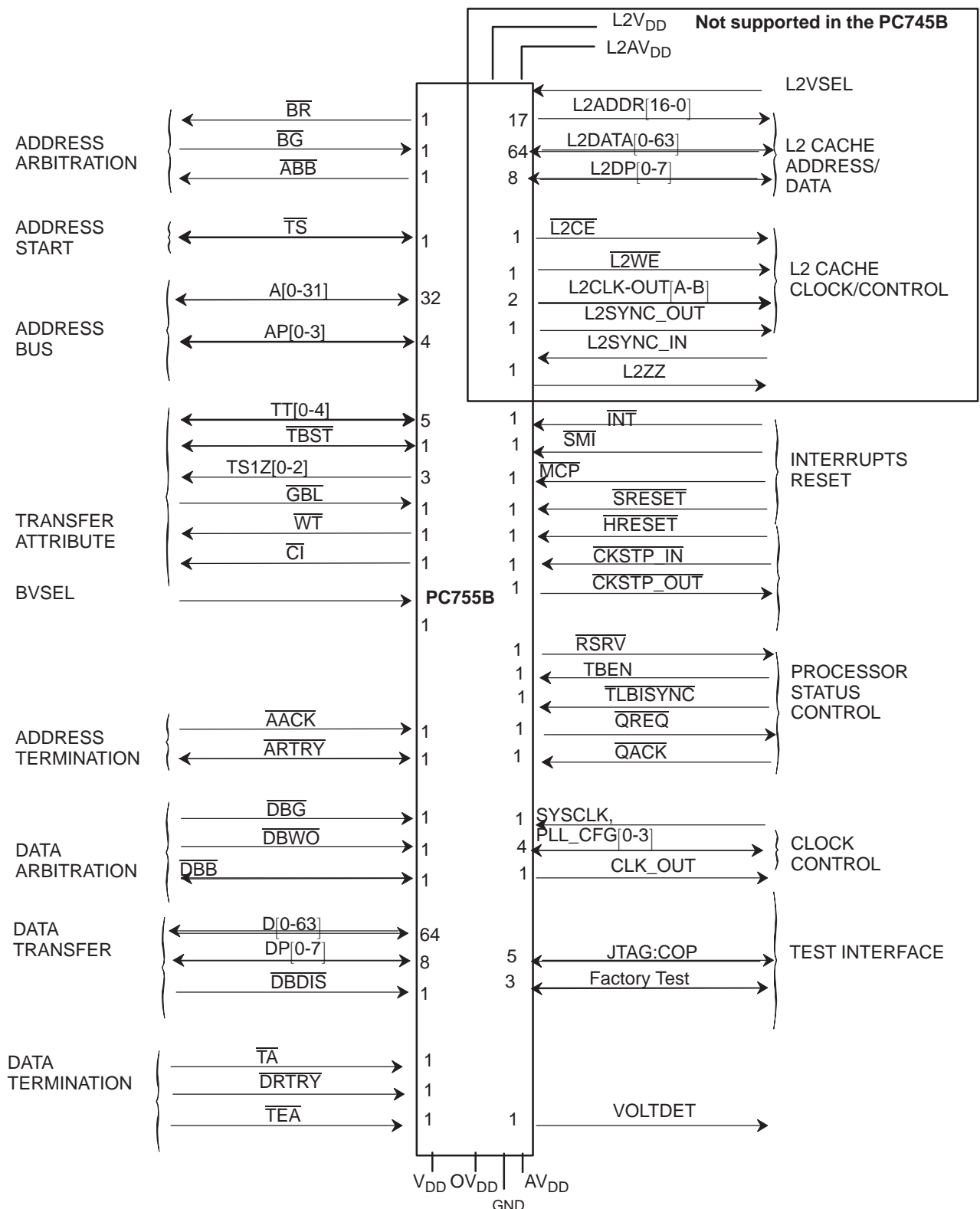


Figure 4 : PC755B microprocessor signal groups

B. DETAILED SPECIFICATION

1. SCOPE

This drawing describes the specific requirements for the microprocessor PC755B, in compliance with ATMEL Grenoble standard screening.

2. APPLICABLE DOCUMENTS

- 1) MIL-STD-883 : Test methods and procedures for electronics.
- 2) MIL-PRF-38535 appendix A : General specifications for microcircuits.

3. REQUIREMENTS

3.1. General

The microcircuits are in accordance with the applicable documents and as specified herein.

3.2. Design and construction

3.2.1. Terminal connections

Depending on the package, the terminal connections is shown in table 1, table 2 and Figure 4.

3.2.2. Absolute maximum rating

Table 3. Absolute Maximum Ratings					
Characteristic		Symbol	Maximum Value	Unit	Note
Core supply voltage		V _{dd}	−0.3 to 2.5	V	4
PLL supply voltage		AV _{dd}	−0.3 to 2.5	V	4
L2 DLL supply voltage		L2AV _{dd}	−0.3 to 2.5	V	4
Processor bus supply voltage		OV _{dd}	−0.3 to 3.465	V	3
L2 bus supply voltage		L2OV _{dd}	−0.3 to 3.465	V	3
Input voltage	Processor bus	V _{in}	−0.3 to OV _{dd} + 0.3V	V	2,5
	L2 Bus	V _{in}	−0.3 to L2OV _{dd} + 0.3V	V	2,5
	JTAG Signals	V _{in}	−0.3 to 3.6	V	
Storage temperature range		T _{stg}	−55 to 150	°C	
Notes: 1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device. 2. Caution: V _{in} must not exceed OV _{dd} or L2OV _{dd} by more than 0.3V at any time including during power-on reset. 3. Caution: L2OV _{dd} /OV _{dd} must not exceed V _{dd} /AV _{dd} /L2AV _{dd} by more than 1.2V at any time including during power-on reset. 4. Caution: V _{dd} /AV _{dd} /L2AV _{dd} must not exceed L2OV _{dd} /OV _{dd} by more than 0.4V at any time including during power-on reset. 5. V _{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.					

Figure 5 shows the allowable overshoot and undershoot voltage on the PC755B and PC745B

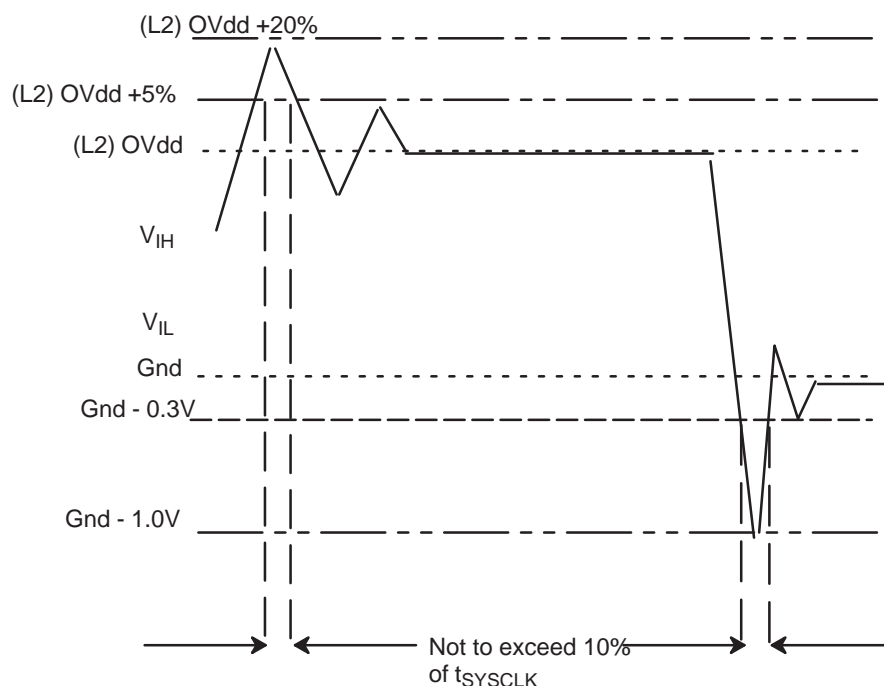


Figure 5 : Overshoot/Undershoot Voltage

The PC755B provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC755B core voltage must always be provided at nominal 2.0V (see Table 5 for actual recommended core voltage). Voltage to the L2 I/Os and Processor Interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 4. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OVdd or L2OVdd power pins.

Table 4 describes the input threshold voltage setting .

Table 4. Input Threshold Voltage Setting			
BVSEL Signal	L2VSEL Signal	Processor Bus Interface Voltage	L2 Bus Interface Voltage
0	0	1.8V or 2.0V	1.8V or 2.0V
0	1	1.8V or 2.0V	3.3V
1	0	3.3V	1.8V or 2.0V
1	1	3.3V	3.3V
Note Caution: The input threshold selection must agree with the OVdd/L2OVdd voltages supplied.			

3.3. Recommended operating conditions

Table 5. Recommended Operating Conditions				
Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		Vdd	2.0v \pm 100mV	V
PLL supply voltage		AVdd	2.0v \pm 100mV	V
L2 DLL supply voltage		L2AVdd	2.0v \pm 100mV	V
Processor bus supply voltage	BVSEL = 0	OVdd	1.8v \pm 100mV or 2.0 \pm 100mV	V
	BVSEL = 1	OVdd	3.3v \pm 165mV	V
L2 bus supply voltage	L2VSEL = 0	L2OVdd	1.8v \pm 100mV or 2.0 \pm 100mV	V
	L2VSEL = 1	L2OVdd	3.3v \pm 165mV	V
Input voltage	Processor bus	V _{in}	GND to OVdd	V
	L2 Bus	V _{in}	GND to L2OVdd	V
	JTAG Signals	V _{in}	GND to OVdd	V
Die-junction temperature		T _j	-55 to 125	°C
Note : These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.				

3.4. Thermal characteristics

3.4.1. Package characteristics

Table 6 provides the package thermal characteristics for the PC755B.

Table 6. Package Thermal Characteristics			
Characteristic	Symbol	Value	Rating
PBGA package thermal resistance, junction-to-case thermal resistance (typical)	θ_{JC}	0.03	C/W
PBGA package thermal resistance, die junction-to-lead thermal resistance (typical)	θ_{JB}	12	C/W
PBGA package typical thermal resistance, die junction-to-ambient resistance (convection only on 2S2P board)	θ_{JA}	33	C/W
PBGA package thermal resistance, die junction-to-ambient resistance (100 ft/min airflow on 2S2P board)	θ_{JA}	30	C/W
Note: Refer to Section 3.4.3. , "Thermal Management Information," for more details about thermal management.			

The board designer can choose between several types of heat sinks to place on the PC755B. There are several commercially-available heat sinks for the PC755B provided by the following vendors:

For the exposed-die packaging technology, shown in Table 5, the intrinsic conduction thermal resistance paths are as follows :

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 6 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/conductive thermal resistances are the dominant terms.

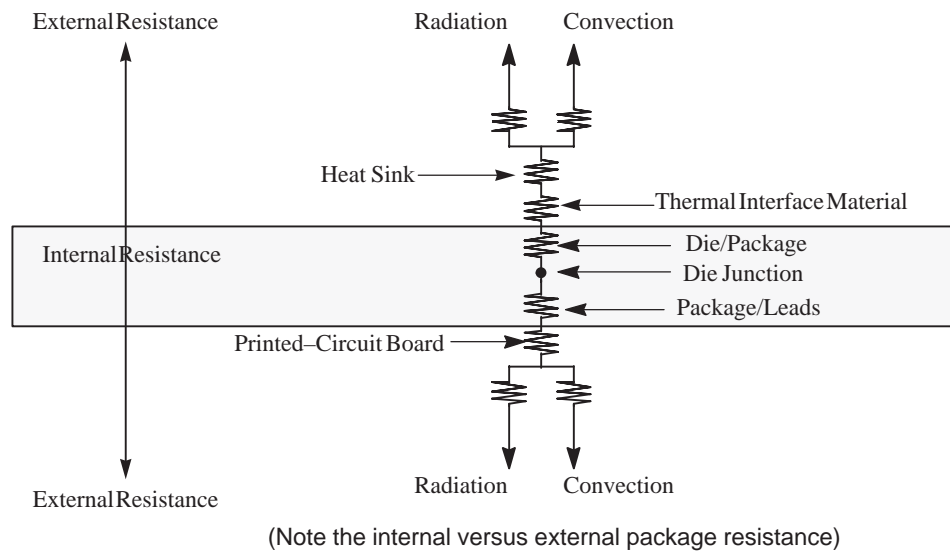


Figure 6 : C4 Package with Heat Sink Mounted to a Printed-Circuit Board

3.4.2. Thermal management assistance

The PC755B incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). Specifications for the thermal sensor portion of the TAU are found in Table 7. More information on the use of this feature is given in the Motorola PC755B RISC Microprocessor User's manual.

Table 7. Thermal Sensor Specifications				
At recommended operating conditions (See Table 5)				
Characteristic	Min	Max	Unit	Notes
Temperature range	0	127	°C	1
Comparator settling time	20	—	s	2,3
Resolution	4	—	°C	3
Accuracy	-12	+12	°C	3
Notes: 1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Motorola Application Note AN1800/D, "Programming the Thermal Assist Unit in the PC750 Microprocessor". 2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR. 3. Guaranteed by design and characterization.				

3.4.3. Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (BGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design—the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 7. This spring force should not exceed 5.5 pounds of force.

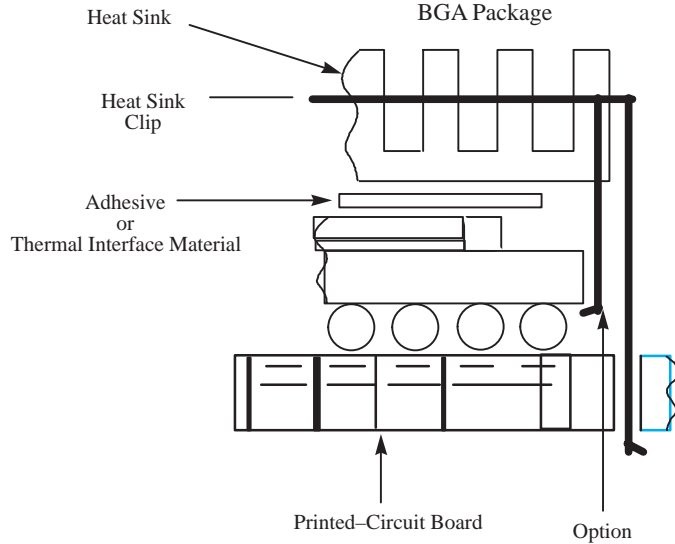


Figure 7 : Package Exploded Cross-Sectional View with Several Heat Sink Options

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.4.3.1. Adhesives and Thermal Interface Materials

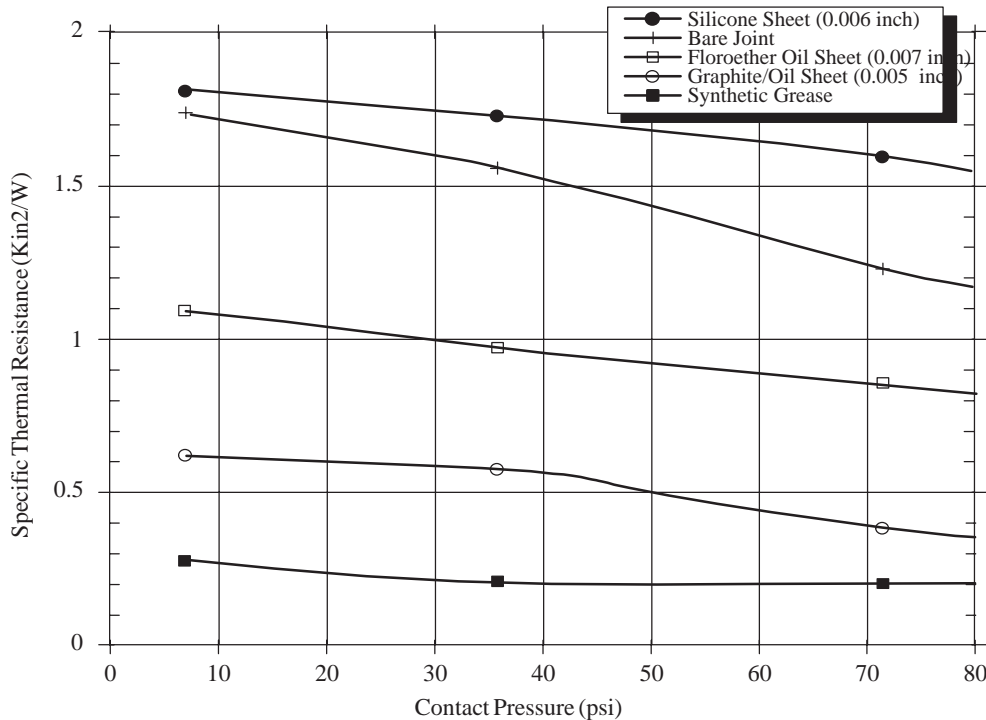


Figure 8 : Thermal Performance of Select Thermal Interface Material

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 8 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 7). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure.

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements.

3.4.3.2. Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) * P_d$$

Where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the adhesive or interface material thermal resistance

θ_{sa} is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 5. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30 to 40 °C. The air temperature rise within a cabinet (T_r) may be in the range of 5 to 10 °C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1 °C/W. Assuming a T_a of 30 °C, a T_r of 5 °C, a CBGA package $\theta_{jc} = 0.03$, and a power consumption (P_d) of 5.0 watts, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30\text{ °C} + 5\text{ °C} + (0.03\text{ °C/W} + 1.0\text{ °C/W} + \theta_{sa}) * 5.0\text{ W}$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 9.

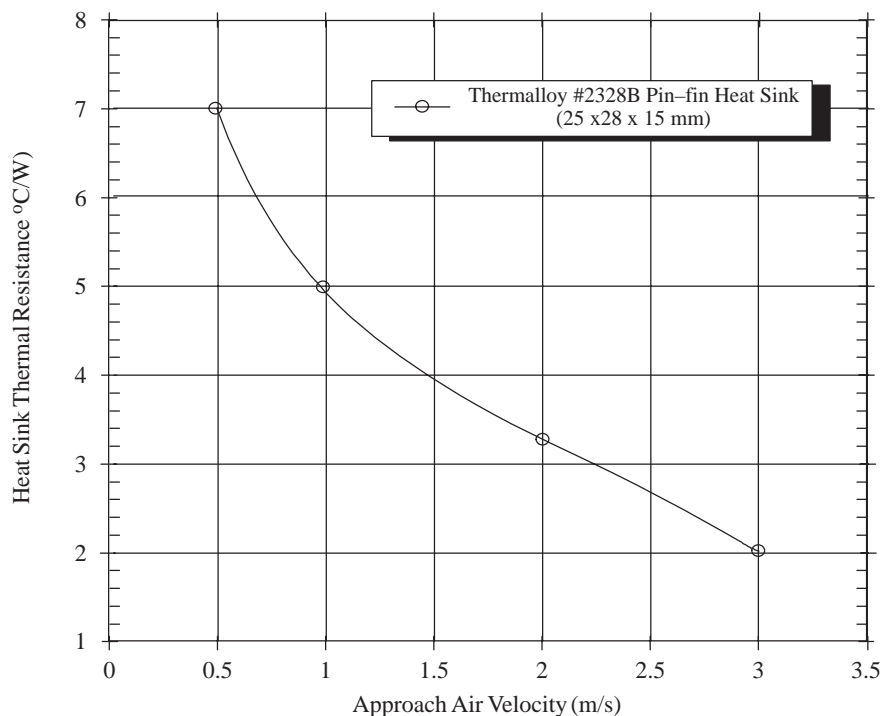


Figure 9 : Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7 °C/W, thus

$$T_j = 30\text{ °C} + 5\text{ °C} + (0.03\text{ °C/W} + 1.0\text{ °C/W} + 7\text{ °C/W}) * 5.0\text{ W},$$

resulting in a die-junction temperature of approximately 81 °C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering, and Aavid Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several "compact" thermal-package models are available within FLOTHERM®. These are available upon request.

3.5. Power consideration

3.5.1. Power management

The PC755B provides four power modes, selectable by setting the appropriate control bits in the MSR and HIDO registers. The four power modes are as follows :

- **Full-power:** This is the default power state of the PC755B. The PC755B is fully powered and the internal functional units are operating at the full processor clock speed. If the dynamic power management mode is enabled, functional units that are idle will automatically enter a low-power state without affecting performance, software execution, or external hardware.
- **Doze:** All the functional units of the PC755B are disabled except for the time base/decrementer registers and the bus snooping logic. When the processor is in doze mode, an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or machine check brings the PC755B into the full-power state. The PC755B in doze mode maintains the PLL in a fully powered state and locked to the system external clock input (SYSCLK) so a transition to the full-power state takes only a few processor clock cycles.
- **Nap:** The nap mode further reduces power consumption by disabling bus snooping, leaving only the time base register and the PLL in a powered state. The PC755B returns to the full-power state upon receipt of an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or a machine check input (\overline{MCP}). A return to full-power state from a nap state takes only a few processor clock cycles. When the processor is in nap mode, if \overline{QACK} is negated, the processor is put in doze mode to support snooping.
- **Sleep:** Sleep mode minimizes power consumption by disabling all internal functional units, after which external system logic may disable the PPL and SUSCLK. Returning the PC755B to the full-power state requires the enabling of the PPL and SYSCLK, followed by the assertion of an external asynchronous interrupt, a system management interrupt, a hard or soft reset, or a machine check input (\overline{MCP}) signal after the time required to relock the PPL.

3.5.2. Power dissipation

Table 8. Power Consumption for PC755B					
	Processor (CPU) Frequency			Unit	Notes
	300MHz	350MHz	400MHz		
Full-On Mode					
Typical	3.3	3.9	4.4	W	1, 3
Maximum	4.9	5.7	6.4	W	1, 2
Doze Mode					
Maximum	1.8	2.0	2.3	W	1, 2
Nap Mode					
Maximum	500	510	530	mW	1, 2
Sleep Mode					
Maximum	460	470	470	mW	1, 2
Sleep Mode—PLL and DLL Disabled					
Typical	340	340	340	mW	1, 3
Maximum	430	430	430	mW	1, 2
Notes: 1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mW and L2AVdd = 15 mW. 2. Maximum power is measured at Vdd = 2.1V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy. 3. Typical power is an average value measured at Vdd = AVdd = L2AVdd = 2.0V, OVdd = L2OVdd = 3.3V in a system executing typical applications and benchmark sequences.					

4. ELECTRICAL CHARACTERISTICS

4.1. Static characteristics

Table 9. DC Electrical Specifications

At recommended operating conditions (See Table 5)

Characteristic	Nominal Bus Voltage ¹	Symbol	Min	Max		Unit	Notes
Input high voltage (all inputs except SYSCLK)	1.8/2.0	V_{IH}	$0.65 * (L2)OVdd$	$(L2)OVdd + 0.15$		V	2,3
	3.3	V_{IH}	2.0	$(L2)OVdd + 0.3$		V	2,3
Input low voltage (all inputs except SYSCLK)	1.8/2.0	V_{IL}	-0.3	$0.35 * (L2)OVdd$		V	2
	3.3	V_{IL}	-0.3	0.8		V	
SYSCLK input high voltage	1.8/2.0	KV_{IH}	1.5	$OVdd + 0.3$		V	
	3.3	KV_{IH}	2.4	$OVdd + 0.3$		V	
SYSCLK input low voltage	1.8/2.0	KV_{IL}	-0.3	0.2		V	
	3.3	KV_{IL}	-0.3	0.4		V	
Input leakage current, $V_{in} = L2OVdd/OVdd$		I_{in}	—	10		μA	2,3
Hi-Z (off-state) leakage current, $V_{in} = L2OVdd/OVdd$		I_{TSI}	—	10		μA	2,3,5
Output high voltage, $I_{OH} = -6 \text{ mA}$	1.8/2.0	V_{OH}	$(L2)OVdd - 0.45$	—		V	
	3.3	V_{OH}	2.4	—		V	
Output low voltage, $I_{OL} = 6 \text{ mA}$	1.8/2.0	V_{OL}	—	0.45		V	
	3.3	V_{OL}	—	0.4		V	
Capacitance, $V_{in} = 0 \text{ V}$, $f = 1 \text{ MHz}$		C_{in}	—	5.0		pF	3,4

Notes:

1. Nominal voltages; See Table 5 for recommended operating conditions.
2. For processor bus signals, the reference is OVdd while L2OVdd is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OVdd and Vdd, or both OVdd and Vdd must vary in the same direction (for example, both OVdd and Vdd vary by either +5% or -5%).

4.2. Dynamic characteristics

After fabrication, parts are sorted by maximum processor core frequency as shown in Section 4.2.1., "Clock AC Specifications" and tested for conformance to the AC specifications for that frequency. These specifications are for 275, 300, 333 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0–3] signals. Parts are sold by maximum processor core frequency.

4.2.1. Clock AC Specifications

Table 10 provides the clock AC timing specifications as defined in Table 3.

Table 10. Clock AC Timing Specifications									
At recommended operating conditions (See Table 5)									
Characteristic	Symbol	Maximum Processor Core Frequency						Unit	Notes
		300 MHz		350 MHz		400 MHz			
		Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	200	300	200	350	200	400	MHz	1
VCO frequency	f_{VCO}	400	600	400	700	400	800	MHz	1
SYSCLK frequency	f_{SYSCLK}	25	100	25	100	25	100	MHz	1
SYSCLK cycle time	t_{SYSCLK}	10	40	10	40	10	40	ns	
SYSCLK rise and fall time	$t_{KR} \& t_{KF}$	—	2.0	—	2.0	—	2.0	ns	2
	$t_{KR} \& t_{KF}$	—	1.0	—	1.0	—	1.0	ns	2
SYSCLK duty cycle measured at OVdd/2	$t_{KHL}/t_{SYSC LK}$	40	60	40	60	40	60	%	3
SYSCLK jitter		—	150	—	150	—	150	ps	3,4
Internal PLL relock time		—	100	—	100	—	100	μs	3,5
Notes: <ol style="list-style-type: none"> 1. Caution: The SYSCLK frequency and PLL_CFG[0–3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0–3] signal description in Table 17," for valid PLL_CFG[0–3] settings 2. Rise and fall times measurements are now specified in terms of slew rates, rather than time to account for selectable I/O bus interface levels. The minimum slew rate of 1v/ns is equivalent to a 2ns maximum rise/fall time measured at 0.4v and 2.4v or a rise/fall time of 1ns measured at 0.4v to 1.4v. 3. Timing is guaranteed by design and characterization. 4. This represents total input jitter - short term and long term combined and is guaranteed by design. 5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence. 									

Figure 10 provides the SYSCLK input timing diagram.

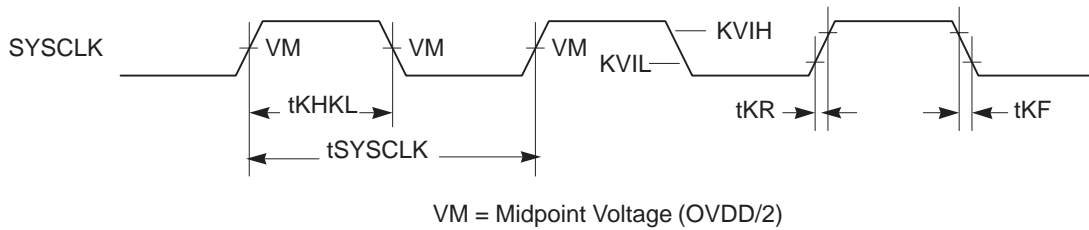


Figure 10 : SYSCLK Input Timing Diagram

4.2.2. Processor Bus AC Specifications

Table 11 provides the processor bus AC timing specifications for the PC755B as defined in Figure 11 and Figure 13. Timing specifications for the L2 bus are provided in Section 4.2.1., "L2 Clock AC Specifications."

Table 11. Processor Bus Mode Selection AC Timing Specifications¹					
At Vdd=AVdd=2.0V 100mV; -55 ≤ Tj ≤ +125 °C, OVdd = 3.3V 165mV and OVdd = 1.8V ± 100mV and OVdd = 2.0V 100mV					
Parameter	Symbols ²	300, 350, 400 MHz		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{\text{HRESET}}$	t _{MVRH}	8	—	t _{sysclk}	3,4,5,6,7
$\overline{\text{HRESET}}$ to mode select input hold	t _{MXRH}	∞	—	ns	3,4,6,7,8
Notes: <ol style="list-style-type: none"> All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50 ohm load (See Figure 11). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. The symbology used for timing specifications herein follows the pattern of t_{(signal)(state)(reference)(state)} for inputs and t_{(reference)(state)(signal)(state)} for outputs. For example, t_{VKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high(H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high(H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) - note the position of the reference and its state for inputs -and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX). For additional explanation of AC timing specifications in Motorola PowerPC microprocessors, see the application note "Understanding AC Timing Specifications for PowerPC Microprocessors." The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 11). This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0-3] Guaranteed by design and characterization. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once $\overline{\text{HRESET}}$ is negated the states of the bus mode selection pins must remain stable. 					

Figure 11 provides the mode select input timing diagram for the PC755B.

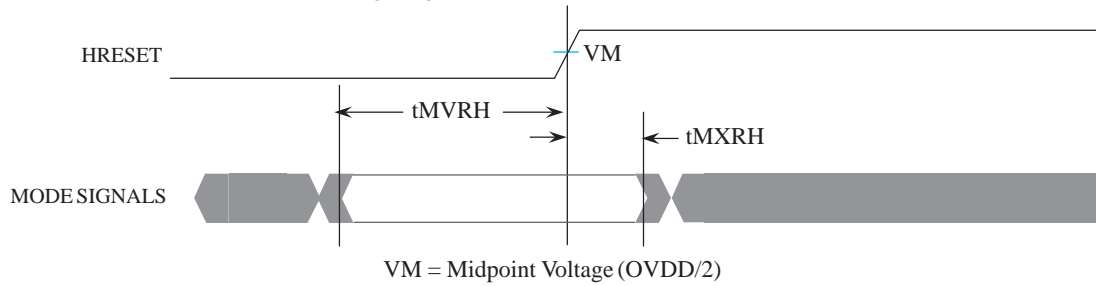


Figure 11 : Mode Input Timing Diagram

Figure 12 provides the AC test load for the PC755B.

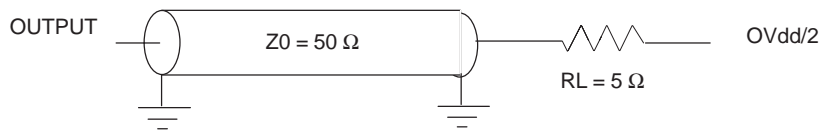


Figure 12 : AC Test Load

Table 12. Processor Bus AC Timing Specifications

At Vdd=AVdd=2.0V 100mV; $-55 \leq T_j \leq +125^\circ\text{C}$, OVdd = 3.3V $\leq 165\text{mV}$ and OVdd = 1.8V 100mV and OVdd = 2.0V 100mV

Parameter	Symbols	300, 350, 400 MHz		Unit	Notes
		Min	Max		
Setup Times: All Inputs	$t_{V\text{KH}}$	2.5	—	ns	
Input Hold Times: All Inputs	$t_{X\text{KH}}$	0.6	—	ns	
Valid Times: All Outputs	$t_{K\text{HOV}}$	—	4.5	ns	
Output Hold Times: All Outputs	$t_{K\text{HOX}}$	1.0	—	ns	
SYSClk to Output Enable	$t_{K\text{HOE}}$	0.5	—	ns	4
SYSClk to Output High Impedance (all except $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	$t_{K\text{HOZ}}$	—	6.0	ns	4
SYSClk to $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ High Impedance after precharge	$t_{K\text{HABPZ}}$	—	1.0	t_{sysclk}	1,2,4
Maximum Delay to $\overline{\text{ARTRY}}$ Precharge	$t_{K\text{HARP}}$	—	1	t_{sysclk}	1,3,4
SYSClk to $\overline{\text{ARTRY}}$ High Impedance After Precharge	$t_{K\text{HARPZ}}$	—	2	t_{sysclk}	1,3,4

Notes:

- t_{sysclk} is the period of the external clock (SYSClk) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSClk to compute the actual time duration (in nanoseconds) of the parameter in question.
- Per the 60x bus protocol, $\overline{\text{TS}}$, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 13. The nominal precharge width for $\overline{\text{TS}}$, $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is $0.5 \cdot t_{\text{sysclk}}$, i.e. less than the minimum t_{sysclk} period, to ensure that another master asserting $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
- Per the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is $1.0 \cdot t_{\text{sysclk}}$, i.e. it should be high-Z as shown in Figure 12 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z and precharge behavior is guaranteed by design.
- Guaranteed by design and characterization.



The timing diagram illustrates the relationship between several signals and their timing parameters:

- SYSCLK**: System clock signal, shown as a periodic square wave.
- VM**: Midpoint Voltage, indicated by vertical lines at the midpoint of each SYSCLK cycle.
- ALL INPUTS**: Represented by a signal that is high during the VM period and low otherwise. The transition time from high to low is labeled t_{IVKH} .
- ALL OUTPUTS (Except TS, ABB, ARTRY, DBB)**: Represented by a signal that is high during the VM period and low otherwise. The transition time from high to low is labeled t_{IXKH} .
- TS, ABB, DBB**: These signals are high during the VM period and low otherwise. The transition time from high to low is labeled t_{KHOE} .
- ARTRY**: This signal is high during the VM period and low otherwise. The transition time from high to low is labeled t_{KHOV} .
- Timing Parameters**:
 - t_{KHOV} : Time from the start of the VM period to the output signal becoming high.
 - t_{KHOX} : Time from the end of the VM period to the output signal becoming low.
 - t_{KHOZ} : Time from the end of the VM period to the output signal becoming high.
 - t_{KHABPZ} : Time from the start of the VM period to the output signal becoming high.
 - t_{KHARPZ} : Time from the end of the VM period to the output signal becoming low.
 - t_{KHARP} : Time from the end of the VM period to the output signal becoming high.
 - t_{KHOPZ} : Time from the end of the VM period to the output signal becoming low.

VM = Midpoint Voltage ($O_{VDD}/2$ or $V_{in}/2$)

4.2.3. L2 Clock AC Specifications

The minimum L2CLK frequency of Table 13 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase aligned with the PC755B core clock at the SRAMs.

Motorola is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 13. Therefore functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater. Functionality of core-to-L2 divisors of 1 or 1.5 is verified at less than maximum rated frequencies.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the PC755B to synchronize L2CLKOUT at the SRAM with the processor's internal clock. L2CLKOUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Motorola Application Note AN179/D "PowerPC™ Backside L2 Timing Analysis for the PCB Design Engineer."

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Table 13. L2CLK Output AC Timing SpecificationAt V_{dd}=AV_{dd}=2.0V 100mV; -55 ≤ T_j ≤ +125 °C, OV_{dd} = 3.3V 165mV and OV_{dd} = 1.8V 100mV and OV_{dd} = 2.0V 100mV

Parameter	Symbol	300,350,400 MHz		Unit	Notes
		Min	Max		
L2CLK frequency	f L2CLK	80	400	MHz	1,4
L2CLK cycle time	t L2CLK	2,5	12.5	ns	
L2CLK duty cycle	tCHCL/tL2CLK	50		%	2,7
Internal DLL-relock time		640	—	L2CLK	3,7
DLL capture window		0	10	ns	5,7
L2CLKOUT output-to-output skew	t _{L2CSKW}		50	ps	6,7
L2CLKOUT output jitter			150	ps	6,7

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUT and L2SYNC_OUT pins. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2CLK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL re-lock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in nanoseconds. Re-lock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYCLK affects L2CLKOUT and the L2 address/data/control signals equally and therefore is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.
7. Guaranteed by design and characterization.

The L2CLK_OUT timing diagram is shown in Figure 14.

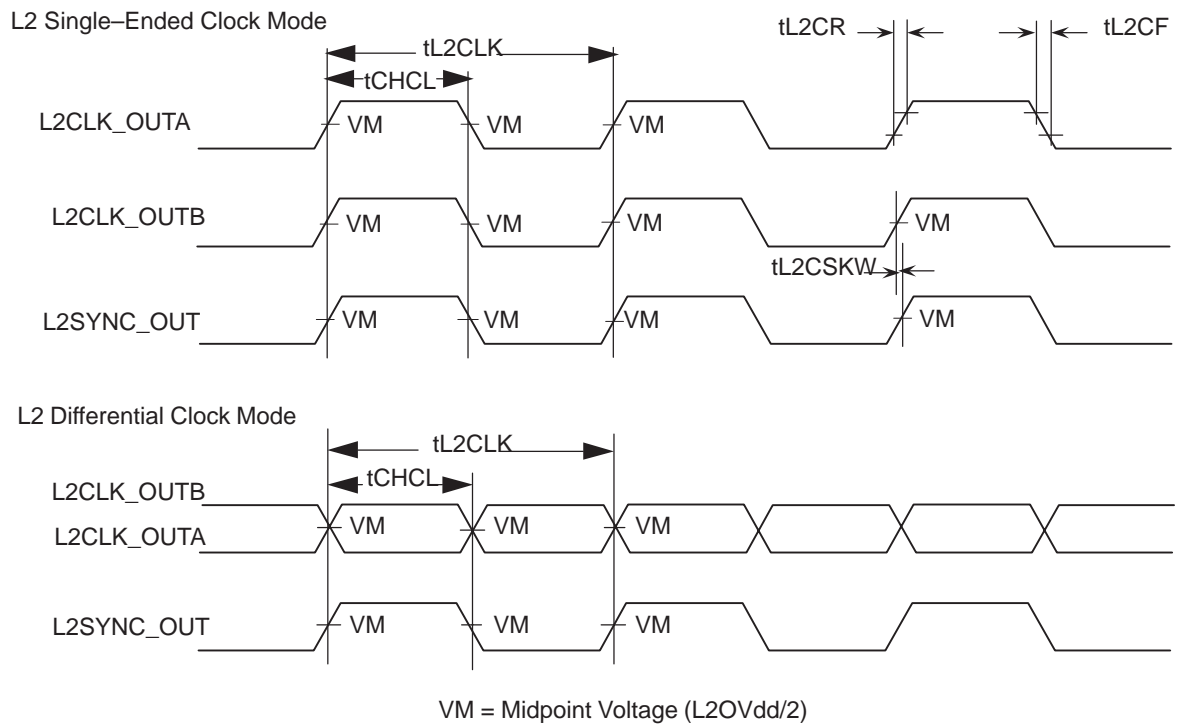


Figure 14 : L2CLK_OUT Output Timing Diagram

4.2.4. L2 Bus Input AC Specifications

Table 14 provides the L2 bus interface AC timing specifications for the PC755B as defined in Figure 15 and Figure 16 for the loading conditions described in Figure 17.

Table 14. L2 Bus Interface AC Timing Specifications									
At Vdd=AVdd=2.0V 100mV; -55 ≤ Tj ≤ +125 °C, OVdd = 3.3V 165mV and OVdd = 1.8V 100mV and OVdd = 2.0V 100mV									
Parameter	Symbol	300 MHz		350 MHz		400 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2SYNC_IN rise and fall time	tL2CR& tL2CF	—	1.0	—	1.0	—	1.0	ns	1
Setup Times: Data and parity	tDVL2CH	1.5	—	1.5	—	1.4	—	ns	2
Input Hold Times: Data and parity	tDXL2CH	0.5	—	0.5	—	0.5	—	ns	2
Valid Times: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	tL2CHOV	—	3.6 3.8 4.0 4.2	—	3.6 3.8 4.0 4.2	—	3.6 3.8 4.0 4.2	ns	3,4
Output Hold Times All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	tL2CHOX	0.5 0.7 0.9 1.1	— — — —	0.5 0.7 0.9 1.1	— — — —	0.5 0.7 0.9 1.1	— — — —	ns	3
L2SYNC_IN to high impedance: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	tL2CHOZ	— — — —	3.5 4.0 4.2 4.5	— — — —	3.5 4.0 4.2 4.5	— — — —	3.5 4.0 4.2 4.5	ns	3,5
Notes: 1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of L2OVdd. 2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 15). Input timings are measured at the pins. 3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 ohm load (See Figure 16). 4. he outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous burst RAMs, L2CR[14–15] = 01 or 10 is recommended. For pipelined late-write synchronous burst SRAMs, L2CR[14–15] = 11 is recommended. 5. Guaranteed by design and characterization.									

Figure 15 shows the L2 bus input timing diagrams for the PC755B.

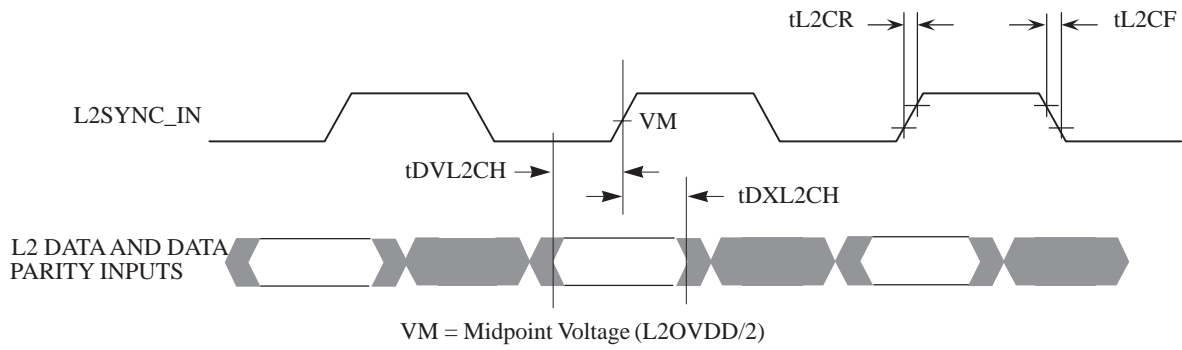


Figure 15 : L2 Bus Input Timing Diagrams

Figure 16 shows the L2 bus output timing diagrams for the PC755B.

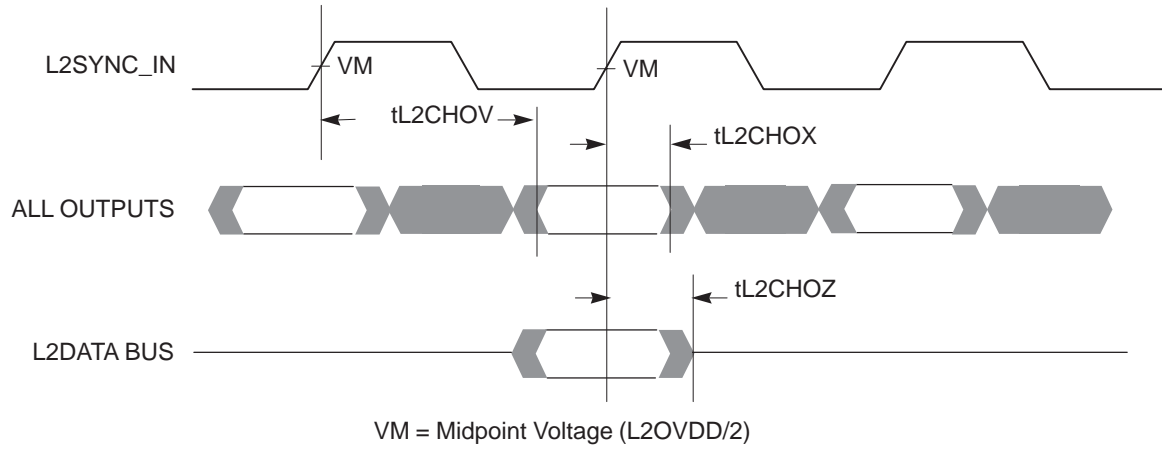


Figure 16 : L2 Bus Output Timing Diagrams

Figure 17 provides the AC test load for L2 interface of the PC755B.

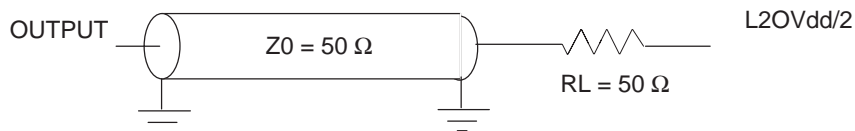


Figure 17 : AC Test Load for the L2 Interface

4.2.5. IEEE 1149.1 AC Timing Specifications

4.2.5.1. Timing Specifications

Table 15 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 18, Figure 19, Figure 20, and Figure 21.

Table 15. JTAG AC Timing Specifications (Independent of SYSCLK)¹ At recommended operating conditions (See Table 5)					
Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	fTCLK	0	33.3	MHz	
TCK cycle time	tTCLK	30	—	ns	
TCK clock pulse width measured at 1.4V	tJHJL	15	—	ns	
TCK rise and fall times	tJR & tJF	0	2	ns	
$\overline{\text{TRST}}$ assert time	tTRST	25	—	ns	2
Input Setup Times:				ns	
Boundary-scan data TMS, TDI	tDVJH tIVJH	4 0	— —		3
Input Hold Times:				ns	
Boundary-scan data TMS, TDI	tDXJH tIXJH	15 12	— —		3
Valid Times:				ns	
Boundary-scan data TDO	tJLDV tJLOV	— —	4 4		4
Output Hold Times:				ns	
Boundary-scan data TDO	tJLDH tJLOH	20 12	— —		4
TCK to output high impedance:				ns	
Boundary-scan data TDO	tJLDZ tJLOZ	3 3	19 9		4,5
Notes: 1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 ohm load (See Figure 18). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system. 2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only. 3. Non-JTAG signal input timing with respect to TCK. 4. Non-JTAG signal output timing with respect to TCK. 5. Guaranteed by design and characterization.					

Figure 18 provides the AC test load for TDO and the boundary-scan outputs of the PC755B.

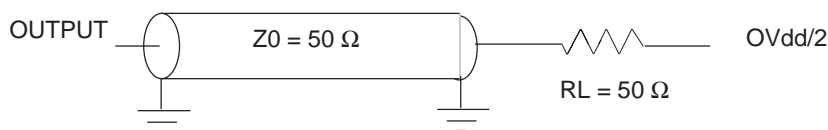


Figure 18 : ALTERNATE AC Test Load for the JTAG Interface

Figure 19 provides the JTAG clock input timing diagram.

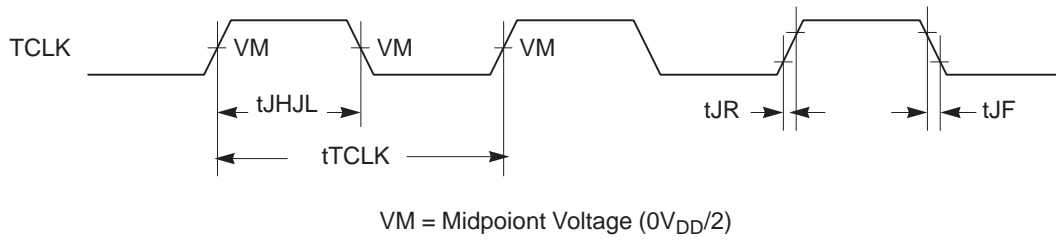


Figure 19 : JTAG Clock Input Timing Diagram

Figure 20 provides the $\overline{\text{TRST}}$ timing diagram.

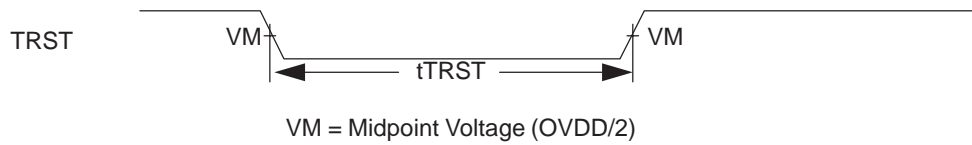


Figure 20 : $\overline{\text{TRST}}$ Timing Diagram

Figure 21 provides the boundary-scan timing diagram.

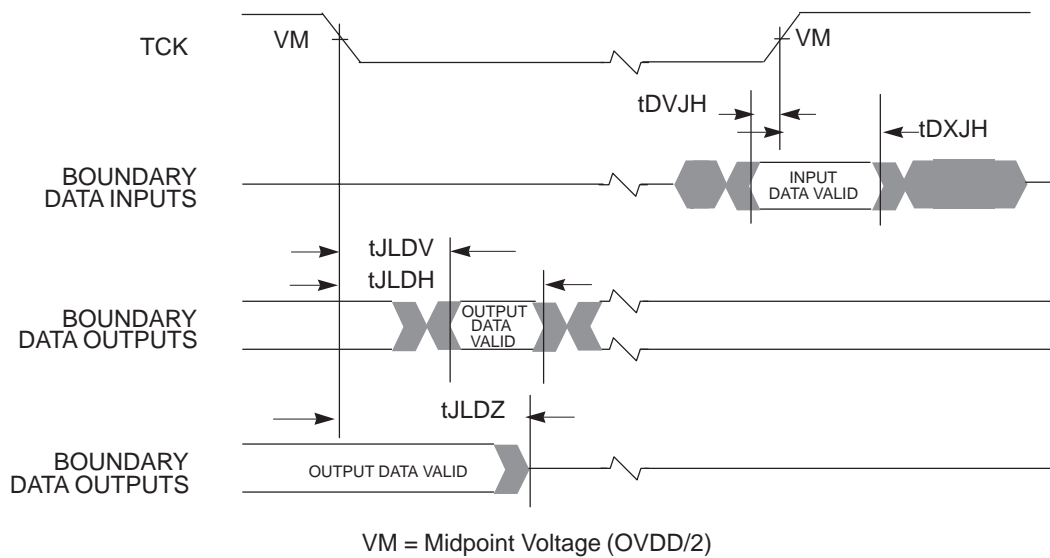


Figure 21 : Boundary-Scan Timing Diagram

Figure 22 provides the test access port timing diagram.

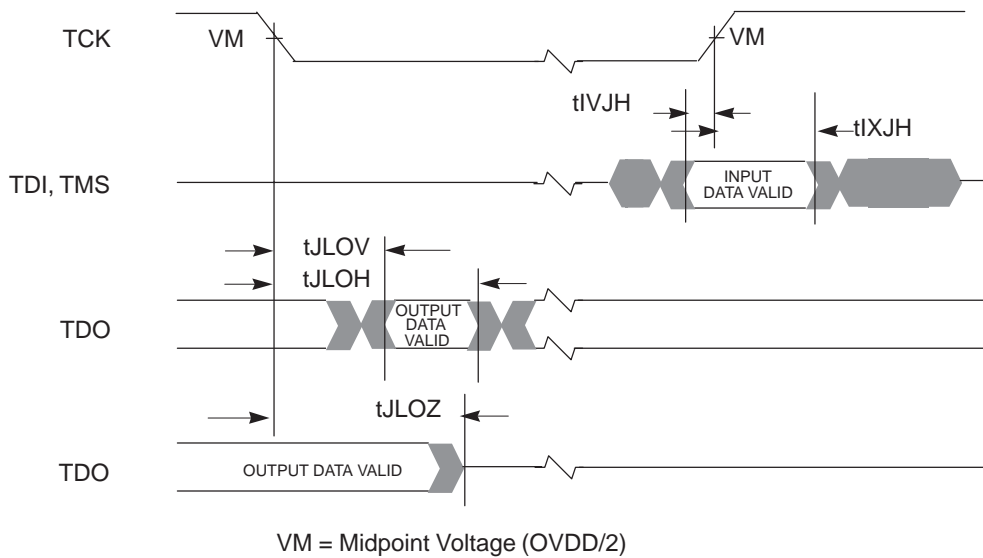


Figure 22 : Test Access Port Timing Diagram

4.2.5.2. JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification but is provided on all PowerPC implementations. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Since the JTAG interface is also used for accessing the common on-chip processor (COP) function of PowerPC processors, simply tying $\overline{\text{TRST}}$ to HRESET isn't practical.

The common on-chip processor (COP) function of PowerPC processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 23 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while insuring that the target can drive $\overline{\text{HRESET}}$ as well. The pull-down resistor on $\overline{\text{TRST}}$ ensures that the JTAG scan chain is initialized during power-on if a JTAG interface cable is not attached; if it is, it is responsible for driving $\overline{\text{TRST}}$ when needed.

Figure 23 shows the suggested $\overline{\text{TRST}}$ connection.

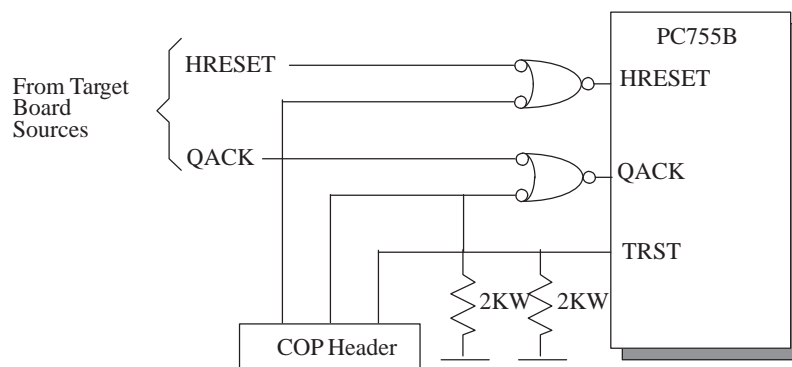


Figure 23 : Suggested TRST Connection

The COP header shown in Figure 24 adds many benefits—breakpoints, watchpoints, register and memory examination/modification and other standard debugger features are possible through this interface – and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

System design information

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a "Berg" header). The connector typically has pin 14 removed as a connector key.

Figure 24 shows the COP connector diagram.

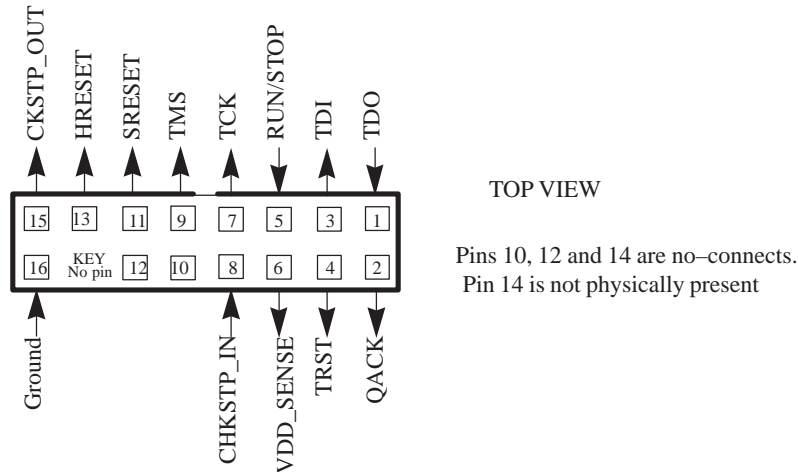


Figure 24 : COP Connector Diagram

There is no standardized way to number the COP header shown in Figure 24; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin one (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 24 is common to all known emulators.

The \overline{QACK} signal shown in Table 15 is usually hooked up to the PCI bridge chip in a system and is an input to the PC755B informing it that it can go into the quiescent state. Under normal operation this occurs during a low power mode selection. In order for COP to work the PC755B must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. To preserve correct power down operation, \overline{QACK} should be merged so that it also can be driven by the PCI bridge.

Table 16 shows the pin definitions.

Table 16. COP Pin Definitions			
Pins	Signal	Connection	Special Notes
1	TDO	TDO	
2	\overline{QACK}	\overline{QACK}	Add 2K pulldown to ground. Must be merged with on-board \overline{QACK} , if any.
3	TDI	TDI	
4	\overline{TRST}	\overline{TRST}	Add 2K pulldown to ground. Must be merged with on-board \overline{TRST} , if any. See Figure 23.
5	$\overline{RUN/STOP}$	No Connect	Used on 604e; leave no-connect for all other processors.
6	VDD_SENSE	VDD	Add 2K pullup to OVDD (for short circuit limiting protection only).
7	TCK	TCK	
8	$\overline{CKSTP_IN}$	$\overline{CKSTP_IN}$	Optional. Add 10K pullup to OVDD. Used on several emulator products. Useful for checkstopping the processor from a logic analyzer or other external trigger.
9	TMS	TMS	
10	N/A		
11	\overline{SRESET}	\overline{SRESET}	Merge with on-board \overline{SRESET} , if any.
12	N/A		
13	\overline{HRESET}	\overline{HRESET}	Merge with on-board \overline{HRESET} .
14	N/A		Key location; pin should be removed.
15	$\overline{CKSTP_OUT}$	$\overline{CKSTP_OUT}$	Add 10K pullup to OVDD.
16	Ground	Digital Ground	

5. PREPARATION FOR DELIVERY

5.1. Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535 .

5.2. Certificate of compliance

TCS offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-PRF-883 and guarantiyng the parameters not tested at temperature extremes for the entire temperature range.

6. HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surfaces.
- Ground test equipment, tools and operator.
- Do not handle devices by the leads.
- Store devices in conductive foam or carriers.
- Avoid use of plastic, rubber, or silk in MOS areas.
- Maintain relative humidity above 50 percent if practical.
- For CI-CGA packages, use specific tray to take care of the highest heighth of the package compared with the normal CBGA.

7. PACKAGE MECHANICAL DATA

The following sections provide the package parameters and mechanical dimensions for the PC745B, 255 PBGA package as well as the PC755B, 360 CBGA and PBGA packages. While both the PC755B plastic and the ceramic packages are described here, both packages are not guaranteed to be available at the same time. All new designs should allow for either ceramic or plastic BGA packages for this device. For more information on designing a common footprint for both plastic and ceramic package types, please contact your local Motorola sales office.

7.1. Parameters for the PC745B

7.1.1. Package Parameters for the PC745B PBGA

The package parameters are as provided in the following list. The package type is 21 x 21 mm, 255-lead plastic ball grid array (PBGA)

Package outline	21 x 21 mm
Interconnects	255 (16 x 16 ball array - 1
Pitch	1.27 mm (50 mil)
Minimum module height	2.25 mm
Maximum module height	2.80 mm
Ball diameter (typical)	0.75 mm (29.5 mil)

7.1.2. Mechanical Dimensions of the PC745B PBGA package

Figure 25 provides the mechanical dimensions and bottom surface nomenclature of the PC745B, 255 PBGA package.

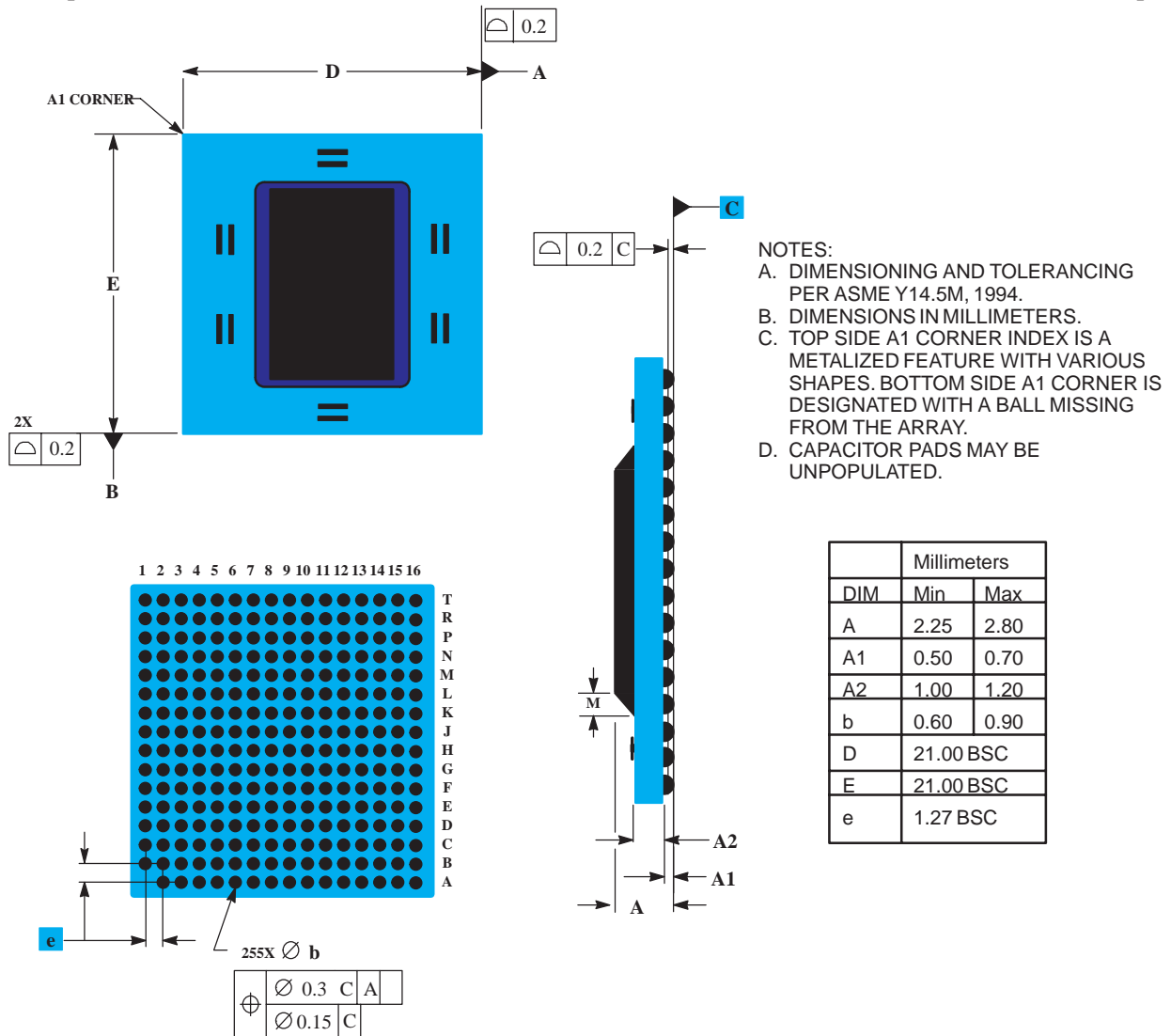


Figure 25 : Mechanical Dimensions and Bottom Surface Nomenclature of the PC745B PBGA

7.2. Parameters for the PC755B PBGA

7.2.1. Package parameter for the PC755B PBGA

The package parameters are as provided in the following list. The package type is 25 x 25 mm, 360-lead plastic ball grid array (PBGA).

Package outline	25 x 25 mm
Interconnects	360 (19 x 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.22 mm
Maximum module height	2.77 mm
Ball diameter	0.75 mm (29.5 mil)

7.2.2. Mechanical Dimensions of the PC755B PBGA

Figure 26 provides the mechanical dimensions and bottom surface nomenclature of the PC755B, 360 PBGA package.

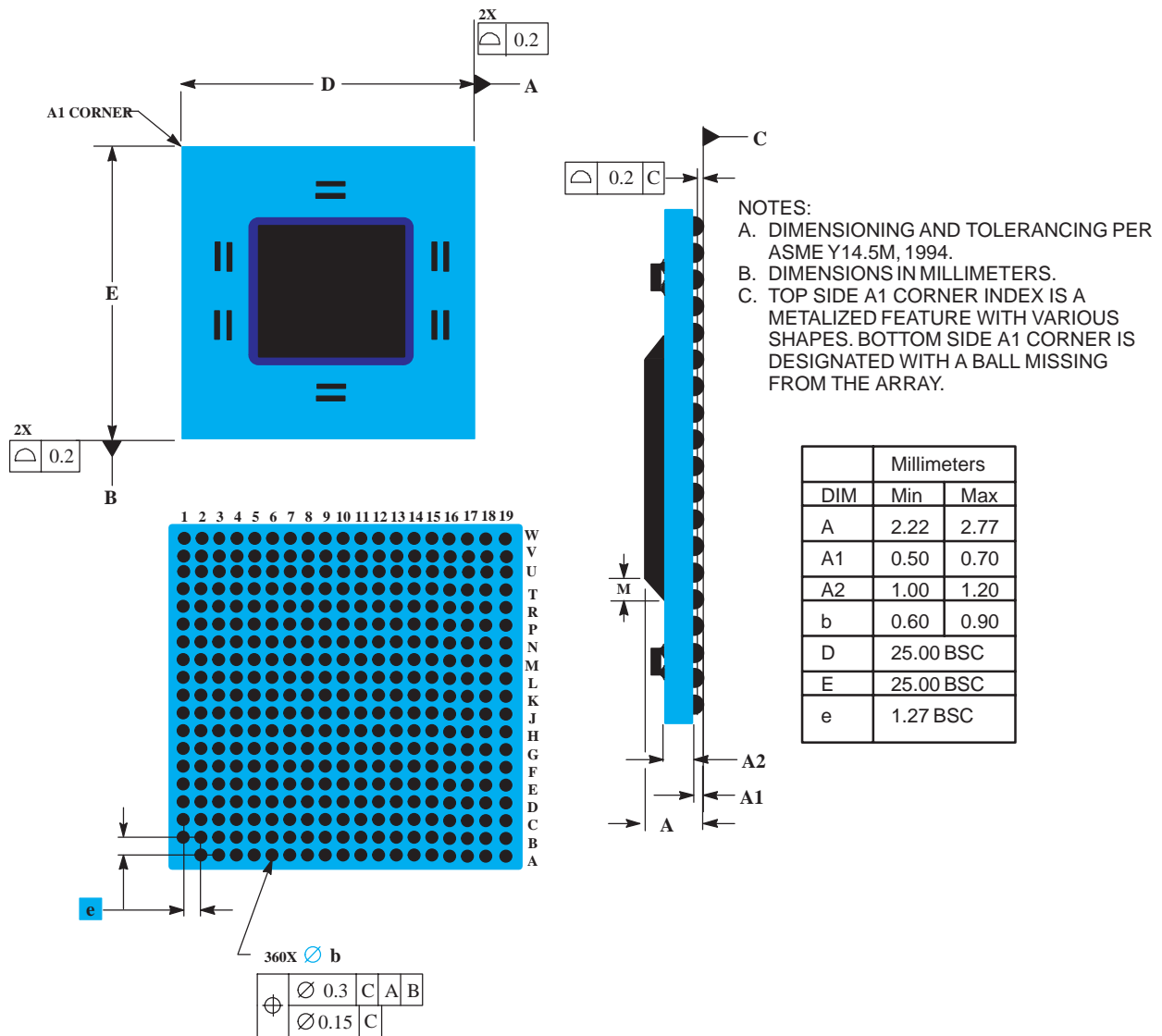


Figure 26 : Mechanical Dimensions and Bottom Surface Nomenclature of the PC755B PBGA

8. CLOCK RELATIONSHIPS CHOICE

The PC755B's PLL is configured by the PLL_CFG[0–3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC755B is shown in Figure 27 for example frequencies.

Table 17. PC755B Microprocessor PLL Configuration

PLL_CFG [0–3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz
0100	2x	2x	—	—	—	—	—	200 (400)
1000	3x	2x	—	—	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	—	—	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	—	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)
0111	4.5x	2x	—	225 (450)	300 (600)	338 (675)	360 (720)	—
1011	5x	2x	—	250 (500)	333 (666)	375 (750)	400 (800)	—
1001	5.5x	2x	—	275 (550)	366 (733)	—	—	—
1101	6x	2x	200 (400)	300 (600)	400 (800)	—	—	—
0101	6.5x	2x	216 (433)	325 (650)	—	—	—	—
0010	7x	2x	233 (466)	350 (700)	—	—	—	—
0001	7.5x	2x	250 (500)	375 (750)	—	—	—	—
1100	8x	2x	266 (533)	400 (800)	—	—	—	—
0110	10x	2x	333 (666)	—	—	—	—	—
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					
1111	PLL off		PLL off, no core clocking occurs					

Notes:

1. PLL_CFG[0–3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC755B; see Section 4.2.1, “Clock AC Specifications,” for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the PC755B regardless of the SYSCLK input.

The PC755B generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the PC755B. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the PC755B to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the PC755B core, and the phase adjustment range that the L2 DLL supports. Figure 18 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 80MHz.

Table 18. Sample Core-to-L2 Frequencies					
Core Frequency in MHz	1	1.5	2	2.5	3
250	250	166	125	100	83
266	266	177	133	106	89
275	275	183	138	110	92
300	300	200	150	120	100
325	325	217	163	130	108
333	333	222	167	133	111
350	350	233	175	140	117
366	366	244	183	146	122
375	375	250	188	150	125
400	400	266	200	160	133
Note : The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the PC755B; see Section 4.2.1., " L2 Clock AC Specifications," for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.					

9. SYSTEM DESIGN INFORMATION

9.1. PLL Power Supply Filtering

The AVdd and L2AVdd power signals are provided on the PC755B to provide power to the clock generation phase-locked loop and L2 cache delay-locked loop respectively. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered of any noise in the 500kHz to 10MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 27 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

The circuit should be placed as close as possible to the AVdd pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the L2AVdd pin. It is often possible to route directly from the capacitors to the AVdd pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The L2AVdd pin may be more difficult to route but is proportionately less critical.

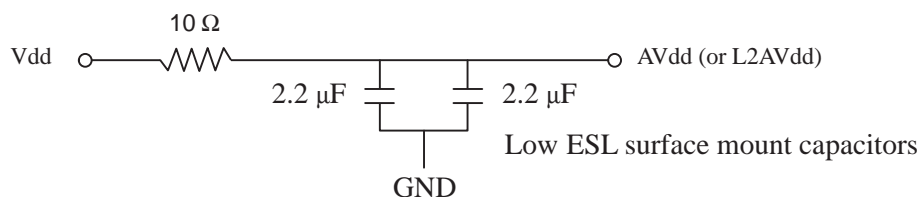


Figure 27 : PLL Power Supply Filter Circuit

9.2. Power Supply Voltage Sequencing

The notes in Figure 28 contain cautions about the sequencing of the external bus voltages and core voltage of the PC755B (when they are different). These cautions are necessary for the long term reliability of the part. If they are violated, the ESD (Electrostatic Discharge) protection diodes will be forward biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit of Figure 28 can be added to meet these requirements. The MUR420 Schottky diodes of Figure 28 control the maximum potential difference between the external bus and core power supplies on power-up and the 1N5820 diodes regulate the maximum potential difference on power-down.

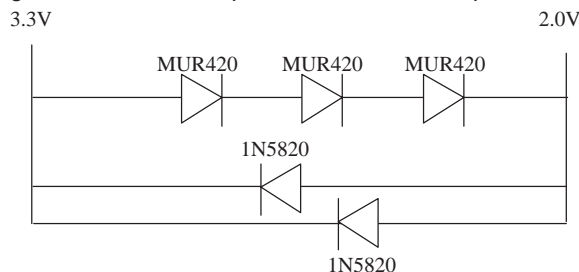


Figure 28 : Example Voltage Sequencing Circuit

9.3. Decoupling Recommendations

Due to the PC755B's dynamic power management feature, large address and data buses, and high operating frequencies, the PC755B can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC755B system, and the PC755B itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each Vdd, OVdd, and L2OVdd pin of the PC755B. It is also recommended that these decoupling capacitors receive their power from separate Vdd, (L2)OVdd and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 μ F or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd, L2OVdd, and OVdd planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100-330 μ F (AVX TPS tantalum or Sanyo OSCON).

9.4. Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OVdd. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, OVdd, L2OVdd, and GND pins of the PC755B.

9.5. Output Buffer DC Impedance

The PC755B 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0 , an external resistor is connected from the chip pad to (L2)OVdd or GND. Then, the value of each resistor is varied until the pad voltage is (L2)OVdd/2 (See Figure 29).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When Data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals (L2)OVdd/2. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals (L2)OVdd/2. R_P then becomes the resistance of the pull-up devices.

AUCUN LIEN describes the driver impedance measurement circuit described above.

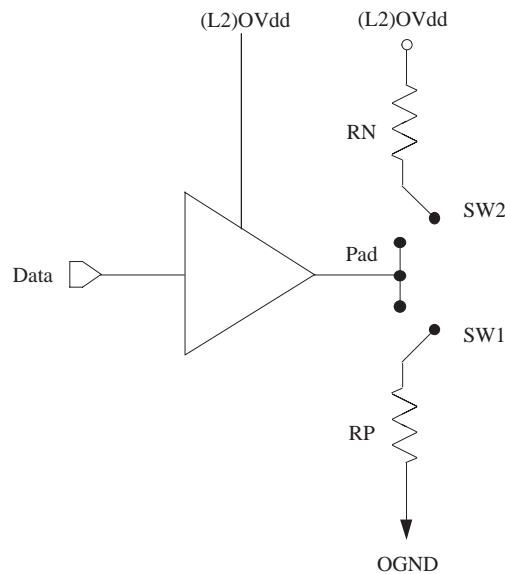


Figure 29 : Driver Impedance Measurement Circuit

Alternately, the following is another method to determine the output impedance of the PC755B. A voltage source, V_{force} , is connected to the output of the PC755B as in Figure 30. Data is held low, the voltage source is set to a value that is equal to (L2)OVdd/2 and the current sourced by V_{force} is measured. The voltage drop across the pulldown device, which is equal to (L2)OVdd/2, is divided by the measured current to determine the output impedance of the pulldown device, R_N . Similarly, the impedance of the pullup device is determined by dividing the voltage drop of the pullup, (L2)OVdd/2, by the current sunk by the pullup when the data is high and V_{force} is equal to (L2)OVdd/2. This method can be employed with either empirical data from a test set up or with data from simulation models, such as IBIS.

R_P and R_N are designed to be close to each other in value. Then $Z_0 = (R_P + R_N)/2$.

Figure 30 describes the alternate driver impedance measurement circuit.

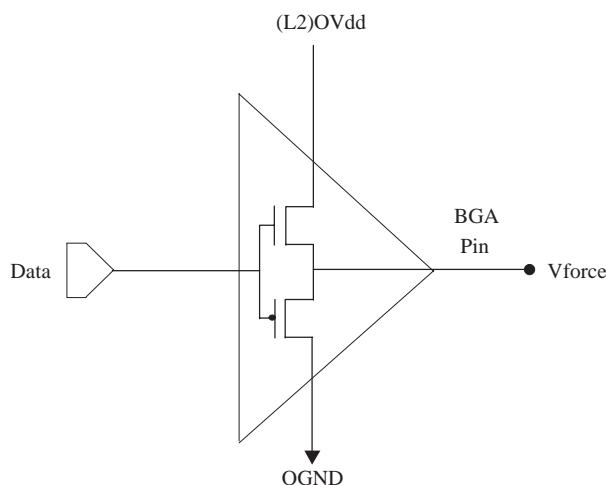


Figure 30 : Alternate Driver Impedance Measurement Curcuit

Table 19 summarizes the signal impedance results. The driver impedance values were characterized at 0 C, 65 C, and 105 C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 19. Impedance Characteristics Vdd = 2.0V, OVdd = 3.3V, Tc = 0 - 105 C				
Impedance	Processor bus	L2 bus	Symbol	Unit
RN	25-36	25-36	Z ₀	Ohms
RP	26-39	26-39	Z ₀	Ohms

9.6. Pull-up Resistor Requirements

The PC755B requires high-resistive (weak: 10 K Ω) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PC755B or other bus masters. These pins are \overline{TS} , \overline{ABB} , \overline{ARTRY} .

In addition, the PC755B has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7 K Ω –10 K Ω) if it is used by the system. This pin is $\overline{CKSTP_OUT}$.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may therefore float in the high-impedance state for relatively long periods of time. Since the PC755B must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PC755B or by other receivers in the system. It is recommended that these signals be pulled up through weak (10 K Ω) pull-up resistors by the system, or that they may be otherwise driven by the system during inactive periods of the bus. The snooped address and transfer attribute inputs are: A[0:31], AP[0:3], TT[0:4], \overline{TBST} and \overline{GBL} .

The data bus input receivers are normally turned off when no read operation is in progress and therefore do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pullups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31] and DP[0:7]

If 32-bit data bus mode is selected, the input receivers of the unused data and parity bits will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L2 interface does not normally require pull-up resistors.

10. DEFINITIONS

Datasheet status		Validity
Objective specification	This datasheet contains target and goal specification for discussion with customer and application validation.	Before design phase.
Target specification	This datasheet contains target or goal specification for product development.	Valid during the design phase.
Preliminary specification \propto site	This datasheet contains preliminary data. Additional data may be published later ; could include simulation result.	Valid before characterization phase.
Preliminary specification β site	This datasheet contains also characterization results.	Valid before the industrialization phase.
Product specification	This datasheet contains final product specification.	Valid for production purpose.
Limiting values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		

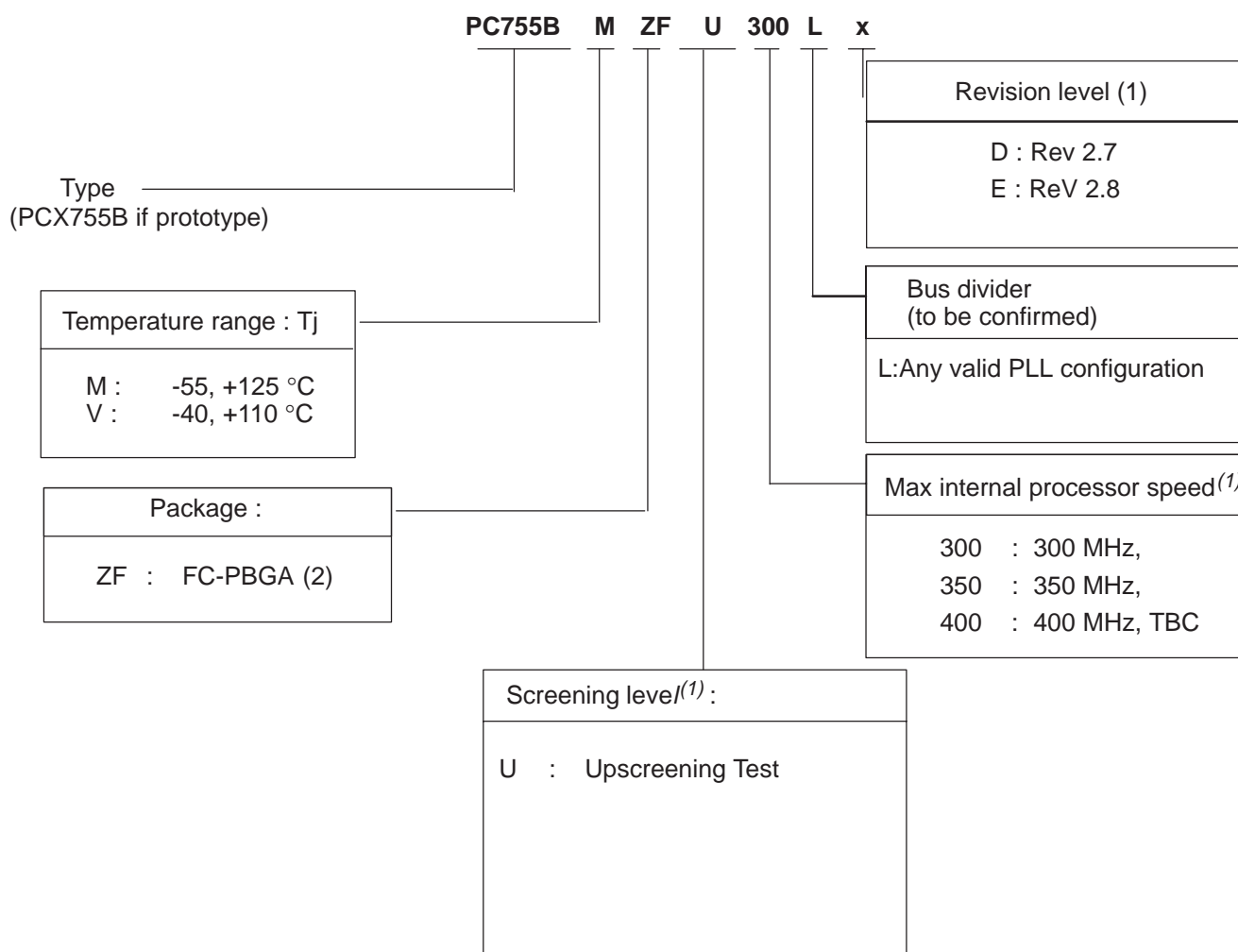
LIFE SUPPORT APPLICATIONS

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11. DIFFERENCES WITH COMMERCIAL PART

	Commercial part	Military part
Temperature range	Tj = 0 to 105°C	Tj = -55 to 125°C

12. ORDERING INFORMATION



(1) For availability of the different versions, contact your Atmel-Grenoble sale office

(2) FC-PBGA = PBGA with Flip Chip Assembly process

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