



PRELIMINARY

# 27256 256K (32K x 8) UV ERASABLE PROM

- Software Carrier Capability
- 250 ns Maximum Access Time
- Two-Line Control
- Intelligent Identifier™ Mode
  - Automated Programming Operations
- TTL Compatible
- Industry Standard Pinout . . . JEDEC Approved
- Low Power
  - 100 mA max. Active
  - 40 mA max. Standby
- Intelligent Programming™ Algorithm
  - Fastest EPROM Programming

The Intel 27256 is a 5V only, 262,144-bit ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM). Organized as 32K words by 8 bits, individual bytes are accessed in under 250ns. This is compatible with high performance microprocessors, such as the Intel 8MHz iAPX 186, allowing full speed operation without the addition of performance-degrading WAIT states. The 27256 is also directly compatible with Intel's 8051 family of microcontrollers.

The 27256 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the 27256's high density, cost effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems.

The 27256's large storage capability of 32K bytes enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27256 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time consuming disk accesses and downloads.

Several advanced features have been designed into the 27256 that allow for fast and reliable programming—the intelligent identifier™ mode and the intelligent Programming™ Algorithm. Programming equipment that takes advantage of these innovations will electronically identify the 27256 and then rapidly program it using an efficient programming method.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27256 is manufactured using Intel's advanced HMOS \*II-E technology.

\*HMOS is a patented process of Intel Corporation.

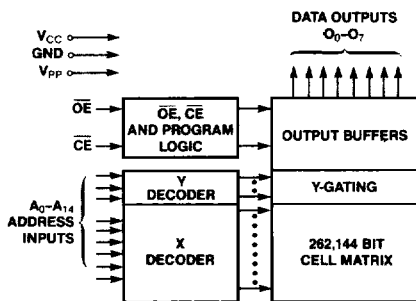
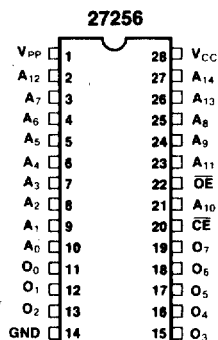


Figure 1. Block Diagram



PIN NAMES	
A <sub>0</sub> -A <sub>14</sub>	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
O <sub>0</sub> -O <sub>7</sub>	OUTPUTS

Figure 2. Pin Configuration

Intel Corporation Assumes No Responsibility for the Use of Any Circuitry Other Than Circuitry Embodied in an Intel Product. No Other Circuit Patent Licenses are Implied.

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6.25 V to -0.6V
Voltage on Pin 24 with Respect to Ground	+13.5V to -0.6V
V <sub>PP</sub> Supply Voltage with Respect to Ground	+14.0 V to -0.6V

*\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**D.C. AND A.C. OPERATING CONDITIONS DURING READ**

	27256	27256-3	27256-4	27256-25	27256-30	27256-45
Operating Temperature Range	0°C-70°C	0°C-70°C	0°C-70°C	0°C-70°C	0°C-70°C	0°C-70°C
V <sub>CC</sub> Power Supply <sup>1,2</sup>	5V ± 5%	5V ± 5%	5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

**READ OPERATION****D.C. CHARACTERISTICS**

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ. <sup>3</sup>	Max.		
I <sub>LI</sub>	Input Load Current			10	μA	V <sub>IN</sub> = 5.5V
I <sub>LO</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = 5.5V
I <sub>PP1</sub> <sup>2</sup>	V <sub>PP</sub> Current Read/Standby			5	mA	V <sub>PP</sub> = 5.5V
I <sub>CC1</sub> <sup>2</sup>	V <sub>CC</sub> Current Standby		20	40	mA	$\overline{CE} = V_{IH}$
I <sub>CC2</sub> <sup>2</sup>	V <sub>CC</sub> Current Active		45	100	mA	$\overline{CE} = \overline{OE} = V_{IL}$ V <sub>PP</sub> = V <sub>CC</sub>
V <sub>IL</sub>	Input Low Voltage	-1		+8	V	
V <sub>IH</sub>	Input High Voltage	2.0		V <sub>CC</sub> +1	V	
V <sub>OL</sub>	Output Low Voltage			.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -400 μA
V <sub>PP</sub> <sup>2</sup>	V <sub>PP</sub> Read Voltage	3.8		V <sub>CC</sub>	V	V <sub>CC</sub> = 5.0V ± 0.25V

## READ OPERATION

### A.C. CHARACTERISTICS

Symbol	Parameter	27256-25 & 27256 Limits		27256-30 & 27256-3 Limits		27256-45 & 27256-4 Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{ACC}$	Address to Output Delay		250		300		450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	$\overline{CE}$ to Output Delay		250		300		450	ns	$\overline{OE} = V_{IL}$
$t_{OE}$	$\overline{OE}$ to Output Delay		100		120		150	ns	$\overline{CE} = V_{IL}$
$t_{DF}^4$	$\overline{OE}$ High to Output Float	0	60	0	105	0	130	ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

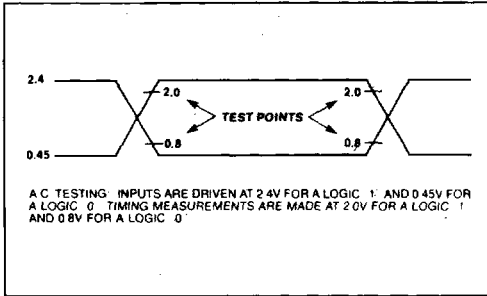
#### NOTES:

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- $V_{PP}$  may be connected directly to  $V_{CC}$  except during programming. The supply current would then be the sum of  $I_{CC}$  and  $I_{PP1}$ .
- Typical values are for  $t_A = 25^\circ\text{C}$  and nominal supply voltages.
- This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram on the following page.

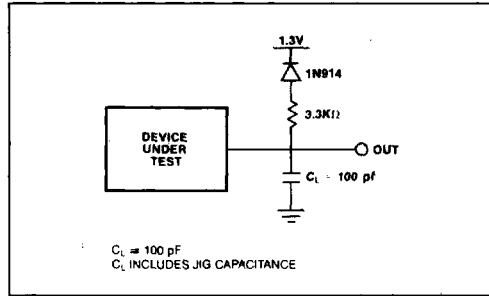
**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Symbol	Parameter	Typ. <sup>1</sup>	Max.	Unit	Conditions
$C_{IN}^2$	Input Capacitance	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

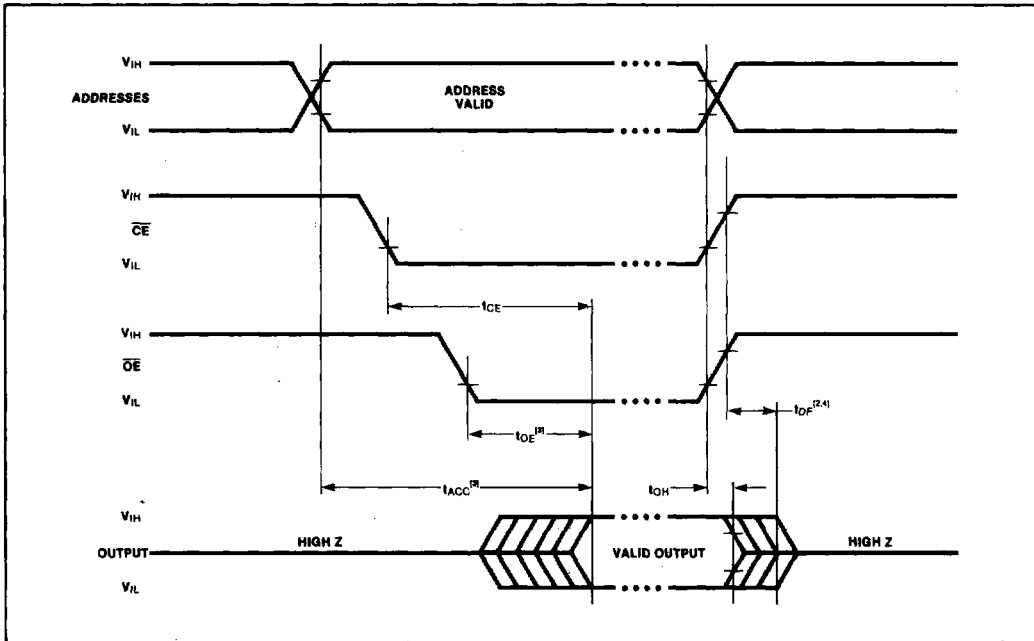
**A.C. TESTING INPUT/OUTPUT WAVEFORM**



**A.C. TESTING LOAD CIRCUIT**



**A.C. WAVEFORMS**



**NOTES:**

1. Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .
4.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.

## DEVICE OPERATION

The eight modes of operation of the 27256 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for  $V_{PP}$  and 12V on A9 for intelligent identifier mode.

Table 1. Operating Modes

MODE	PINS (20)	$\overline{CE}$ (22)	$\overline{OE}$ (24)	A <sub>9</sub> (1)	V <sub>PP</sub> (28)	V <sub>CC</sub> (11-13, 15-19)	OUTPUTS (11-13, 15-19)
Read	V <sub>IL</sub>	V <sub>IL</sub>	X	V <sub>CC</sub>	V <sub>CC</sub>	D <sub>OUT</sub>	
Output Disable	V <sub>IL</sub>	V <sub>IH</sub>	X	V <sub>CC</sub>	V <sub>CC</sub>	High Z	
Standby	V <sub>IH</sub>	X	X	V <sub>CC</sub>	V <sub>CC</sub>	High Z	
intelligent Programming	V <sub>IL</sub>	V <sub>IH</sub>	X	V <sub>PP</sub>	V <sub>CC</sub>	D <sub>IN</sub>	
Verify	V <sub>IH</sub>	V <sub>IL</sub>	X	V <sub>PP</sub>	V <sub>CC</sub>	D <sub>OUT</sub>	
Optional Verify	V <sub>IL</sub>	V <sub>IL</sub>	X	V <sub>PP</sub>	V <sub>CC</sub>	D <sub>OUT</sub>	
Program Inhibit	V <sub>IH</sub>	V <sub>IH</sub>	X	V <sub>PP</sub>	V <sub>CC</sub>	High Z	
intelligent Identifier	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>H</sub>	V <sub>CC</sub>	V <sub>CC</sub>	Code	

### NOTES:

1. X can be V<sub>IH</sub> or V<sub>IL</sub>
2. V<sub>H</sub> = 12.0V ± 0.5V

## READ MODE

The 27256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is avail-

able at the outputs after a delay of  $t_{OE}$  from the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been low and addresses have been stable for at least  $t_{ACC} - t_{OE}$ .

## STANDBY MODE

The 27256 has a standby mode which reduces the maximum active current from 100 mA to 40 mA. The 27256 is placed in the standby mode by applying a TTL-high signal to the  $\overline{CE}$  input. When in standby mode, the outputs are in a high impedance state, independent of the  $\overline{OE}$  input.

## Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

- a) the lowest possible memory power dissipation, and
- b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently,  $\overline{CE}$  (pin 20) should be decoded and used as the primary device selecting function, while  $\overline{OE}$  (pin 22) should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

## System Considerations

The power switching characteristics of HMOS II-E EPROMs require careful decoupling of the devices. The supply current,  $I_{CC}$ , has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by

properly selected decoupling capacitors. It is recommended that a 0.1  $\mu\text{F}$  ceramic capacitor be used on every device between  $V_{\text{CC}}$  and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7  $\mu\text{F}$  bulk electrolytic capacitor should be used between  $V_{\text{CC}}$  and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

## PROGRAMMING

**Caution:** Exceeding 14V on pin 1 ( $V_{\text{PP}}$ ) will permanently damage the 27256.

Initially, and after each erasure, all bits of the 27256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 27256 is in the programming mode when the  $V_{\text{PP}}$  input is at 12.5V and  $\overline{\text{CE}}$  is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

### intelligent Programming™ Algorithm

The 27256 intelligent Programming Algorithm rapidly programs Intel 27256 EPROMS using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of five minutes. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the 27256 intelligent Programming Algorithm is shown in Figure 3.

The intelligent Programming Algorithm utilizes two different pulse types: *initial* and *overprogram*. The duration of the initial  $\overline{\text{CE}}$  pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length  $3X$  msec.  $X$  is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular 27256 location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

**The entire sequence of program pulses and byte verifications is performed at  $V_{\text{CC}} = 6.0\text{V}$  and  $V_{\text{PP}} = 12.5\text{V}$ .** When the intelligent Programming cycle has been completed, all bytes should be compared to the original data with  $V_{\text{CC}} = V_{\text{PP}} = 5.0\text{V}$ .

### Program Inhibit

Programming of multiple 27256s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level  $\overline{\text{CE}}$  input inhibits the other 27256s from being programmed.

Except for  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$ , all like inputs of the parallel 27256s may be common. A TTL low-level pulse applied to the  $\overline{\text{CE}}$  input with  $V_{\text{PP}}$  at 12.5V will program the selected 27256.

### Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with  $\overline{\text{OE}}$  at  $V_{\text{IL}}$ ,  $\overline{\text{CE}}$  at  $V_{\text{IH}}$  and  $V_{\text{PP}}$  at 12.5V.

### Optional Verify

The optional verify may be performed in place of the verify mode. It is performed with  $\overline{\text{OE}}$  at  $V_{\text{IL}}$ ,  $\overline{\text{CE}}$  at  $V_{\text{IL}}$  (as opposed to the standard verify which has  $\overline{\text{CE}}$  at  $V_{\text{IH}}$ ), and  $V_{\text{PP}}$  at 12.5V. The outputs will tri-state according to the signal presented to  $\overline{\text{OE}}$ . Therefore, all devices with  $V_{\text{PP}} = 12.5\text{V}$  and  $\overline{\text{OE}} = V_{\text{IL}}$  will present data on the bus independent of the  $\overline{\text{CE}}$  state. When parallel programming several devices which share a common bus,  $V_{\text{PP}}$  should be lowered to  $V_{\text{CC}} (= 6.0\text{V})$  and the normal read mode used to execute a program verify.

### intelligent Identifier™ Mode

The intelligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the  $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$  ambient temperature range that is required when programming the 27256.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the 27256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from  $V_{\text{IL}}$  to  $V_{\text{IH}}$ . All other address lines must be held at  $V_{\text{IL}}$  during intelligent Identifier Mode.

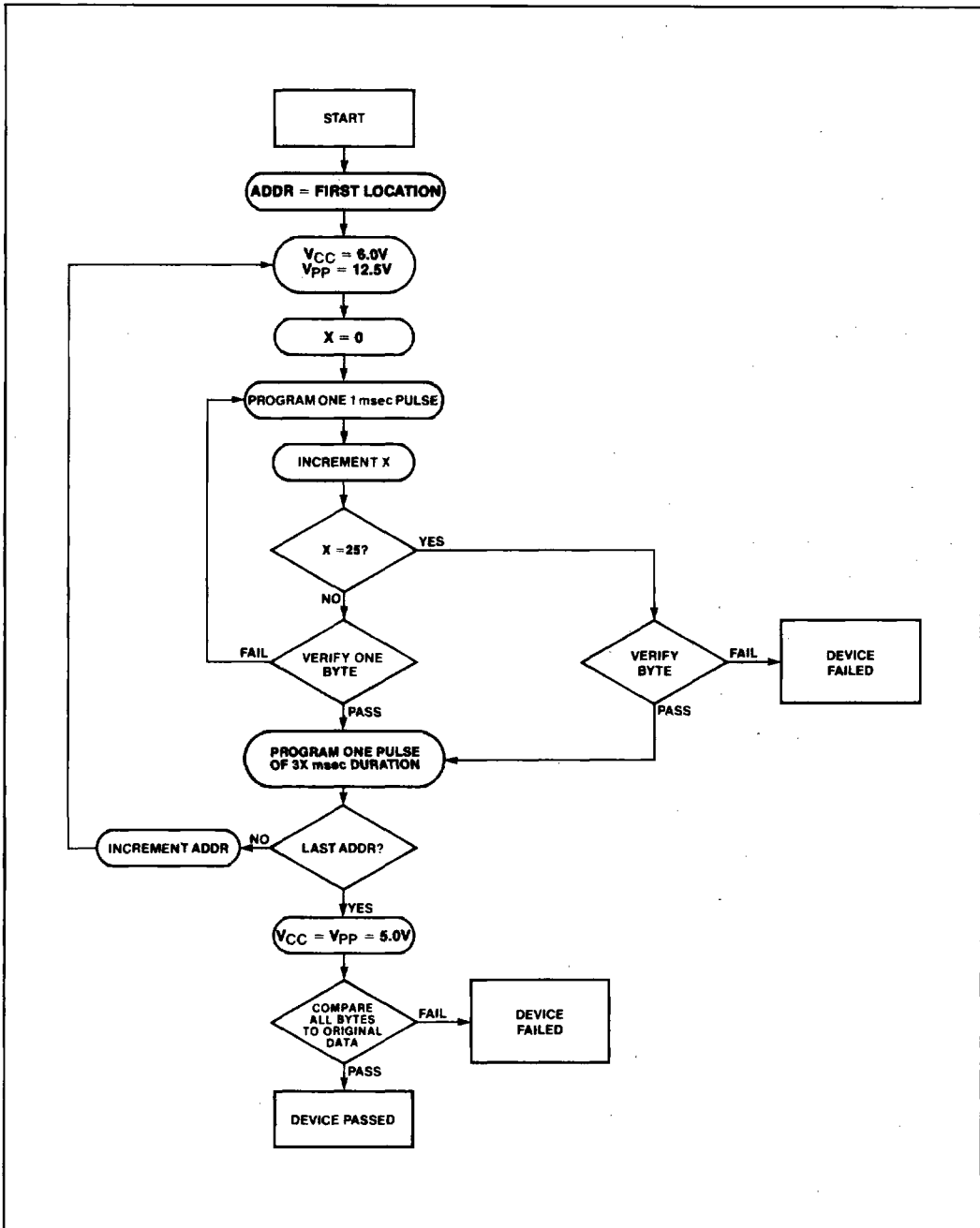


Figure 3. 27256 Intelligent Programming™ Flowchart

Byte 0 ( $A_0 = V_{IL}$ ) represents the manufacturer code and byte 1 ( $A_0 = V_{IH}$ ) the device identifier code. For the Intel 27256, these two identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the MSB ( $O_7$ ) defined as the parity bit.

### ERASURE CHARACTERISTICS

The erasure characteristics of the 27256 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms ( $\text{\AA}$ ). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000  $\text{\AA}$  range. Data show that constant exposure to room level fluorescent lighting could erase the typical 27256 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 27256 is to be ex-

posed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the 27256 window to prevent unintentional erasure.

The recommended erasure procedure for the 27256 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms ( $\text{\AA}$ ). The integrated dose (i.e., UV intensity  $\times$  exposure time) for erasure should be a minimum of 15 Wsec/cm<sup>2</sup>. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000  $\mu\text{W}/\text{cm}^2$  power rating. The 27256 should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose a 27256 can be exposed to without damage is 7258 Wsec/cm<sup>2</sup> (1 week @ 12000  $\mu\text{W}/\text{cm}^2$ ). Exposure of the 27256 to high intensity UV light for long periods may cause permanent damage.

Table 2. 27256 Intelligent Identifier™ Bytes

Identifier \ Pins	$A_0$ (10)	$O_7$ (19)	$O_6$ (18)	$O_5$ (17)	$O_4$ (16)	$O_3$ (15)	$O_2$ (13)	$O_1$ (12)	$O_0$ (11)	Hex Data
Manufacturer Code	$V_{IL}$	1	0	0	0	1	0	0	1	89
Device Code	$V_{IH}$	0	0	0	0	0	1	0	0	04

#### NOTES:

- $A_9 = 12.0\text{V} \pm 0.5\text{V}$
- $A_1 - A_8, A_{10} - A_{13}, \overline{CE}, \overline{OE} = V_{IL}$
- $A_{14} = V_{IH}$  or  $V_{IL}$

### Intelligent Programming™ Algorithm

#### D.C. PROGRAMMING CHARACTERISTICS:

$$T_A = 25 \pm 5^\circ\text{C}, V_{CC} = 6.0\text{V} \pm 0.25\text{V}, V_{PP} = 12.5\text{V} \pm 0.5\text{V}$$

Symbol	Parameter	Limits			Test Conditions (see Note 1)
		Min.	Max.	Unit	
$I_{LI}$	Input Current (All Inputs)		10	$\mu\text{A}$	$V_{IN} = V_{IL}$ or $V_{IH}$
$V_{IL}$	Input Low Level (All Inputs)	-0.1	0.8	V	
$V_{IH}$	Input High Level	2.0	$V_{CC}$	V	
$V_{OL}$	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1\text{mA}$
$V_{OH}$	Output High Voltage During Verify	2.4		V	$I_{OH} = -400\mu\text{A}$
$I_{CC2}$	$V_{CC}$ Supply Current (Program & Verify)		100	mA	
$I_{PP2}$	$V_{PP}$ Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
$V_{ID}$	$A_9$ Intelligent Identifier Voltage	11.5	12.5	V	

#### NOTES:

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .



**A.C. PROGRAMMING CHARACTERISTICS:**
 $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.0\text{V} \pm 0.25\text{V}$ ,  $V_{PP} = 12.5\text{V} \pm 0.3\text{V}$ 

Symbol	Parameter	Limits				Test Conditions* (see Note 1)
		Min.	Typ.	Max.	Unit	
$t_{AS}$	Address Setup Time	2			$\mu\text{s}$	
$t_{OES}$	$\overline{\text{OE}}$ Setup Time	2			$\mu\text{s}$	
$t_{DS}$	Data Setup Time	2			$\mu\text{s}$	
$t_{AH}$	Address Hold Time	0			$\mu\text{s}$	
$t_{DH}$	Data Hold Time	2			$\mu\text{s}$	
$t_{DFP}^4$	$\overline{\text{OE}}$ High to Output Float Delay	0		130	ns	
$t_{VPS}$	$V_{PP}$ Setup Time	2			$\mu\text{s}$	
$t_{VCS}$	$V_{CC}$ Setup Time	2			$\mu\text{s}$	
$t_{PW}$	$\overline{\text{CE}}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	(see Note 3)
$t_{OPW}$	$\overline{\text{CE}}$ Overprogram Pulse Width	2.85		78.75	ms	(see Note 2)
$t_{OE}$	Data Valid from $\overline{\text{OE}}$			150	ns	

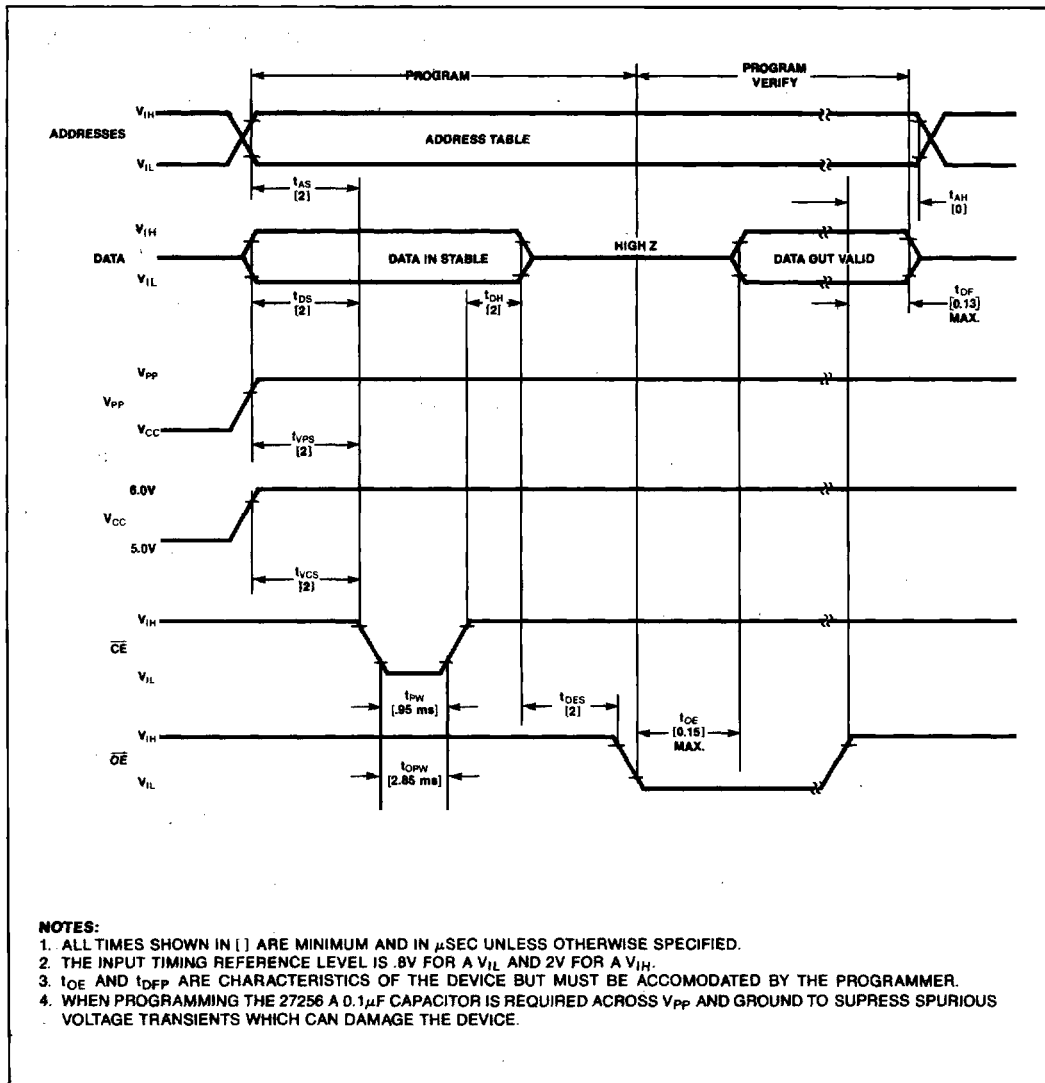
**\*A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) ... 20 ns  
 Input Pulse Levels ..... 0.45V to 2.4V  
 Input Timing Reference Level ..... 0.8V and 2.0V  
 Output Timing Reference Level ... 0.8V and 2.0V

**NOTES:**

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
- Initial Program Pulse width tolerance is 1 msec  $\pm 5\%$ .
- This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram on the following page.

Intelligent Programming™ WAVEFORMS



NOTES:

1. ALL TIMES SHOWN IN [ ] ARE MINIMUM AND IN  $\mu$ -SEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS .8V FOR A  $V_{IL}$  AND 2V FOR A  $V_{IH}$ .
3.  $t_{OE}$  AND  $t_{DF}$  ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
4. WHEN PROGRAMMING THE 27256 A  $0.1\mu F$  CAPACITOR IS REQUIRED ACROSS  $V_{PP}$  AND GROUND TO SUPPRESS SPURIOUS VOLTAGE TRANSIENTS WHICH CAN DAMAGE THE DEVICE.