SCG9800 Microcontroller Specification

FEATURE SUMMARY

Technology

- CMOS technology.

CPU

- 8-bit CPU core.
- 128 powerful and easy-to-use instruction set.

Memory

- Internal RAM: 240 x 8
- Memory is organized as 16K-byte page.
- External memory access of up to 1M x 8, can be both ROM and RAM.

I/O Structure

- Memory mapped I/O structure.

Oscillation Frequency

- RC Oscillator for the main system clock up to 4MHz, instruction cycle ~0.5us.
- Subsystem clock frequency of 32.768kHz for real time timer.

Power Down

- Stop mode (stop main and subsystem clock to core)
- Sleep mode (stop main system clock only)

Interrupts

- 2 timer interrupts.
- 1 real time interrupt.
- 1 external event interrupt.
- 1 software interrupt.

I/O Ports

- 1 8-bit programmable I/O port.
- 1 2-bit output port.

Timer

- 2 8-bit pre-scalar auto reload timers which can be cascaded to form one 16-bit timer.
- 1 real time timer.
- 1 watch dog timer.

Operating Voltage

- 2.4V to 5.5V.

FUNCTION OVERVIEW

Program Memory Map

RAM Area:

Address	Description
$00-$0F	H/W registers and I/Os
$10-$FF	Data memory and Stack

Figure 1. Memory map in RAM area

External ROM Area:

Physical Address	Description
$0000-$3FFF	Page 0 Program Reset address at $0000
$4000-$7FFF	Page 1
$8000-$BFFF	Page 2
$C000-$FFFF	Page 3 Software interrupt at $FFC0 External interrupt at $FFD0 Timer 1 interrupt at $FFE0 Timer 0/RTC interrupt at $FFF0
$7C000-$7FFFF	Page 31
$FC000-$FFFFF	Page 63

Figure 2. Memory map in external ROM area

CPU core

An 8-bit accumulator based CPU core can directly address up to 64 x 16K byte addressing space. Most of the instructions are executed in two cycles. Instruction is generally one byte and will have an extra byte for some addressing modes.

CPU Registers:

Program Counter (PC)

The 14-bit Program Counter stores address for instruction fetch during program execution. It makes up a page size of 16K bytes. Together with the Program Page Register (iPAGE), it becomes a 20-bit address that can access up to 1,048,576 bytes. When the CPU resets, the content of the iPAGE:PC will be 00:0000. If interrupt occurs, the type of interrupt will then determine its content. PC will automatically be incremented to the next instruction after an instruction fetch.

Table 1. Different types of interrupt

Interrupt	IPAGE:PC
Timer 0 / RTC Interrupt	3H:3FF0H
Timer 1 Interrupt	3H:3FE0H
External Interrupt	3H:3FD0H
Software Interrupt	3H:3FC0H

Page Register (PAGE)

An 8-bit Page Register is used to change the program flow. The most significant two bits are always set to zero.

Data Bank Register (BANK)

An 8-bit Bank Register is used to access data memory. The most significant two bits are always set to zero.

Program Page Register (iPAGE)

An 8-bit Program Page Register is combined with PC for instruction fetch. The most significant two bits are always set to zero.

Accumulator (A)

An 8-bit Accumulator is used for arithmetic, logical and data movement operation.

Temporary Register (B)

An 8-bit temporarily storage is used for accumulator.

Index Registers (X, Y)

These two 8-bit registers can be used for general registers and index registers of the indirect addressing mode. They can also be used as pointer for table read and memory write instructions.

Stack Register (SP)

An 8-bit Stack Register (SP) stores the address for stack operation. After CPU resets, the value is $00. The SP has to be initialized at $FF by software. This means the stack frame starts from the highest address memory location.

Program Status (PS)

This is an 8-bit Program Status Register. However only 4-bit is used for controlling ALU operations and instruction execution sequences.
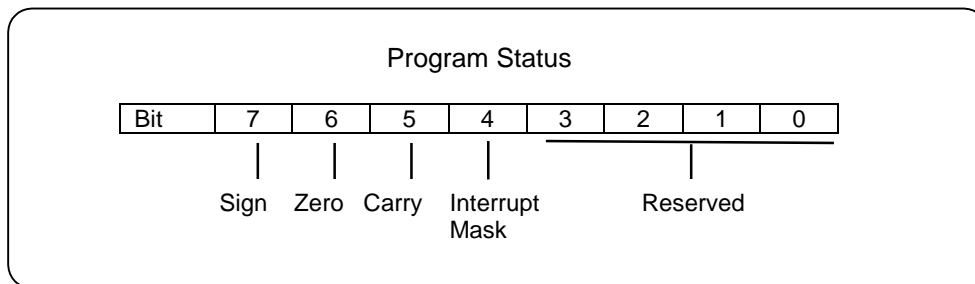
Program Status

Bit	7	6	5	4	3	2	1	0

Sign   Zero   Carry   Interrupt   Reserved
                      Mask

Figure 3. 8-bit Program Status

Carry Flag (C)

Whenever there is a carry or borrow occurs after an arithmetic operation, carry flag is set to 1. Otherwise, it is cleared to 0.

Besides, the "Rotate" instructions can also change the carry flag which value is a bit shifted out of the specified source operand.

Executing single instruction of "SETC" or "CLRC" can also alter this flag.

Upon returning from an interrupt service routine, this flag will be restored.

Zero Flag (Z)

For arithmetic and logical operations, Zero flag will be set to 1 if the result is zero.

Besides, for operation that involves moving source operand to accumulator, zero flag will also be set to 1 if the content of the source operand is zero.

Upon returning from an interrupt service routine, this flag will be restored.

Sign Flag (N)

Sign flag stores the most significant bit of a result after the following operations: -
a.   Arithmetic
b.   Logic
c.   Move from source operand to accumulator

This flag will also be restored upon returning from an interrupt service routine.

Interrupt Mask Flag (I)

The flag will be set to 1 when entering an interrupt service routine. By that time, all other interrupt events will be pending.

After exiting from the interrupt service routine, this interrupt mask flag will be cleared to 0. Then interrupt handling will be resumed.

Memory

By connecting PAD_EXT_ADDR to HIGH, external memory access of 512K bytes is allowed. In addition, setting bit5 of the internal register TCONG will expand memory access to another 512K bytes. This extra external memory block can be RAM or ROM. For this ROM-less chip, memory is arranged in 16K-byte page size each. Therefore, there can have 32 pages for 512K bytes of memory space. Regarding the instruction pointer, it is organized as iPAGE:PC for instruction fetch.

Change of program flow between pages is by modifying the PAGE register and then followed by executing a JMP or CALL instruction. These two instructions will load the PAGE register to iPAGE and change the content in PC for long JMP or CALL instruction. It does not need to change the PAGE register if it is a short JMP/CALL (i.e. JMP/CALL within page) because the PAGE register is normally the same as the iPAGE register. To exit a subroutine, long or short return type must be specified for long or short CALL respectively.

The microcontroller has 240 bytes internal RAM data storage of address $10-$FF. This area includes stack frame and data memory. The stack frame is usually initialized at the highest RAM address location, i.e. $FF.

Oscillation Circuits

Main system and subsystem oscillation circuitry generates the internal clock signal for the CPU and other hardware timings. The main system clock uses the RC oscillation source. The operating frequency is up to 4 MHz. This clock is for the CPU and the two timers.

The subsystem clock is for the real time signals. It uses a 32.768 kHz crystal. It has to be tied to a voltage level, either HIGH or LOW, if the real time timer and the watch dog timer are not used.

Power Down

The microcontroller supports power down mode for saving power.

Executing a STOP instruction will stop both main system and subsystem clock to the core to save most of the microcontroller power. To enter sleep mode, execute a SLEEP instruction will stop the system clock only.

Only an external interrupt will release the microcontroller from STOP mode if external interrupt enable bit is set to 1. For SLEEP mode, the microcontroller will be awoken every 0.5 sec or by the external interrupt if corresponding enable bit is set to 1.

Interrupts

The MICROCONTROLLER has 2 timer interrupts, one real time interrupt, one external event interrupt and one software interrupt. When interrupt occurs, the content of PC, iPAGE and PS are pushed onto the stack in sequence. And then, the corresponding interrupt vector is loaded into iPAGE:PC. Upon executing a RTI instruction, the registers are popped out of the stack in the reversed order.

The preference of interrupt priority is Timer 0 / RTC interrupt, Timer 1 interrupt and then external interrupt.

I/O Ports

The microcontroller has one 2-bit output port and one software-controllable 8-bit I/O port.

For I/O port 0, there is a pull-low resistor when it is configured in input mode, and this resistor is disabled when it is in output mode.

For Port 5, it is a 2-bit output port only.

Remark: Port 4 bit3 can be an output if the chip is not configured as 8M bits external memory access via setting bit6 of the internal register TCONG.

Timers

The microcontroller has two programmable 8-bit timers (T0 and T1) for system timing. It has also a real time timer and a watch dog timer when subsystem clock is employed. All the timers can be enabled or disabled by configuring an internal register, TCONG. At CPU resets, all of them are disabled.

T0 and T1 are up-counters and can be configured as either two 8-bit pre-scalar auto reload timer or as a 16-bit pre-scalar auto reload timer. The timer overflow flag will be set if the timer overflows. Then an interrupt will be generated if the corresponding interrupt enable bit is set to 1.

The real time timer provides 0.5 sec interrupt for RTC functions. Watch dog timer will overflow in ~1 sec and then will reset the CPU.

BLOCK DIAGRAM
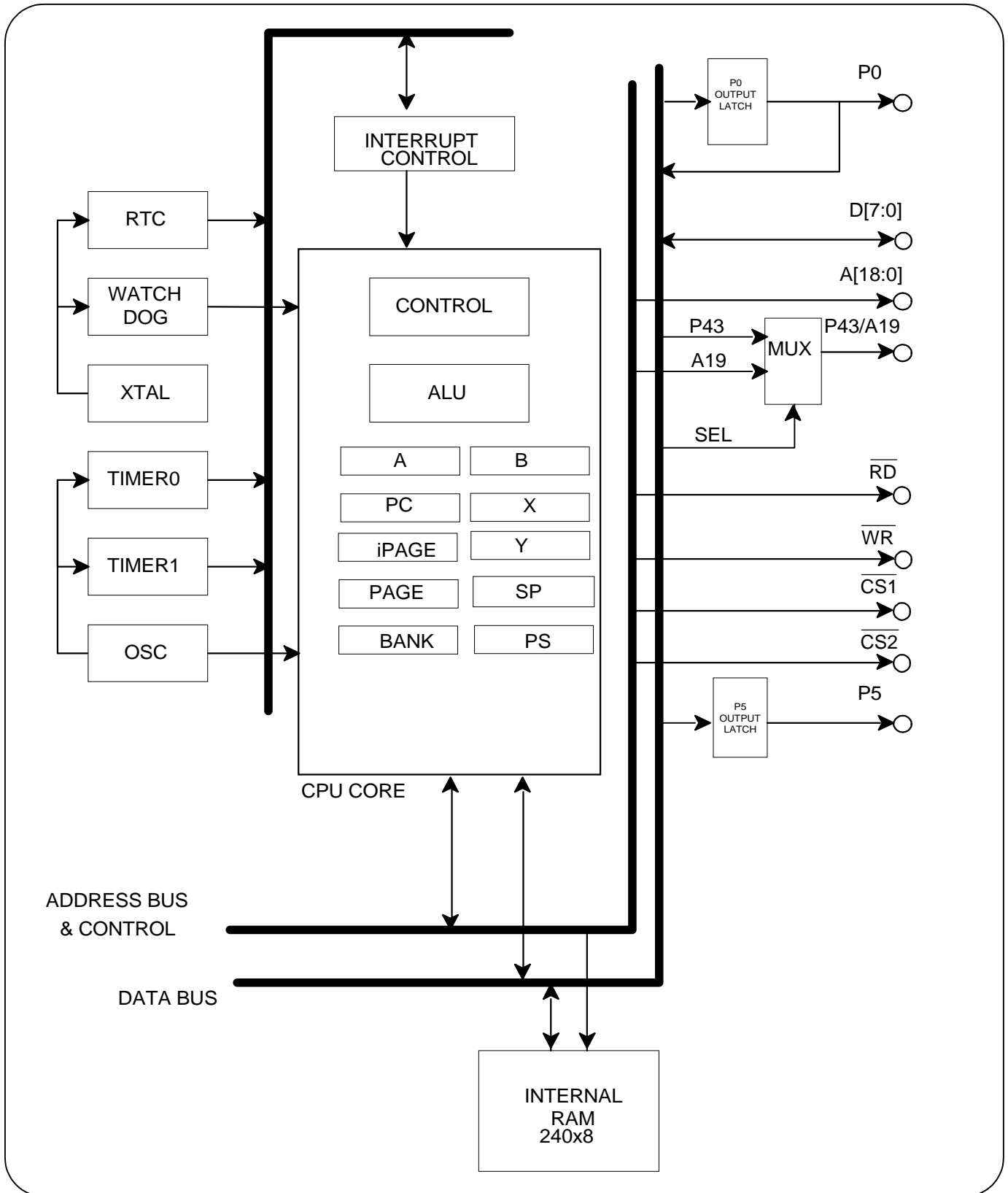
Figure 4. Block diagram of SCG9800

PIN DESCRIPTIONS

Table 2. Pin Description

Pin	Name	Type	Description	Pad Type
1	A0	O/P	Address bus	Pad type 2
2	A1	O/P	Address bus	Pad type 2
3	A2	O/P	Address bus	Pad type 2
4	A3	O/P	Address bus	Pad type 2
5	A4	O/P	Address bus	Pad type 2
6	A5	O/P	Address bus	Pad type 2
7	A6	O/P	Address bus	Pad type 2
8	A7	O/P	Address bus	Pad type 2
9	VDD	Power	Supply Voltage	
10	VSS	Power	Ground	
11	D0	I/O	Data bus	Pad type 1
12	D1	I/O	Data bus	Pad type 1
13	D2	I/O	Data bus	Pad type 1
14	D3	I/O	Data bus	Pad type 1
15	D4	I/O	Data bus	Pad type 1
16	D5	I/O	Data bus	Pad type 1
17	D6	I/O	Data bus	Pad type 1
18	D7	I/O	Data bus	Pad type 1
19	P50	O/P	Port 5	Pad type 2
20	P51	O/P	Port 5	Pad type 2
21	-			
22	-			
23	P00	I/O	Port 0	Pad type 1
24	P01	I/O	Port 0	Pad type 1
25	P02	I/O	Port 0	Pad type 1
26	VDD	Power	Supply Voltage	
27	VSS	Power	Ground	
28	P03	I/O	Port 0	Pad type 1
29	P04	I/O	Port 0	Pad type 1
30	P05	I/O	Port 0	Pad type 1
31	P06	I/O	Port 0	Pad type 1
32	P07	I/O	Port 0	Pad type 1
33	EXT_ADDR	I/P	External address	Pad type 4
34	TEST_ROM	I/P	Test pin, no connection	Pad type 4
35	VSS	Power	Ground	
36	VDD	Power	Supply Voltage	
37	$\overline{\text{RESET}}$	I/P	Reset pin	Pad type 3
38	EXT_INT	I/P	External Interrupt pin	Pad type 4
39	CLK32I	I/P	32.768kHz RTC	Pad type 6

Pin	Name	Type	Description	Pad Type
40	CLK320	O/P	32.768KHz RTC	Pad type 6
41	TEST	I/P	Test pin, no connection	Pad type 4
42	P_CLK_0	O/P	RC oscillator output	Pad type 6
43	P_CLK	I/P	RC oscillator for the main system clock	Pad type 5
44	A15	I/O	Address bus	Pad type 1
45	A14	I/O	Address bus	Pad type 1
46	A13	I/O	Address bus	Pad type 1
47	A12	I/O	Address bus	Pad type 1
48	A11	I/O	Address bus	Pad type 1
49	A10	I/O	Address bus	Pad type 1
50	A9	I/O	Address bus	Pad type 1
51	A8	I/O	Address bus	Pad type 1
52	VSS	Power	Ground	
53	VDD	Power	Supply Voltage	
54	$\overline{CS2}$	O/P	Chip select 2	Pad type 2
55	$\overline{CS1}$	O/P	Chip select 1	Pad type 2
56	$\overline{WR}$	O/P	Write signal	Pad type 2
57	$\overline{RD}$	O/P	Read signal	Pad type 2
58	P43/A19	O/P	Port 4 bit3/ Address bus bit19	Pad type 2
59	A18	O/P	Address bus	Pad type 2
60	A17	O/P	Address bus	Pad type 2
61	A16	O/P	Address bus	Pad type 2
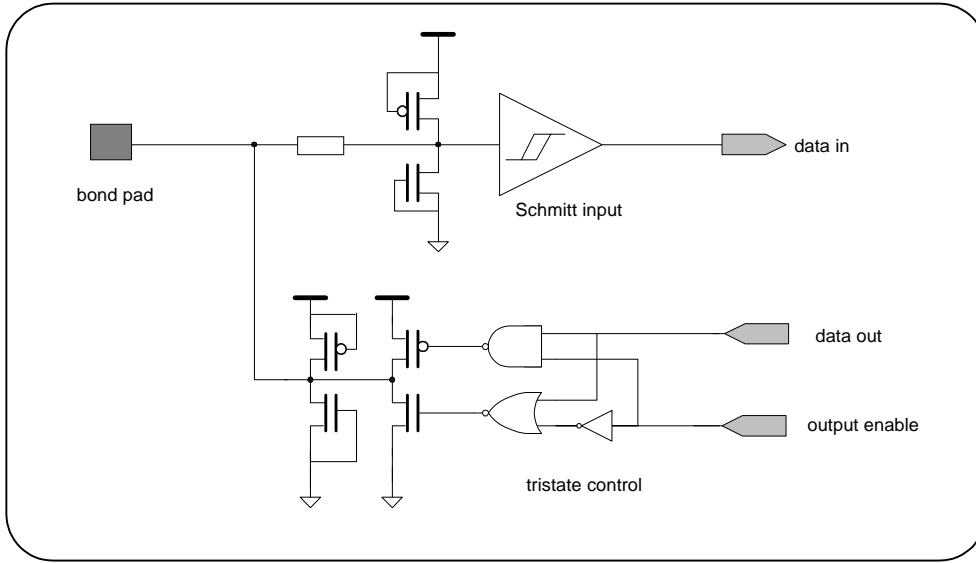
Figure 5. Pad type 1 (bi-directional pad)
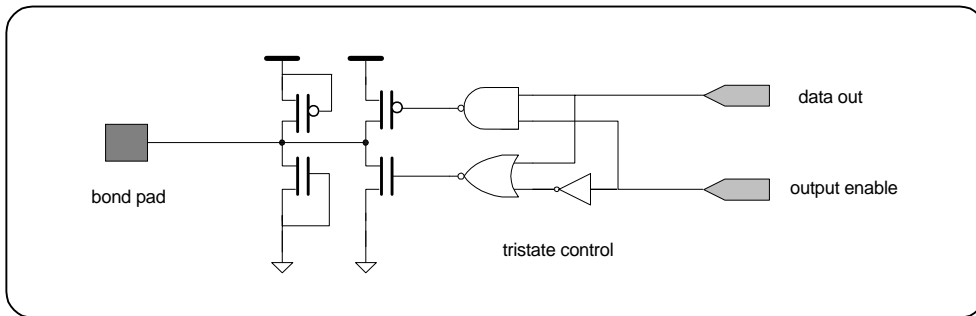
Figure 6. Pad type 2 (output pad)
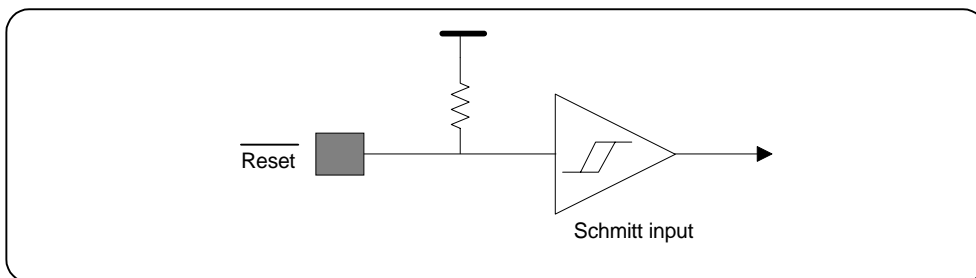
Figure 7. Pad type 3 ($\overline{\text{Reset}}$)
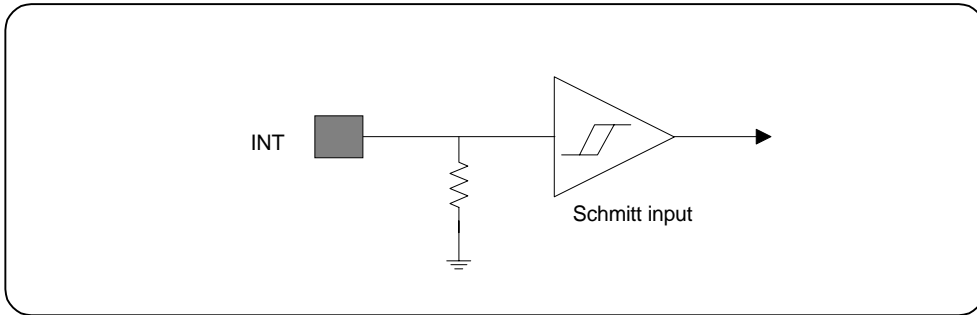
Figure 8. Pad type 4 (external interrupt)
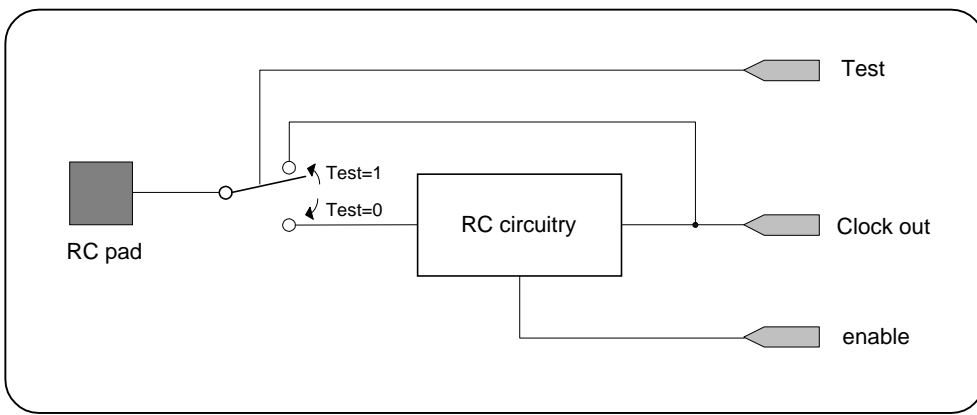
Figure 9. Pad type 5 (RC oscillation pad)
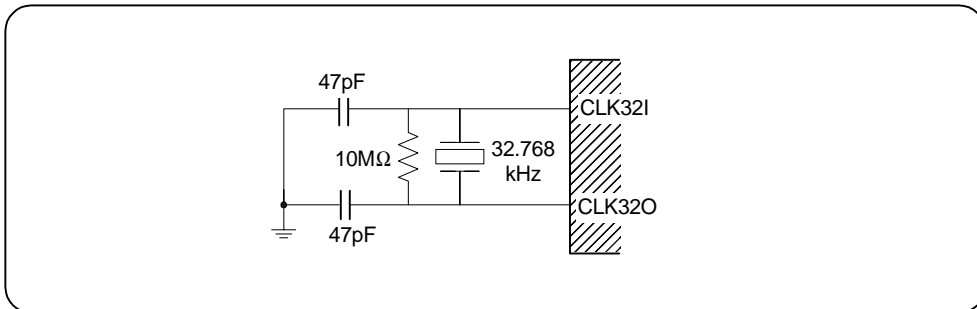
Figure 10. Pad type 6 (Clock circuit)

Control Registers

Summary

Table 3. Summary of Control Registers

Hex	Mnemonic	Control Registers Name	R/W
00H	P0DIR	Port 0 Direction Control Register	W
01H	P0PULL	Port 0 Pull-Low Control Register	W
02H	P0RW	Port 0 Read/Write Port	R/W
03H	P1DIR	Port 1 Direction Control Register	W
04H	P1RW	Port 1 Read/Write Port	R/W
05H	P2W	Port 2 Output Port	W
06H	-	-	-
07H	P4W	Port 4 Output Port	W
08H	P5W	Port 5 Output Port	W
09H	TCONG	Timer Configuration Port	W
0AH	INTR	Interrupt Control Register	W
0BH	TFLAG	Timer Flag Status Register/Watch-dog Reset	R/W
0CH	T0VAL	Timer 0 Preset Value Register	W
0DH	T1VAL	Timer 1 Preset Value Register	W
0EH	-	-	-
0FH	-	-	-

Descriptions

P0DIR and P1DIR

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W

0: Input mode (default)
1: Output mode
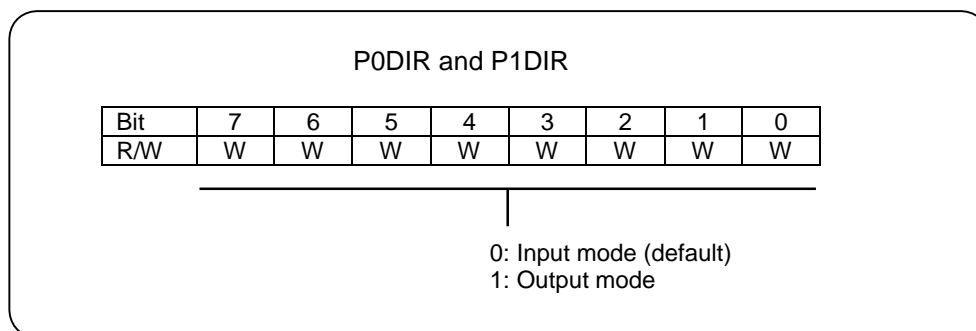
Figure 11. Port 0 and Port 1 Direction Control Registers

P0PULL

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W

0: Pull-low resistor disable (default)
1: Pull-low resistor enable
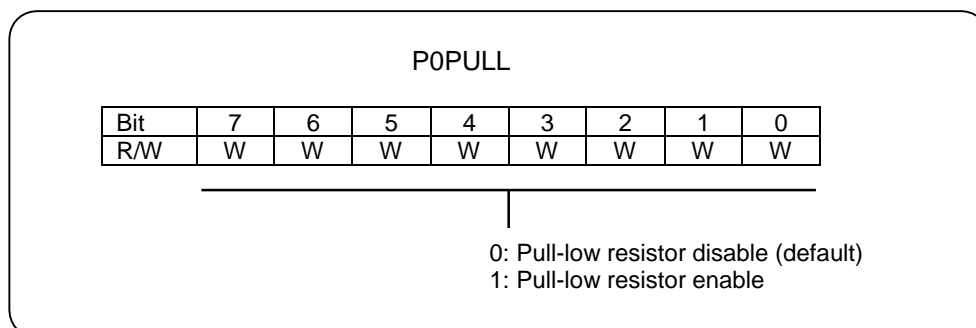
Figure 12. Port 0 Pull-low Control Register

P0RW and P1RW

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Write to output latch.
Read from input pin. Read value of Output pin
will be the output latch value.
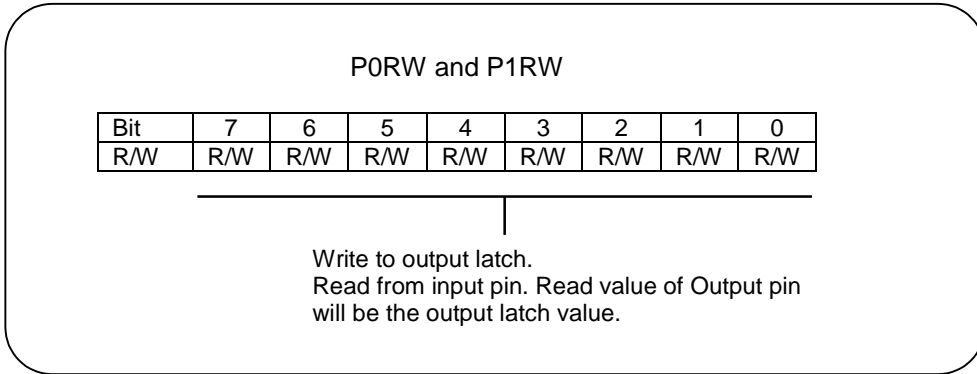
Figure 13. Port 0 and Port 1 Read/Write Port

P2W

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W

Write to output latch
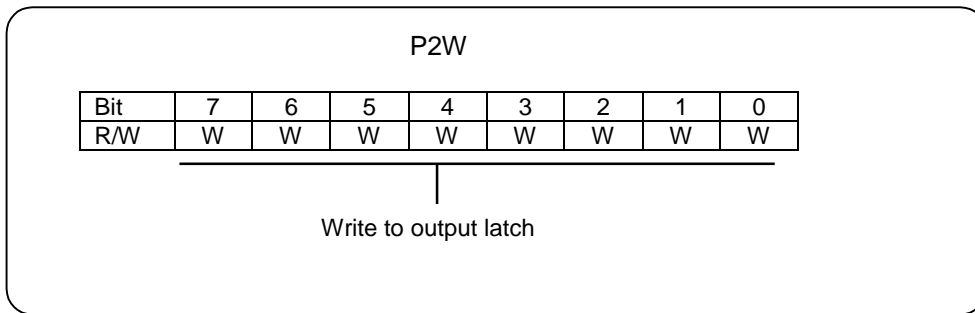
Figure 14. Port 2 Output Port

TCONG

Bit	7	6	5	4	3	2	1	0
R/W	-	-	-	W	W	W	W	W

Reserved

000 : disable T0 and T1
0x1 : enable T0
01x : enable T1
1xx : cascade T0:T1 as 16-bit timer

Real time timer
0 : disable
1 : enable (0.5s interrupt)

Watch dog timer
0 : disable
1 : enable (~1s)

External memory access, EM
0 : disable (default)
1 : enable

External memory access mode, EMM (see below)

External memory access mode, EMM

With external memory access enabled, i.e. EM set,

EXT-ADDR	EMM	External Memory	
		Size	Chip Select
0	0	4M-bit	$\overline{CS1}$
0	1	2M-bit	$\overline{CS1}$
		2M-bit	$\overline{CS2}$
1	0	4M bit	$\overline{CS1}$
		4M bit	$\overline{CS2}$
1	1	8M bit	$\overline{CS1}$

Figure 15. Timer Configuration Port

INTR

Bit	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	W	W	W

Reserved

External interrupt
0 : disable
1 : enable

T1 interrupt
0 : disable
1 : enable

T0/RTC (half second) interrupt
0 : disable
1 : enable
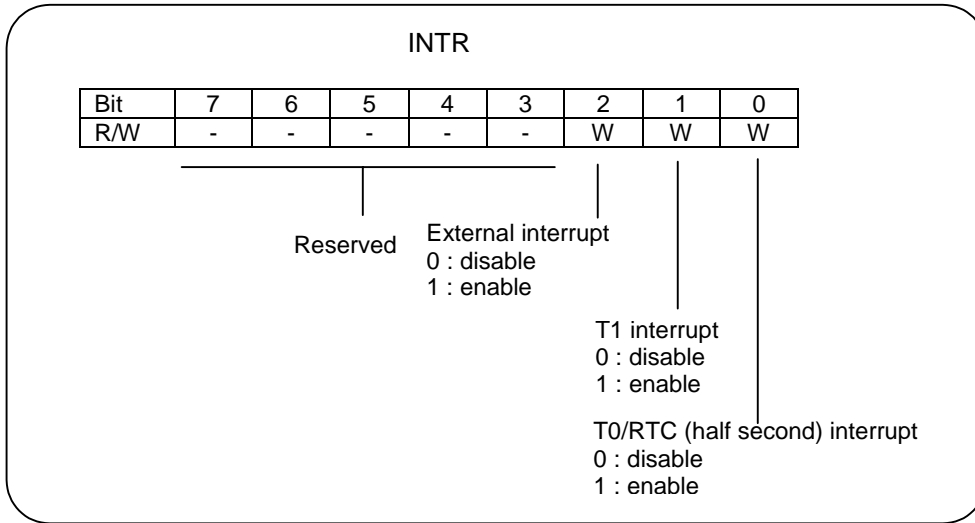
Figure 16. Interrupt Control Register

TFLAG

Bit	7	6	5	4	3	2	1	0
R/W	-	-	-	-	R	R	R	R

Reserved

CLK32I Input

0 : T0 not overflow
1 : T0 overflow

0 : T1 not overflow
1 : T1 overflow

0 : not half second
1 : half second

Note :
Read will reset all flags.
Any write operation to TFLAG will reset the
watch dog timer.
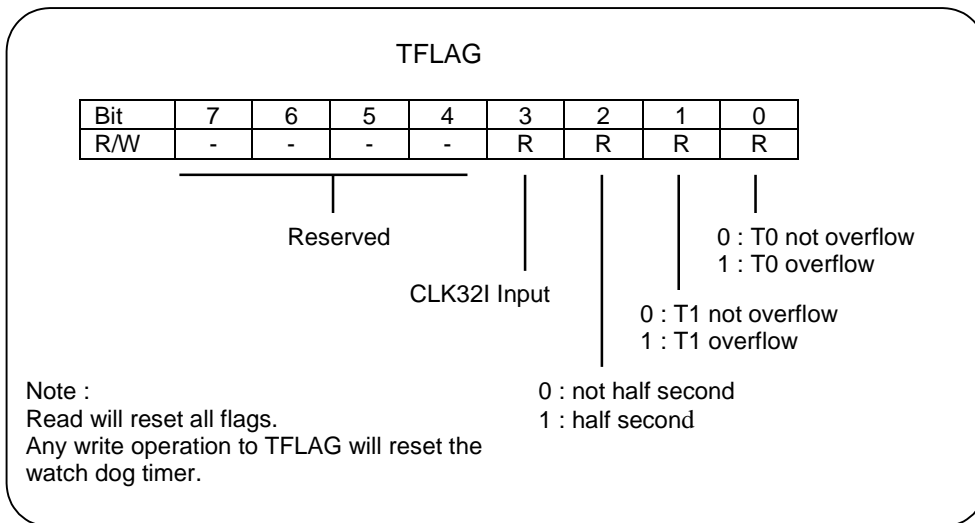
Figure 17. Timer Flag Status Register/Watch-dog Reset

T0VAL and T1VAL

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W

Write timer 0 and timer 1 preset value

$$\text{Timer frequency} = \frac{\text{system clock}}{2} \times \frac{1}{\text{counter value}}$$

For either T0 or T1,
       Maximum counter value = 255
       Minimum frequency $\approx$ 7840Hz
For T0:T1,
       Maximum counter value = 65535
       Minimun frequency $\approx$ 30Hz
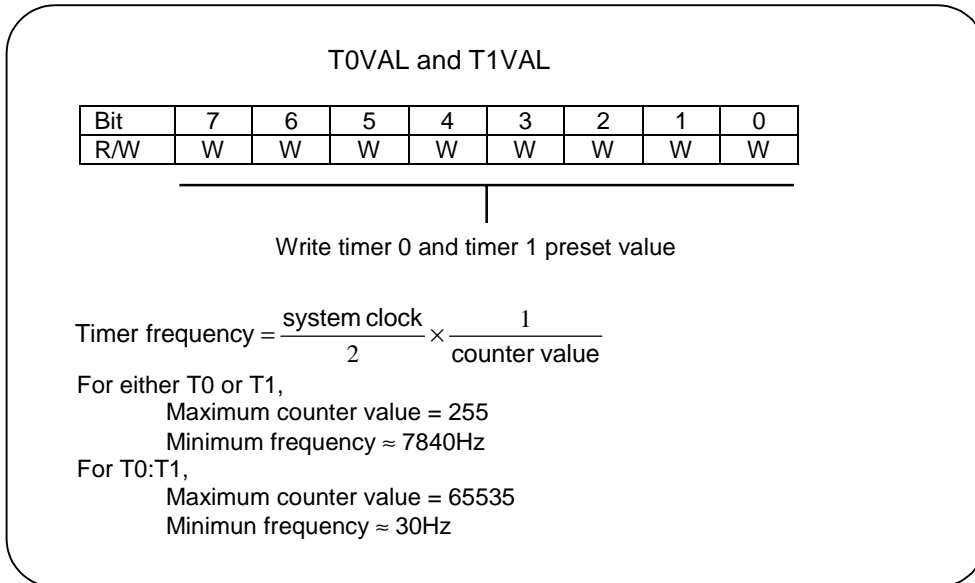
Figure 18. Timer 0 and Timer 1 Preset Value Register

INSTRUCTION SUMMARY

There are 128 instructions. All instructions are one or two byte instructions.
The followings are the notations used:

A	Accumulator
B	B Register
C	Carry bit
Z	Zero bit
N	Negative bit
X	X Index Register
Y	Y Index Register
SP	Stack Pointer Register
(SP)	Stack
BANK	Data Bank Register
PAGE	Page Register
iPAGE	The page register for PC19-PC14
PC	Program Counter PC13-0
PS	Program Status
I	Interrupt flag
(X)	RAM pointed by X
(Y)	RAM pointed by Y
label	A 8-bit RAM/Register label
(label)	RAM pointed by the label
ADDR14	A 14-bit address
ADDR 8	A 8-bit address
#CONSTANT	A 8-bit constant

INSTRUCTION SET

1.

ADC A	
Code	0100 0000
Operation	A + A + C→A
Flags	N, Z, C

2.

ADC X	
Code	0100 0010
Operation	X + A + C→A
Flags	N, Z, C

3.

ADC Y	
Code	0100 0011
Operation	Y + A + C→A
Flags	N, Z, C

4.

ADC (X)	
Code	0100 0110
Operation	(X) + A + C→A
Flags	N, Z, C

5.

ADC (Y)	
Code	0100 0111
Operation	(Y) + A + C→A
Flags	N, Z, C

6.

ADC label	
Code	0100 0100 zzzz zzzz
Operation	(zzzz zzzz)+A+C→A
Flags	N, Z, C

7.

ADC #CONSTANT	
Code	0100 0001 zzzz zzzz
Operation	Zzzz zzzz +A+C→A
Flags	N, Z, C

8.

AND A	
Code	0100 1000
Operation	A ∧ A→A
Flags	N,Z

9.

AND X	
Code	0100 1010
Operation	X ∧ A→A
Flags	N,Z

10.

AND Y	
Code	0100 1011
Operation	Y ∧ A→A
Flags	N,Z

11.

AND (X)	
Code	0100 1110
Operation	(X) ∧ A→A
Flags	N,Z

12.

AND (Y)	
Code	0100 1111
Operation	(Y) ∧ A→A
Flags	N,Z

13.

AND label	
Code	0100 1100 zzzz zzzz
Operation	(zzzz zzzz)∧A→A
Flags	N,Z

14.

AND #CONSTANT	
Code	0100 1001 zzzz zzzz
Operation	Zzzz zzzz ∧ A →A
Flags	N,Z

15.

BRA ADDR8	
Code	0011 0010 zzzz zzzz
Operation	Zzzz zzzz → PC0-7
Flags	-----

16.

CALL ADDR14	
Code	11zz zzzz zzzz zzzz
Operation	PC →(SP);SP-2→SP
	ADDR14 →PC[13:0]
	If PAGE ≠ iPAGE
	IPAGE→(SP);SP-1→SP
	PAGE →iPAGE
Flags	-----

17.

CLR A	
Code	0010 1000
Operation	0 →A
Flags	N,Z

18.

CLR X	
Code	0010 1010
Operation	0 →X
Flags	-----

19.

CLR Y	
Code	0010 1011
Operation	0 →Y
Flags	-----

20.

CLR (X)	
Code	0010 1110
Operation	0 →(X)
Flags	-----

21.

CLR (Y)	
Code	0010 1111
Operation	0 →(Y)
Flags	-----

22.

CLR label	
Code	0010 1100
Operation	0 →(zzzz zzzz)
Flags	-----

23.

CLRC	
Code	0110 0001
Operation	0 →C
Flags	C

24.

CMP	
Code	0000 0001 zzzz zzzz
Operation	A ∀ zzzz zzzz
Flags	Z

25.

CMP label	
Code	0000 0101 zzzz zzzz
Operation	A ∀ (zzzz zzzz)
Flags	Z

26.

CPMX #CONSTANT	
Code	0000 1001 zzzz zzzz
Operation	(X) ∀ zzzz zzzz
Flags	Z

27.

CPMX label	
Code	0000 1101 zzzz zzzz
Operation	(X) ∀ zzzz zzzz
Flags	Z

28.

CPX #CONSTANT	
Code	0001 0001 zzzz zzzz
Operation	X ∀ zzzz zzzz
Flags	Z

29.

CPX label	
Code	0001 0101 zzzz zzzz
Operation	X ∀ (zzzz zzzz)
Flags	Z

30.

CPY #CONSTANT	
Code	0001 1001 zzzz zzzz
Operation	Y ∀ zzzz zzzz
Flags	Z

31.

CPY label	
Code	0001 1101 zzzz zzzz
Operation	Y ∀ (zzzz zzzz)
Flags	Z

32.

DEC A	
Code	0110 1000
Operation	$A - 1 \rightarrow A$
Flags	N, Z, C

33.

DEC X	
Code	0110 1010
Operation	$X - 1 \rightarrow X$
Flags	N, Z, C

34.

DEC Y	
Code	0110 1011
Operation	$Y - 1 \rightarrow Y$
Flags	N, Z, C

35.

DEC (X)	
Code	0110 1110
Operation	$(X) - 1 \rightarrow (X)$
Flags	N, Z, C

36.

DEC (Y)	
Code	0110 1111
Operation	$(Y) - 1 \rightarrow (Y)$
Flags	N, Z, C

37.

DEC label	
Code	0110 1100 zzzz zzzz
Operation	$(zzzz\ zzzz)-1 \rightarrow (zzzzzzzz)$
Flags	N, Z, C

38.

EOR X	
Code	0101 1010
Operation	$X \ \forall \ A \rightarrow A$
Flags	N, Z

39.

EOR Y	
Code	0101 1011
Operation	$Y \ \forall \ A \rightarrow A$
Flags	N, Z

40.

EOR (X)	
Code	0101 1110
Operation	$(X) \ \forall \ A \rightarrow A$
Flags	N, Z

41.

EOR (Y)	
Code	0101 1111
Operation	$(Y) \ \forall \ A \rightarrow A$
Flags	N, Z

42.

EOR label	
Code	0101 1100 zzzz zzzz
Operation	$(zzzz\ zzzz) \forall \ A \rightarrow A$
Flags	N, Z

43.

EOR #CONSTANT	
Code	0101 1001 zzzz zzzz
Operation	$zzzz\ zzzz \ \forall \ A \rightarrow A$
Flags	N, Z

44.

INC A	
Code	0110 0000
Operation	$A + 1 \rightarrow A$
Flags	N, Z, C

45.

INC X	
Code	0110 0010
Operation	$X + 1 \rightarrow X$
Flags	N, Z, C

46.

INC Y	
Code	0110 0011
Operation	$Y + 1 \rightarrow Y$
Flags	N, Z, C

47.

INC (X)	
Code	0110 0110
Operation	$(X) + 1 \rightarrow X$
Flags	N, Z, C

48.

INC (Y)	
Code	0110 0111
Operation	$(Y) + 1 \rightarrow Y$
Flags	N, Z, C

49.

INC label	
Code	0110 0100 zzzz zzzz
Operation	(zzzz zzzz) + 1 → (zzzz zzzz)
Flags	N, Z, C

50.

INT	
Code	0011 0110
Operation	PC LOW → (SP),
	SP-1 → SP
	PCHIGH→(SP),
	SP-1 → SP
	IPAGE → (SP),
	SP-1 → SP
	PS → (SP),
	SP-1 → SP
	1 → I
	3FC0H → PC
	3 → iPAGE,PAGE
Flags	I

51.

JA	
Code	0111 0001
Operation	A →PC[7:0]
Flags	-----

52.

JUMP ADDR14	
Code	10zz zzzz zzzz zzzz
Operation	ADDR14 →PC[13:0]
	If PAGE≠iPAGE PAGE →iPAGE
Flags	-----

53.

MOV A, X	
Code	0000 0010
Operation	A →X
Flags	-----

54.

MOV A, Y	
Code	0000 0011
Operation	A →Y
Flags	-----

55.

MOV A, (X)	
Code	0000 0110
Operation	A →(X)
Flags	-----

56.

MOV A, (Y)	
Code	0000 0111
Operation	A →(Y)
Flags	-----

57.

MOV A label	
Code	0000 0100 zzzz zzzz
Operation	A →(zzzz zzzz)
Flags	-----

58.

MOV X, A	
Code	0001 0000
Operation	X →A
Flags	N, Z

59.

MOV X, Y	
Code	0001 0011
Operation	X →Y
Flags	-----

60.

MOV X, (Y)	
Code	0001 0111
Operation	X →(Y)
Flags	-----

61.

MOV X, label	
Code	0001 0100 zzzz zzzz
Operation	X →(zzzz zzzz)
Flags	-----

62.

MOV Y, A	
Code	0001 1000
Operation	Y →A
Flags	N, Z

63.

MOV Y, X	
Code	0001 1010
Operation	Y →X
Flags	-----

72.

MOV (Y), (X)	
Code	0011 1110
Operation	(Y) →(X)
Flags	-----

64.

MOV Y, (X)	
Code	0001 1110
Operation	Y →(X)
Flags	-----

73.

MOV (Y), label	
Code	0011 1100 zzzz zzzz
Operation	(Y) →(zzzz zzzz)
Flags	-----

65.

MOV Y, label	
Code	0001 1100 zzzz zzzz
Operation	Y →(zzzz zzzz)
Flags	-----

74.

MOV label, A	
Code	0010 0000 zzzz zzzz
Operation	(zzzz zzzz) →A
Flags	N, Z

66.

MOV (X), A	
Code	0011 0000
Operation	(X) →A
Flags	N, Z

75.

MOV label, X	
Code	0010 0010 zzzz zzzz
Operation	(zzzz zzzz) →X
Flags	-----

67.

MOV (X), Y	
Code	0011 0011
Operation	(X) →Y
Flags	-----

76.

MOV label, Y	
Code	0010 0011 zzzz zzzz
Operation	(zzzz zzzz) →Y
Flags	-----

68.

MOV (X), (Y)	
Code	0011 0111
Operation	(X) →(Y)
Flags	-----

77.

MOV label, (X)	
Code	0010 0110 zzzz zzzz
Operation	(zzzz zzzz) →(X)
Flags	-----

69.

MOV (X), label	
Code	0011 0100 zzzz zzzz
Operation	(X) →(zzzz zzzz)
Flags	-----

78.

MOV label, (Y)	
Code	0010 0111 zzzz zzzz
Operation	(zzzz zzzz) →(Y)
Flags	-----

70.

MOV (Y), A	
Code	0011 1000
Operation	(Y) →A
Flags	N, Z

79.

MOV #CONSTANT, A	
Code	0000 1000 zzzz zzzz
Operation	Zzzz zzzz →A
Flags	N, Z

71.

MOV (Y), X	
Code	0011 1010
Operation	(Y) →X
Flags	-----

80.

MOV #CONSTANT, X	
Code	0000 1010 zzzz zzzz
Operation	Zzzz zzzz →X
Flags	-----

81.

MOV #CONSTANT, Y	
Code	0000 1011 zzzz zzzz
Operation	Zzzz zzzz →Y
Flags	-----

82.

MOV #CONSTANT, (X)	
Code	0000 1110 zzzz zzzz
Operation	Zzzz zzzz →(X)
Flags	-----

83.

MOV #CONSTANT, (Y)	
Code	0000 1111 zzzz zzzz
Operation	zzzz zzzz →(Y)
Flags	-----

84.

NOP	
Code	0000 0000
Operation	No operation
Flags	-----

85.

OR X	
Code	0101 0010
Operation	X V A→A
Flags	N, Z

86.

OR Y	
Code	0101 0011
Operation	Y V A→A
Flags	N, Z

87.

OR (X)	
Code	0101 0110
Operation	(X) V A→A
Flags	N, Z

88.

OR (Y)	
Code	0101 0111
Operation	(Y) V A→A
Flags	N, Z

89.

OR label	
Code	0101 0100 zzzz zzzz
Operation	(zzzz zzzz)V A→A
Flags	N, Z

90.

OR #CONSTANT	
Code	0101 0001 zzzz zzzz
Operation	Zzzz zzzzV A→A
Flags	N, Z

91.

POP	
Code	0011 1111
Operation	SP+1→SP
	(SP)→A
Flags	-----

92.

PSHPAGE	
Code	0110 1101
Operation	PAGE→ (SP); SP-1→SP
Flags	-----

93.

PUSH	
Code	0110 1001
Operation	A→(SP),SP-1→SP
Flags	-----

94.

ROL A	
Code	0111 0000
Operation	C←A←C
Flags	N, Z, C

95.

ROL X	
Code	0111 0010
Operation	C←X←C
Flags	N, Z, C

96.

ROL Y	
Code	0111 0011
Operation	C←Y←C
Flags	N, Z, C

97.

ROL (X)	
Code	0111 0110
Operation	C←(X)←C
Flags	N, Z, C

98.

ROL (Y)	
Code	0111 0111
Operation	C←(Y)←C
Flags	N, Z, C

99.

ROL label	
Code	0111 0100 zzzz zzzz
Operation	C←(zzzz zzzz)←C
Flags	N, Z, C

100.

ROM A	
Code	0111 1101
Operation	ROM (BANK,X,A)→A
Flags	-----

101.

ROM Y	
Code	0111 1001
Operation	ROM (BANK,X,Y)→A
Flags	-----

102.

ROMDBL	
Code	0001 1001
Operation	ROM (BANK,X,Y)→B ROM (BANK,X,Y+1)→A
Flags	-----

103.

ROR A	
Code	0111 1000
Operation	C→A→C
Flags	N, Z, C

104.

ROR X	
Code	0111 1010
Operation	C→X→C
Flags	N, Z, C

105.

ROR Y	
Code	0111 1011
Operation	C→Y→C
Flags	N, Z, C

106.

ROR (X)	
Code	0111 1110
Operation	C→(X)→C
Flags	N, Z, C

107.

ROR (Y)	
Code	0111 1111
Operation	C→(Y)→C
Flags	N, Z, C

108.

ROR label	
Code	0111 1100 zzzz zzzz
Operation	C→(zzzz zzzz)→C
Flags	N, Z, C

109.

RTI	
Code	0100 0101
Operation	SP+1→SP
	(SP)→PS;SP+1→1
	(SP)→IPAGE,PAGE;
	SP+1→SP
	(SP)→PCHIGH;
	SP+1→SP
	(SP)→PCLOW
Flags	-----

110.

RTL	
Code	0100 1101
Operation	SP+1→SP
	(SP)→iPAGE,PAGE;
	SP+1→SP
	(SP)→PCHIGH
	SP+1→SP
	(SP)→PCLOW
Flags	-----

111.

RTS	
Code	0101 0101
Operation	SP+1→SP
	(SP)→PCHIGH;
	SP+1→SP
	(SP)→PCLOW
Flags	-----

112.

SETC	
Code	0110 0101
Operation	1→C
Flags	C

113.

SETZ	
Code	0101 1000
Operation	1→Z,0→A,
Flags	N, Z

114.

SKIPC	
Code	0011 0001
Operation	PC+2→PC if C = 1
Flags	-----

115.

SKIPMI	
Code	0001 0110
Operation	PC+2→PC if N = 1
Flags	-----

116.

SKIPNC	
Code	0011 1001
Operation	PC+2→PC if C = 0
Flags	-----

117.

SKIPNZ	
Code	0010 1001
Operation	PC+2→PC if Z = 0
Flags	-----

118.

SKIPPL	
Code	0001 1111
Operation	PC+2→PC if N = 0
Flags	-----

119.

SKIPZ	
Code	0010 0001
Operation	PC+2→PC if Z = 1
Flags	-----

120.

SLEEP	
Code	0000 1100
Operation	Sleep
Flags	-----

121.

STOP	
Code	0010 0100
Operation	Stop
Flags	------

122.

TAPAGE	
Code	0011 1 0101
Operation	A→PAGE
Flags	-----

123.

TZ	
Code	0101 0000
Operation	Z=1 if A = 0
	Z=0 if A ≠ 0
Flags	N, Z

124.

WRITE	
Code	0101 1101
Operation	A→(BANK,X,Y)
Flags	-----

125.

XB	
Code	0010 0101
Operation	B↔A
Flags	-----

126.

XBANK	
Code	0011 0101
Operation	BANK↔A
Flags	-----

127.

XSP	
Code	0011 1101
Operation	SP↔A
Flags	-----

128.

XST	
Code	0010 1101
Operation	PS↔A
Flags	N, Z, C, I

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings:

1. VDD   7.0V
2. VIH   VDD + 0.3V
3. VIL   VSS - 0.3V
4. Operating Temperature   0°C to + 60°C
5. Storage Temperature   -50°C to + 150°C

Recommended Operating:

		MIN	TYP	MAX	Unit
1. Operating Voltage (VDD)		2.4	3.0	5.5	V
2. Operating Frequency (Fosc)		-	4.0	-	MHz
3. Input Voltage					
3.1 VDD = 2.4V	VIH	1.6	2.0	2.4	V
	VIL	0	0.4	0.8	V
3.2 VDD = 3.0V	VIH	2.0	2.4	3.0	V
	VIL	0	0.6	1.0	V
3.3 VDD = 5.5V	VIH	3.6	4.0	5.5V	V
	VIL	0	1.5	1.8V	V
4. Output Voltage					
4.1 VDD = 2.4V	VOH	2.0	-	-	V
@1mA	VOL	-	-	0.4	V
4.2 VDD = 3.0V	VOH	2.4	-	-	V
@2mA	VOL	-	-	0.6	V
4.3 VDD = 5.5V	VOH	4.0	-	-	V
@10mA	VOL	-	-	1.5	V
5. Input Current					
VIH = VDD	IH	-	-	0.3	μA (P0, P1 and P3)
		-	-	150	μA (P0 only via internal pull-low resistor)
VIL = OV	IL	-	-	0.3	μA (leakage)
6. Output Current					
6.1 VDD = 2.4V,	IOH@VOH =2.0V	1.0	1.5	-	mA
	IOL@VOL =0.4V	2.0	3.0	-	mA
6.2 VDD = 3.0V,	IOH@VOH =2.4V	1.5	3.5	-	mA
	IOL@VOL =0.6V	3.0	7.0	-	mA
6.3 VDD = 5.5V,	IOH@VOH =4.0V	8	10	-	mA
	IOL@VOL =1.5V	16	20	-	mA
7. Current Dissipation					
7.1 Operating Current @4MHz, 3.0V & Output Pad Load = 50pF		1.0	1.5	4.5	mA
7.2 Operating Current @4MHz, 5.0V & Output Pad Load = 50pF		2.0	3.0	9.0	mA
7.3 Standby Current (OFF mode)		-	1.0	9.0	μA

PAD Co-ordinates

Left column		Right column	
1	A0	61	A16
2	A1	60	A17
3	A2	59	A18
4	A3	58	P43/A19
5	A4	57	$\overline{RD}$
6	A5	56	$\overline{WR}$
7	A6	55	$\overline{CS}1$
8	A7	54	$\overline{CS}2$
9	VDD	53	VDD
10	VSS	52	VSS
11	D0	51	A8
12	D1	50	A9
13	D2	49	A10
14	D3	48	A11
15	D4	47	A12
16	D5	46	A13
17	D6	45	A14
18	D7	44	A15
19	P50		

Y

X

(0,0)

20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43
P51			P00	P01	P02	VDD	VSS	P03	P04	P05	P06	P07	EXT_ADDR	TEST_ROM	VSS	VDD	RESET-	EXT_INT	CLK32I	CLK32O	TEST	P_CLK_O	P_CLK

The substrate of IC should be connected to VSS

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
1	A0	-1773.100	1127.050	41	TEST	1496.500	-1722.550
2	A1	-1773.100	987.050	42	P_CLK_0	1636.500	-1722.550
3	A2	-1773.100	847.050	43	P_CLK	1776.500	-1722.550
4	A3	-1773.100	707.050	44	A15	1766.900	-746.700
5	A4	-1773.100	567.050	45	A14	1766.900	-606.700
6	A5	-1773.100	427.050	46	A13	1766.900	-466.700
7	A6	-1773.100	287.050	47	A12	1766.900	-326.700
8	A7	-1773.100	147.050	48	A11	1766.900	-186.700
9	VDD	-1773.100	7.050	49	A10	1766.900	-46.700
10	VSS	-1773.100	-132.950	50	A9	1766.900	93.300
11	D0	-1773.100	-272.950	51	A8	1766.900	233.300
12	D1	-1773.100	-412.950	52	VSS	1766.900	373.300
13	D2	-1773.100	-552.950	53	VDD	1766.900	513.300
14	D3	-1773.100	-692.950	54	$\overline{CS2}$	1766.900	653.300
15	D4	-1773.100	-832.950	55	$\overline{CS1}$	1766.900	793.300
16	D5	-1773.100	-972.950	56	$\overline{WR}$	1766.900	933.300
17	D6	-1773.100	-1112.950	57	$\overline{RD}$	1766.900	1073.300
18	D7	-1773.100	-1252.950	58	P43/A19	1766.900	1213.300
19	P50	-1773.100	-1512.950	59	A18	1766.900	1353.300
20	P51	-1563.500	-1722.550	60	A17	1766.900	1493.300
21	-	-	-	61	A16	1766.900	1633.300
22	-	-	-				
23	P00	-1143.500	-1722.550				
24	P01	-1003.500	-1722.550				
25	P02	-863.500	-1722.550				
26	VDD	-723.500	-1722.550				
27	VSS	-583.500	-1722.550				
28	P03	-443.500	-1722.550				
29	P04	-303.500	-1722.550				
30	P05	-163.500	-1722.550				
31	P06	-23.500	-1722.550				
32	P07	116.500	-1722.550				
33	EXT_ADDR	256.500	-1722.550				
34	TEST_ROM	396.500	-1722.550				
35	VSS	656.500	-1722.550				
36	VDD	796.500	-1722.550				
37	$\overline{RESET}$	936.500	-1722.550				
38	EXT_INT	1076.500	-1722.550				
39	CLK32I	1216.500	-1722.550				
40	CLK32O	1356.500	-1722.550				

Application Circuit

U5
SCG9800

Pin	Signal
9	VDD
10	GND
11	D0
12	D1
13	D2
14	D3
15	D4
16	D5
17	D6
18	D7
19	P50
20	P51
23	P00
24	P01
56	WR
55	CS1
54	CS2
53	VDD
52	GND
51	A8
50	A9
49	A10
48	A11
47	A12
46	A13
45	A14
44	A15
43	P_CLK
42	P_CLK_O
41	TEST

A7 A6 A5 A4 A3 A2 A1 A0 A16 A17 A18 P43/A19 RD

TEST_ROM EXT_ADDR VDD GND P07 P06 P05 P04 P03 P02 RESET EXT_INT CLK32I CLK32O

WR- CS1- CS2- A8 A9 A10 A11 A12 A13 A14 A15

R2 100K
C3 22p
OPTIONAL

D1 LED
D2 LED
D4 LED
D3 LED

VCC
R3 47K
C4 0.1u

VCC

OPTIONAL
Y1 32768
R1 1M
C1
C2

U4
27C040

Pin	Signal		Pin	Signal
12	A0	O0	13	D0
11	A1	O1	14	D1
10	A2	O2	15	D2
9	A3	O3	17	D3
8	A4	O4	18	D4
7	A5	O5	19	D5
6	A6	O6	20	D6
5	A7	O7	21	D7
27	A8			
26	A9			
23	A10			
25	A11			
4	A12			
28	A13			
29	A14			
3	A15			
2	A16			
30	A17			
31	A18			
22	CE			
24	OE			

RD-

SCORE CONCEPT SEMICONDUCTOR LIMITED		
Title SCG9800 application circuit		
Size A	Document Number SCG9800	Rev 1
Date: Saturday, September 16, 2000	Sheet 1 of 1	