

MOS INTEGRATED CIRCUIT

μ PD72001-11, 72001-A8

MULTI-PROTOCOL SERIAL CONTROLLERS

DESCRIPTION

The μ PD72001-11 is an MPSC (Multi-Protocol Serial Controller) which is a general-purpose communication LSI equipped with two sets of bidirectional parallel/serial converter circuits for data communication. This controller has a transmitter function to convert the parallel data output by a data terminal into serial data and transmit this data to a data transmission system such as a modem, and a receiver function to convert the serial data output by the data transmission system into parallel data.

The MPSC can be used with data communications equipment with a variety of communication modes such as the generally and widely used start-stop synchronization mode, and the HDLC mode which is used for high-speed communication.

The μ PD72001-A8 is a low-voltage model.

For this product, the following documents are separately available. Read these documents as well as this Data Sheet.

- User's Manual (S12472E)
- Application Notes
 - (I) (S12753E)
 - (II) (On preparation)
 - (III) (On preparation)

FEATURES

- Two sets of parallel/serial circuits supporting three modes: start-stop synchronization, character synchronization, and bit synchronization modes
 - Easy application to a system supporting two or more communication protocols such as a protocol converter or ISDN terminal adapter
- DPLL (Digital Phase Locked Loop), baud rate generator, and crystal oscillation circuit for transmission/reception clock
 - Helps reduce cost by decreasing the number of external circuits
- Many variations with power-saving features and small package size
 - Easy application to portable terminals and high-accuracy portable terminals

The features common to the μ PD72001-11 and 72001-A8 are explained as the features of the MPSC in this document.

The information in this document is subject to change without notice.

ORDERING INFORMATION

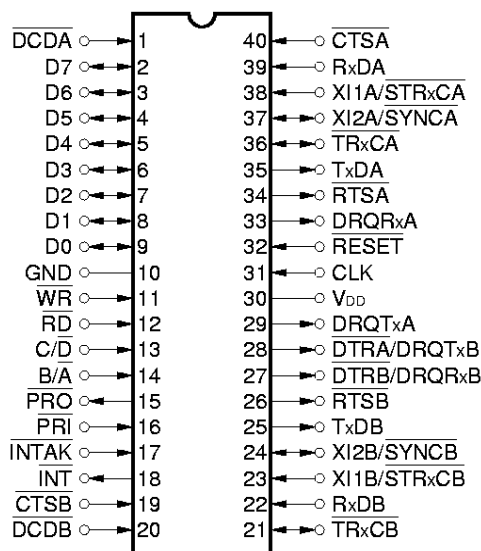
Part Number	Package
μ PD72001C-11	40-pin plastic DIP (600 mil)
μ PD72001G-11-22	44-pin plastic QFP (10 × 10 mm) (resin thickness: 1.45 mm)
μ PD72001GC-11-3B6	52-pin plastic QFP (14 × 14 mm) (resin thickness: 2.7 mm)
μ PD72001L-11	52-pin plastic QFJ (750 × 750 mil)
μ PD72001C-A8	40-pin plastic DIP (600 mil)
μ PD72001G-A8-22	44-pin plastic QFP (10 × 10 mm) (resin thickness: 1.45 mm)
μ PD72001GC-A8-3B6	52-pin plastic QFP (14 × 14 mm) (resin thickness: 2.7 mm)

SPECIFICATIONS

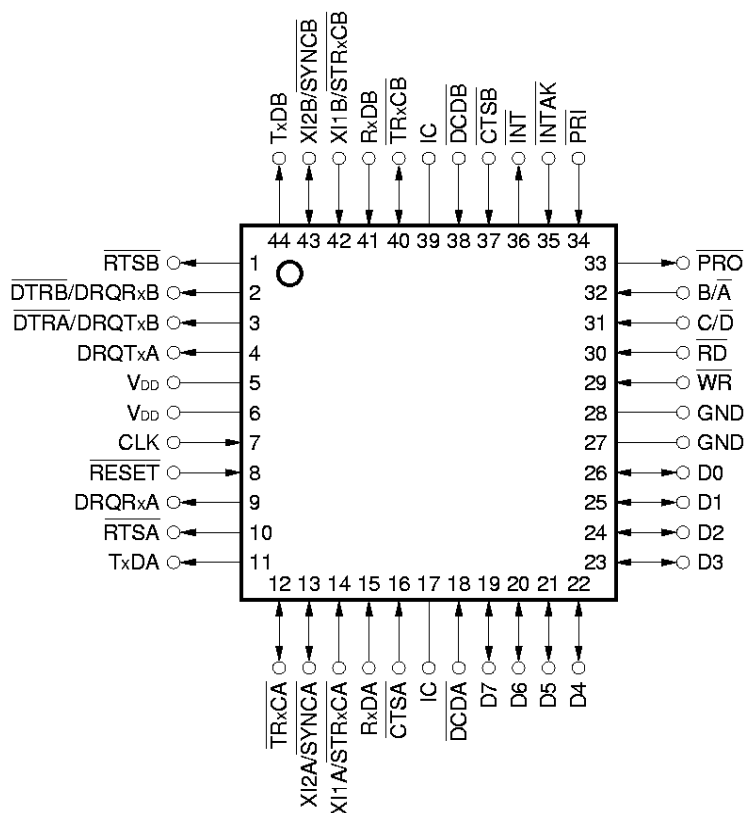
Item	Specifications	
Part number	μPD72001-11	μPD72001-A8
Supply voltage	5 V ±10 %	3.3 V ±0.3 V
System clock frequency	11 MHz MAX.	8 MHz MAX. (at T _A = -10 to +70 °C) 7.14 MHz MAX. (at T _A = -40 to +85 °C)
Maximum transfer rate	2.2 Mbps	1.6 Mbps (at T _A = -10 to +70 °C) 1.43 Mbps (at T _A = -40 to +85 °C)
Process	CMOS	
Internal circuit	Parallel/serial converter circuit: Full-duplex channel × 2 Transmit buffer : Double Receive buffer : Quadruple Interrupt control function DMA request signal output: 2 for transmission, 2 for reception Overrun error detection DPLL Baud rate generator Crystal oscillation circuit for transmission/reception clock generation Self-loopback test function Standby function General-purpose I/O pin: 4 pins × 2	
Communication protocol	Start-stop synchronization	Character bit length: 5, 6, 7, 8 Stop bit length: 1, 1.5, 2 Clock rate: ×1, ×16, ×32, ×64 Parity generation, check Framing error detection Break generation, detection
	COP (Character Oriented Protocol)	Operation mode: Mono-sync, Bi-sync, External sync Character bit length: 5, 6, 7, 8 SYNC character bit length: 6, 8 Character synchronization: Internal/external BCS (Block Check Sequence) generation, check: CRC-16 CRC-CCITT Parity generation, check SYNC character automatic transmission, detection, rejection
	BOP (Bit Oriented Protocol)	Operation mode: HDLC (High-level Data Link Control) SDLC (Synchronous Data Link Control) SDLC Loop Flag transmission, detection Zero insertion, rejection Address field detection (1 byte) FCS (Frame Check Sequence) generation, detection Short frame detection Abort automatic transmission, detection Idle detection Go Ahead detection Transmit number data control
Processing data format	Encode/decode of NRZ (Non-Return to Zero) Encode/decode of NRZI (Non-Return to Zero Inverted) Encode/decode of FM (Frequency Modulation) Decode in Manchester mode	

PIN CONFIGURATION (Top View)

- 40-pin plastic DIP (600 mil) : μPD72001C-11, μPD72001C-A8

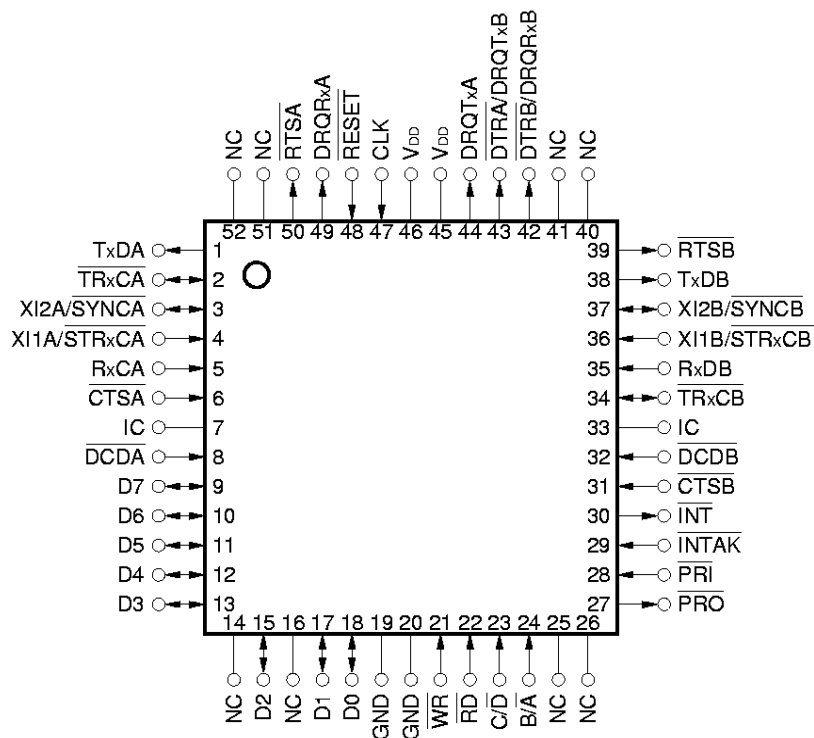


- 44-pin plastic QFP (10 × 10 mm) : μPD72001G-11-22, μPD72001G-A8-22



IC: Internally Connected (Leave this pin unconnected)

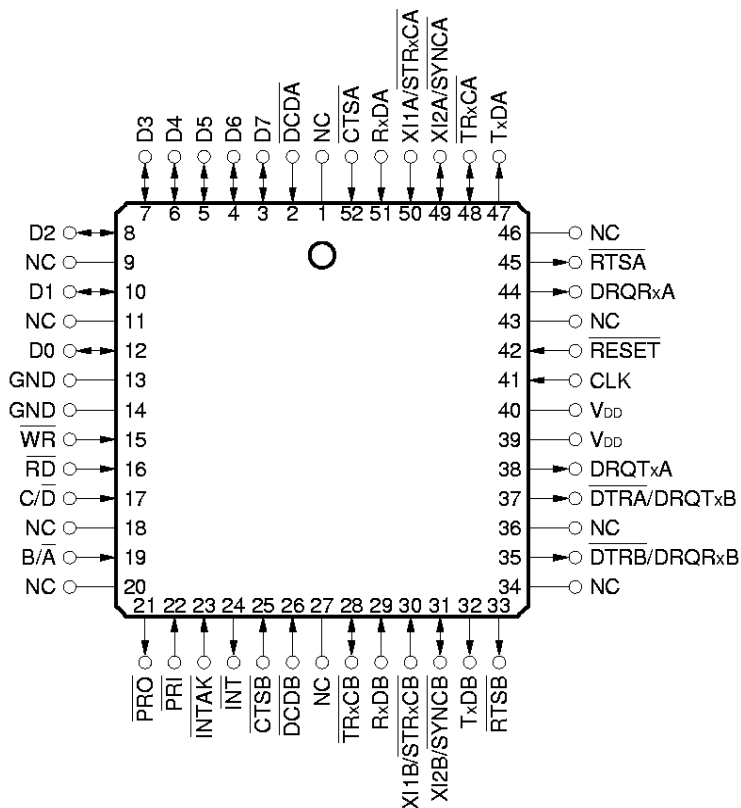
- 52-pin plastic QFP (14 × 14 mm) : μPD72001GC-11-3B6, μPD72001GC-A8-3B6



NC: No Connection

IC : Internally Connected (Leave this pin unconnected.)

- 52-pin plastic QFJ (750 × 750 mil) : μPD72001L-11



The diagram illustrates the internal architecture of the AT91SAM7S64 microcontroller. It features a central **Internal Bus** connecting various components. On the left, the **System CLK** provides a clock signal to the **CLK/Stby Cont.** block. This block, along with the **DB Buf.** (Data Buffer), **RD/WR Cont.** (Read/Write Controller), **DMA Cont.** (Direct Memory Access Controller), and **INT Cont.** (Interrupt Controller), forms the **Interface Cont.** (Interface Controller). The **Internal Bus** also connects to the **CR/SR** (Control/Status Register) block, which includes **CR 0-5**, **SR 12-15**, and **BRG -H, L** (Base Register High/Low). The **CR/SR** block is connected to the **CR 0-5** and **SR 12-15** registers. The **CR/SR** block is also connected to the **CR 6-7** register. The **CR 6-7** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 8-9** register. The **CR 8-9** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 10-11** register. The **CR 10-11** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 12-15** register. The **CR 12-15** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 16-17** register. The **CR 16-17** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 18-19** register. The **CR 18-19** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 20-21** register. The **CR 20-21** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 22-23** register. The **CR 22-23** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 24-25** register. The **CR 24-25** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 26-27** register. The **CR 26-27** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 28-29** register. The **CR 28-29** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 30-31** register. The **CR 30-31** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 32-33** register. The **CR 32-33** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 34-35** register. The **CR 34-35** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 36-37** register. The **CR 36-37** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 38-39** register. The **CR 38-39** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 40-41** register. The **CR 40-41** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 42-43** register. The **CR 42-43** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 44-45** register. The **CR 44-45** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 46-47** register. The **CR 46-47** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 48-49** register. The **CR 48-49** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 50-51** register. The **CR 50-51** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 52-53** register. The **CR 52-53** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 54-55** register. The **CR 54-55** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 56-57** register. The **CR 56-57** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 58-59** register. The **CR 58-59** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 60-61** register. The **CR 60-61** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 62-63** register. The **CR 62-63** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 64-65** register. The **CR 64-65** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 66-67** register. The **CR 66-67** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 68-69** register. The **CR 68-69** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 70-71** register. The **CR 70-71** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 72-73** register. The **CR 72-73** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 74-75** register. The **CR 74-75** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 76-77** register. The **CR 76-77** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 78-79** register. The **CR 78-79** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 80-81** register. The **CR 80-81** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 82-83** register. The **CR 82-83** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 84-85** register. The **CR 84-85** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 86-87** register. The **CR 86-87** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 88-89** register. The **CR 88-89** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 90-91** register. The **CR 90-91** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 92-93** register. The **CR 92-93** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 94-95** register. The **CR 94-95** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 96-97** register. The **CR 96-97** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 98-99** register. The **CR 98-99** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 100-101** register. The **CR 100-101** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 102-103** register. The **CR 102-103** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 104-105** register. The **CR 104-105** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 106-107** register. The **CR 106-107** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 108-109** register. The **CR 108-109** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 110-111** register. The **CR 110-111** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 112-113** register. The **CR 112-113** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 114-115** register. The **CR 114-115** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 116-117** register. The **CR 116-117** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 118-119** register. The **CR 118-119** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 120-121** register. The **CR 120-121** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 122-123** register. The **CR 122-123** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 124-125** register. The **CR 124-125** register is connected to the **CR/SR** block. The **CR/SR** block is also connected to the **CR 126-127** register. The **CR 126-127** register is connected to the **CR/SR** block. The **CR/SR</**

1. PIN FUNCTIONS

The functions of the MPSC can be broadly classified into "system interface functions" that control interfacing with the host system, and "transmission/reception functions" to transmit or receive data. This section explains the functions of the pins of the MPSC by classifying the pins into those related to system interfacing and those related to transmission and reception.

Hereafter, "H" (voltage level satisfying V_{IH} in the case of an input pin, or voltage level satisfying V_{OH} in the case of an output pin) and "L" (voltage level satisfying V_{IL} in the case of an input pin, or voltage level satisfying V_{OL} in the case of an output pin) are used to indicate the input/output status of a pin.

1.1 Pins Related to System Interface

(1) V_{DD}
Supply voltage pin

(2) GND
GND pin

(3) $\overline{\text{RESET}}$... Input

This pin inputs a signal from an external device to reset the MPSC. When "L" is input to this pin for the duration of 2 clock cycles ($2t_{CLK}$) or longer, the MPSC is reset (this is called system reset).

As a result of system reset, the transmitter, receiver, and interrupt/DMA functions of the MPSC are disabled, and the TxD pin and general-purpose output pins go high. In this case, because all bits of the control register (CR) are also reset, CR must be set again if a system reset has been executed.

Table 1-1 shows the status of each pin at system reset, in comparison with the pin status at channel reset (CR0: D5, D4, D3 = "0, 1, 1").

The MPSC automatically enters the standby mode at system reset, lowering the power consumption from that in the normal operation mode.

Table 1-1. Pin Status at Reset

Pin Name	I/O	Pin Status	
		$\overline{\text{RESET}}$ (system reset)	Channel reset
$\overline{\text{WR}}$	I	–	–
$\overline{\text{RD}}$	I	–	–
$\text{B}/\overline{\text{A}}$	I	–	–
$\text{C}/\overline{\text{D}}$	I	–	–
D7 to D0	I/O	–	–
$\overline{\text{INT}}$	O	High impedance	High impedance
$\overline{\text{INTAK}}$	I	–	–
$\overline{\text{PRI}}$	I	–	–
$\overline{\text{PRO}}$	O	Depends on $\overline{\text{PRI}}$	Depends on $\overline{\text{PRI}}$
DRQTxA	O	"L"	"L"
DRQRxA	O	"L"	"L"
$\overline{\text{DTRA}}/\text{DRQTxB}$, $\overline{\text{DTRB}}/\text{DRQRxB}$	O	$\overline{\text{DTR}}$ function, "H"	Retains current status
TxDA , TxDB	O	"H"	"H"
RxDA , RxDB	I	–	–
$\overline{\text{TRxCA}}$, $\overline{\text{TRxCB}}$	I/O	Input status	Retains current status
$\text{XI1A}/\overline{\text{STRxCA}}$ $\text{XI1B}/\overline{\text{STRxCB}}$	I	–	–
$\text{XI2A}/\overline{\text{SYNCA}}$ $\text{XI2B}/\overline{\text{SYNCB}}$	I/O	Input status	Retains current status
$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$	O	"H"	"H"
$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$	I	–	–
$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$	I	–	–

– : Undefined

(4) CLK (System Clock) ... Input

This pin inputs the system clock. The input frequency must be five times that of the data transfer rate or higher.

(5) $\overline{\text{WR}}$ (Write) ... Input

This pin inputs a write control signal for control words and transmit data. This pin is active-low.

(6) $\overline{\text{RD}}$ (Read) ... Input

This pin inputs a read control signal for status and receive data. This pin is active-low.

(7) $\text{B}/\overline{\text{A}}$ (Channel B/Channel A) ... Input

This pin inputs a signal to select a channel to be accessed when data is written or read. When this pin is "L", channel A is selected; when it is "H", channel B is selected.

(8) $\text{C}/\overline{\text{D}}$ (Control/Data) ... Input

This pin inputs a signal that determines the type of the data on the data bus when the data is written or read.

Table 1-2 shows the selection operations by $\overline{WR}$, $\overline{RD}$, $B/\overline{A}$, and $C/\overline{D}$.

Table 1-2. MPSC Control Signals and Operations

$\overline{WR}$	$\overline{RD}$	$B/\overline{A}$	$C/\overline{D}$	Operation	
L	H	L	L	Channel A	Writes transmit data to Tx buffer
		H		Channel B	
H	L	L	L	Channel A	Reads receive data from Rx buffer
		H		Channel B	
L	H	L	H	Channel A	Writes control register
		H		Channel B	
H	L	L	H	Channel A	Reads status register
		H		Channel B	
H	H	×	×	High-impedance state or $\overline{INTAK}$ sequence	
L	L	×	×	Setting prohibited	

× : Don's Care

(9) D7 through D0 (Data Bus) ... I/O

These pins constitute a three-state 8-bit bidirectional data bus. This data bus is connected to the data bus of the host processor to transfer control words, status, and transmit/receive data.

(10) $\overline{INT}$ (Interrupt) ... Output (open drain)

This pin outputs an interrupt request signal. If an interrupt occurs in the MPSC, it goes low (active). Because this is an open-drain output pin, it must be pulled up.

(11) $\overline{INTAK}$ (Interrupt Acknowledge) ... Input

This pin inputs a signal to acknowledge interrupt request signals issued by the MPSC. This pin is active-low. This pin is used when the vector mode (CR2A: D7 = "1") is selected, and must be pulled up to "H" when the non-vector mode (CR2A: D7 = "0") is selected.

(12) $\overline{PRI}$ (Priority Input) ... Input

This input pin is used for an interrupt generation request signal and for an output control signal for interrupt vectors. In the normal operation mode, this pin provides an interrupt generation control function. During the $\overline{INTAK}$ sequence, it provides an output control function for interrupt vectors. How this pin is used differs depending on the interrupt mode.

(a) In vector mode (CR2A: D7 = "1")

In the normal operation mode, the $\overline{PRI}$ pin is used to control generation of interrupts. When interrupt vector output mode of Type A-3 or Type B-2 (CR2A: D5, D4, D3 = "0, 1, 0" or "1, 0, 0") is selected, interrupts can be generated regardless of whether the $\overline{PRI}$ pin is "L" or "H".

If any other interrupt vector output mode is selected, the $\overline{PRI}$ pin must be kept "L" to enable generation of interrupts.

During the $\overline{INTAK}$ sequence, an interrupt vector is output if "L" is input to the $\overline{PRI}$ pin in any interrupt vector output mode, and output of the interrupt vector is disabled if "H" is input to $\overline{PRI}$.

(b) Non-vector mode (CR2A: D7 = "0")

In this mode, the $\overline{\text{PRI}}$ pin controls only the generation of interrupts because the INTAK sequence is not used. If an interrupt vector output mode other than Type A-3 and Type B-2 is selected, generation of an interrupt signal is enabled if "L" is input to the $\overline{\text{PRI}}$ pin. The interrupt signal is not generated if "H" is input to $\overline{\text{PRI}}$. If an interrupt daisy chain is configured, inputting "L" to this pin indicates that a device having a higher priority does not acknowledge interrupt processing or does not have an interrupt request, and only the MPSC with "L" input to its $\overline{\text{PRI}}$ pin can generate an interrupt.

(13) $\overline{\text{PRO}}$ (Priority Output) ... Output

This pin is used when an interrupt daisy chain is configured. This output pin is active-low, and controls generation of interrupts requests from a device with a lower priority. Usually, this pin is used along with the $\overline{\text{PRI}}$ pin, and its operation is as follows:

When $\overline{\text{PRI}}$ = "H", $\overline{\text{PRO}}$ = "H"

When $\overline{\text{PRI}}$ = "L", $\overline{\text{PRO}}$ goes "H" if there is an interrupt request, and goes "L" if there is no interrupt request.

(14) DRQTxA (DMA Request TxA) ... Output

This pin outputs a DMA request to a DMA controller. This pin is active-high. It goes "H" if the transmitter of channel A has entered the Tx Buffer Empty status. The condition under which this pin goes "H" differs as follows depending on the setting of the CR1 and D2 bits.

CR1: D2 = "0": The DRQTxA pin goes "H" when the transmitter has entered the Tx Buffer Empty status after the first transmit data has been written. It does not go "H" when the transmitter has entered the Tx Buffer Empty status after reset.

CR1: D2 = "1": The DRQTxA pin goes "H" when the transmitter has entered the Tx Buffer Empty status. This signal is reset when transmit data has been written to channel A.

(15) DRQRxA (DMA Request RxA) ... Output

This pin outputs a DMA request to a DMA controller. This pin is active-high and goes "H" if the receiver of channel A has entered the Rx Character Available status. This signal is reset only when receive data has been read from channel A.

(16) $\overline{\text{DTRA}}$ /DRQTxB (Data Terminal Ready A/DMA Request TxB) ... Output

The function of this pin is changed as follows depending on the setting of CR2A: D1 and D0.

(a) When CR2A: D1, D0 = "0, 0" or "0, 1"

This pin functions as the $\overline{\text{DTRA}}$ pin. This pin is a general-purpose output pin and can be used to control a modem, etc. The operation of the $\overline{\text{DTRA}}$ pin is as follows:

When CR5A: D7 = "0", $\overline{\text{DTRA}}$ = "H"

When CR5A: D7 = "1", $\overline{\text{DTRA}}$ = "L"

(b) When CR2A: D1, D0 = "1, 0"

This pin functions as the DRQTxB output pin. The function of this pin is the same as the DRQTxA pin, except this pin is used with channel B.

(17) $\overline{\text{DTRB}}$ /DRQRxB (Data Terminal Ready B/DMA Request RxB) ... Output

The function of this pin changes as follows depending on the setting of CR2A: D1 and D0.

- (a) When CR2A: D1, D0 = "0, 0" or "0, 1"

This pin functions as the $\overline{\text{DTRB}}$ output pin. The function of this pin is the same as the $\overline{\text{DTRA}}$ pin, except this pin is used with channel B.

- (b) When CR2A: D1, D0 = "1, 0"

This pin functions as the DRQRxB output pin. The function of this pin is the same as the DRQRxA pin, except this pin is used with channel B.

- (18) $\overline{\text{CTS}}$ A (Clear to Send A) and $\overline{\text{CTS}}$ B (Clear to Send B) ... Input

This pin is a general-purpose input pin and can be used to control a modem, etc. Changes in the status of this pin affect the latching operation of the E/S bit. When E/S INT is enabled (CR1: D0 = "1"), the E/S interrupt is generated.

If the Auto Enable mode (CR3: D5 = "1") is set, the transmitter can be controlled by using the Tx Enable bit (CR5: D3) and this pin. This is illustrated in Table 1-3.

Table 1-3. Auto Enable Mode and $\overline{\text{CTS}}$ Pin

$\overline{\text{CTS}}$ Pin	Tx Enable Bit	Transmitter Status
L	1	Enabled
H	1	Disabled
H or L	0	Disabled

- (19) $\overline{\text{DCDA}}$ (Data Carrier Detect A) ... Input

$\overline{\text{DCDB}}$ (Data Carrier Detect B) ... Input

These are general-purpose input pins and can be used to control a modem, etc. Changes in the status of this pin affect the latching operation of the E/S bit. When E/S INT is enabled (CR1: D0 = "1"), the E/S interrupt is generated.

If the Auto Enable mode (CR3: D5 = "1") is set, the receiver can be controlled by using the Rx Enable bit (CR3: D0) and this pin. This is illustrated in Table 1-4.

Table 1-4. Auto Enable Mode and $\overline{\text{DCD}}$ Pin

$\overline{\text{DCD}}$ Pin	Rx Enable Bit	Receiver Status
L	1	Enabled
H	1	Disabled
H or L	0	Disabled

- (20) $\overline{\text{RTSA}}$ (Request to Send A) ... Output

$\overline{\text{RTSB}}$ (Request to Send B) ... Output

These are general-purpose output pins and can be used to control a modem, etc. The operations of these pins differ depending on the setting of the operation protocol and the setting of the Auto Enable bit, as shown in Table 1-5.

Table 1-5. Auto Enable Bit and $\overline{\text{RTS}}$ Pin

Function Protocol	Auto Enable Bit	RTS Cont. Bit	$\overline{\text{RTS}}$ Pin Status
Start-stop synchronization	0	0	H
		1	L
	1	When "0" from beginning	H
		If set to "1" once and then reset to "0"	If "L" while All Sent ^{Note} = "0", and "H" if All Sent = "1"
COP/BOP	Don't Care	1	L
		0	H
		1	L
		0	H

Note SR1: D2

1.2 Pins Related to Transmission/Reception

- (1) TxDA (Transmit Data A) and TxDB (Transmit Data B) ... Output

These pins output transmit data.

- (2) RxDA (Receive Data A) and RxDB (Receive Data B) ... Input

These pins input receive data.

- (3) XI1A/ $\overline{\text{STRxC A}}$ (Crystal Input 1A/Source of Transmit Receive Clock A) ... Input

XI1B/ $\overline{\text{STRxC B}}$ (Crystal Input 1B/Source of Transmit Receive Clock B) ... Input

The functions of these pins change depending on the setting of CR15: D7.

- (a) When CR15: D7 = "0"

These pins function as the $\overline{\text{STRxC}}$ pins, and input the transmission and reception clocks, or input source clocks to the internal BRG (Baud Rate Generator) and DPLL (Digital Phase Locked Loop).

- (b) When CR15: D7 = "1"

These pins function as XI1 pins and connect one end of the crystal for transmission/reception clock source oscillation.

- (4) XI2A/ $\overline{\text{SYNC A}}$ (Crystal Input 2A/Synchronization A) ... I/O

XI2B/ $\overline{\text{SYNC B}}$ (Crystal Input 2B/Synchronization B) ... I/O

The functions of these pins change depending on the setting of CR15: D7.

- (a) When CR15: D7 = 0

These pins function as $\overline{\text{SYNC}}$ pins. The functions of the $\overline{\text{SYNC}}$ pins differ as shown in Table 1-6, depending on the setting of CR4.

- (b) When CR15: D7 = "1"

These pins function as XI2 pins and connect one end of the crystal for transmission/reception clock source oscillation.

Table 1-6. Functions of $\overline{\text{SYNC}}$ Pins and Setting of CR4 (when CR15: D7 = "0")

Operation Protocol	Synchronization Detection Mode	$\overline{\text{SYNC}}$ Pin Function	CR4						Function
			D7	D6	D5	D4	D3	D2	
Start-stop synchronization		Input	×		×		0 1 1	1 0 1	The $\overline{\text{SYNC}}$ pins function as general-purpose input pins. Changes in the status of these pin ("H" → "L" or "L" → "H") affect the latch operation of the Sync/Hunt bit (SR1: D4), and cause the E/S interrupt.
COP	Internal synchronization	Output	×		0 0	0 1			If a SYNC character is detected in the receive character, the SYNC pins go "L" for the duration of 1RxC cycle.
	External synchronization	Input	0 0	0 1	1 1	1 1	0 0	0 0	
									The $\overline{\text{SYNC}}$ pins input a signal for establishing character synchronization. When these pins go "L" from "H", execution exits from the Hunt Phase and character synchronization is established. While SYNC input is "L", character synchronization is maintained. Assembling a receive character is started at the rising edge of the receive clock preceding the falling of the SYNC input.
BOP		No function	×		1 0				The $\overline{\text{SYNC}}$ pins do not function.

× : Don't Care

Caution If a pattern in which 1 bit ("0" or "1") is inserted in between the "Sync character assigned to CR7" and "Sync character assigned to CR6" is received while data is being assembled in the Bi-Sync mode, an "L" pulse of about 1 bit may be generated on the $\overline{\text{SYNC}}$ pin. If the Enter Hunt command is issued while this "L" pulse is present, the command is invalid. However, the receive operation of the MPSC is not affected at all by the reception of this pattern.

- (5) $\overline{\text{TRxCA}}$ (Transmit Receive Clock A) ... I/O
 $\overline{\text{TRxCB}}$ (Transmit Receive Clock B) ... I/O

- (a) When CR15: D2 = "0"

These pins input the transmit and receive clocks. They are used to supply external transmit and receive clocks.

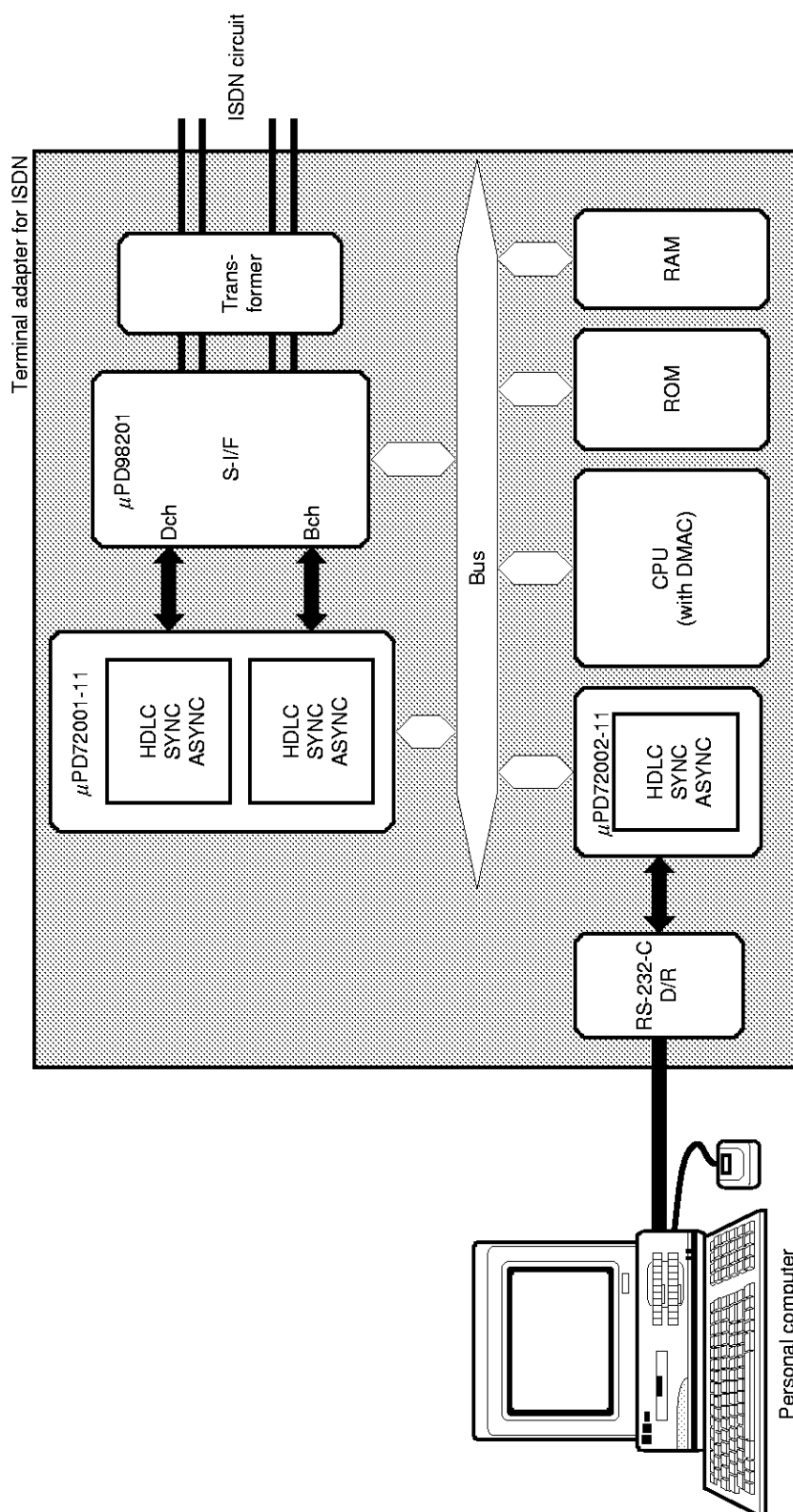
[Exception] If either CR15: D6, D5 = "0, 1" or D4, D3 = "0, 1", or both are set, the $\overline{\text{TRxCA}}$ and $\overline{\text{TRxCB}}$ pins function as input pins, even if CR15: D2 = "1".

- (b) When CR15: D2 = "1"

These pins function as output pins. The source of the output clock can be selected from a crystal oscillation circuit, BRG, DPLL, or transmit clock, depending on the setting of CR15: D1, D0. Under the conditions explained in [Exception] in (a) above, they unconditionally serve as input pins, and the setting of CR15: D2, D1, D0 is invalid.

2. SYSTEM CONFIGURATION EXAMPLE

An example of a system where the μ PD72001-11 is used for a terminal adapter for ISDN is shown below.



3. ELECTRICAL SPECIFICATIONS

(1) μ PD72001-11

Absolute Maximum Ratings ($T_A = 25\text{ }^\circ\text{C}$)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +7.0	V
Input voltage	V_I		-0.5 to $V_{DD} + 0.5$	V
Output voltage	V_O		-0.5 to $V_{DD} + 0.5$	V
Operating temperature	T_A		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-65 to +150	$^\circ\text{C}$

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

DC Characteristics

μ PD72001-11 ($T_A = -40\text{ to }+85\text{ }^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}	CLK, $\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$	3.3		$V_{DD} + 0.5$	V
	V_{IH}	Other pins	2.2		$V_{DD} + 0.5$	V
Low-level input voltage	V_{IL}	CLK, $\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$	-0.5		+0.6	V
	V_{IL}	Other pins	-0.5		+0.8	V
High-level output voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	0.7 V_{DD}			V
Low-level output voltage	V_{OL}	$I_{OL} = 2.0\text{ mA}$			0.45	V
High-level input leakage current	I_{LH}	$V_I = V_{DD}$			10	μA
Low-level input leakage current	I_{LIL}	$V_I = 0\text{ V}$			-10	μA
High-level output leakage current	I_{LOH}	$V_O = V_{DD}$			10	μA
Low-level output leakage current	I_{LOL}	$V_O = 0\text{ V}$			-10	μA
Supply current	I_{DD}	At 11 MHz		20	40	mA
		In standby mode ^{Note}			1	mA

Note System clock : 11 MHz
 Input pin : Inactive
 • High-level input voltage : ($V_{DD} - 0.3\text{ V}$) to ($V_{DD} + 0.5\text{ V}$)
 • Low-level input voltage : 0 V to 0.3 V
 Output pin : Leave unconnected.

Capacitance ($T_A = 25\text{ °C}$, $V_{DD} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{IN}	$f_c = 1\text{ MHz}$ Pins other than test pin: 0 V		10	pF
I/O capacitance	C_{IO}			20	pF

AC Characteristics

μPD72001-11 ($T_A = -40\text{ to }+85\text{ °C}$, $V_{DD} = 5\text{ V} \pm 10\%$)

System interface:

Parameter	Symbol	Condition	Rated Value		Unit
			MIN.	MAX.	
Clock cycle	t_{CYK}		90	2 000	ns
Clock high-pulse width	t_{WKH}		40	1 000	ns
Clock low-pulse width	t_{WKL}		40	1 000	ns
Clock rise time	t_{KR}	1.5 V → 3.0 V		10	ns
Clock fall time	t_{KF}	3.0 V → 1.5 V		10	ns
Address setup time (vs. $\overline{RD} \downarrow$)	t_{SAR}		0		ns
Address hold time (vs. $\overline{RD} \uparrow$)	t_{HRA}		0		ns
$\overline{RD}$ pulse width	t_{WRL}		120		ns
Address → data output delay time	t_{DAD}	$T_A = -10\text{ to }+70\text{ °C}$		100	ns
		$T_A = -40\text{ to }+85\text{ °C}$		110	
$\overline{RD} \rightarrow$ data output delay time	t_{DRD}	$T_A = -10\text{ to }+70\text{ °C}$		100	ns
		$T_A = -40\text{ to }+85\text{ °C}$		110	
$\overline{RD} \rightarrow$ data float delay time	t_{FRD}		10	85	ns
Address setup time (vs. $\overline{WR} \downarrow$)	t_{SAW}		0		ns
Address hold time (vs. $\overline{WR} \uparrow$)	t_{HWA}		0		ns
$\overline{WR}$ pulse width	t_{WWL}		120		ns
Data setup time (vs. $\overline{WR} \uparrow$)	t_{SDW}	$T_A = -10\text{ to }+70\text{ °C}$	100		ns
		$T_A = -40\text{ to }+85\text{ °C}$	90		
Data hold time (vs. $\overline{WR} \uparrow$)	t_{HWA}		0		ns
Recovery time between $\overline{RD}$ and $\overline{WR}$	t_{RV}		140		ns

Serial control:

Parameter		Symbol	Condition	Rated Value		Unit
				MIN.	MAX.	
Transmit/receive data cycle		t _{CYD}		5		t _{cyk}
$\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$ input clock cycle		t _{CYC}		90		ns
$\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$ input clock pulse width	High	t _{wCH}		40		ns
	Low	t _{wCL}	T _A = −10 to +70 °C	40		ns
			T _A = −40 to +85 °C	45		
$\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$ ↓ → TxD delay time		t _{DTCTD1}	×1 mode, COP, BOP		100	ns
		t _{DTCTD2}	×16, 32, 64 mode		300	ns
$\overline{\text{TRxC}}$ ↓ → TxD delay time		t _{DTCTD3}	$\overline{\text{TRxC}}$ is output	0	100	ns
Rx _D setup time (vs. $\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$ ↑)		t _{SRDRC}	When DPLL is not used	0		ns
Rx _D hold time (vs. $\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$ ↑)		t _{HRCRD}	When DPLL is not used	120		ns
Rx _D → Tx _D delay time		t _{DRD1}	ECHO BACK mode		100	ns
		t _{DRD2}	Without SDLC Loop delay		100	ns
Tx _D → $\overline{\text{INT}}$ delay time		t _{TDIQ}	T _x INT mode	4	6	t _{cyk}
Tx _D → DRQTx delay time		t _{TDQ}	T _x DMA mode	4	6	t _{cyk}
$\overline{\text{RxC}}$ ↑ ^{Note} → $\overline{\text{INT}}$ delay time		t _{DRCIQ}	R _x INT mode	7	11	t _{cyk}
$\overline{\text{RxC}}$ ↑ ^{Note} → DRQR _x delay time		t _{DRCDQ}	R _x DMA mode	7	11	t _{cyk}
$\overline{\text{RD}}$ ↓ → DRQR _x ↓ delay time		t _{DRDQ}			120	ns
$\overline{\text{WR}}$ ↓ → DRQTx ↓ delay time		t _{WDQ}			120	ns

Note Of $\overline{\text{STRxC}}$ and $\overline{\text{TRxC}}$, the one used as the receive clock.

Interrupt control:

Parameter	Symbol	Condition	Rated Value		Unit
			MIN.	MAX.	
$\overline{\text{INTAK}}$ low-pulse width	t _{wIAL}		120		ns
$\overline{\text{INTAK}}$ high-pulse width	t _{wIAH}		120		ns
$\overline{\text{PRI}}$ → $\overline{\text{PRO}}$ delay time	t _{DIPO}			50	ns
$\overline{\text{INT}}$ ↓ → $\overline{\text{PRO}}$ ↑ delay time	t _{DIQPO}		-20	+50	ns
2nd $\overline{\text{INTAK}}$ ↓ → $\overline{\text{INT}}$ ↑ delay time	t _{DIQ}	$\overline{\text{INT}}$ output level = 0.8 V ^{Note}		120	ns
		$\overline{\text{INT}}$ output level = 2.2 V ^{Note}		300	ns
SR2B read $\overline{\text{RD}}$ ↓ → $\overline{\text{INT}}$ ↑ delay time	t _{DRDIQ}	$\overline{\text{INT}}$ output level = 0.8 V ^{Note}		150	ns
		$\overline{\text{INT}}$ output level = 2.2 V ^{Note}		300	ns
$\overline{\text{PRI}}$ setup time (vs. $\overline{\text{INTAK}}$ ↓)	t _{SPIA1}	When vector output is enabled	0		ns
$\overline{\text{PRI}}$ hold time (vs. $\overline{\text{INTAK}}$ ↑)	t _{HIAP1}		20		ns
$\overline{\text{PRI}}$ setup time (vs. $\overline{\text{INTAK}}$ ↓)	t _{SPIA2}	When vector output is disabled	20		ns
$\overline{\text{PRI}}$ hold time (vs. $\overline{\text{INTAK}}$ ↑)	t _{HIAP2}		20		ns
$\overline{\text{INTAK}}$ → data output delay time	t _{DIAD}			120	ns
$\overline{\text{INTAK}}$ → data float delay time	t _{FIAD}		10	85	ns

Note Measured value with 2-k Ω pull-up resistor and 100-pF load capacitance connected

Modem control:

Parameter		Symbol	Condition	Rated Value		Unit
				MIN.	MAX.	
$\overline{\text{CTS}}$, $\overline{\text{DCD}}$, $\overline{\text{SYNC}}$ pulse width	High	t_{WMH}		2		t_{CYK}
	Low	t_{WML}		2		t_{CYK}
$\overline{\text{CTS}}$, $\overline{\text{DCD}}$, $\overline{\text{SYNC}} \rightarrow \overline{\text{INT}}$ delay time		t_{DMIQ}			2	t_{CYK}
$\overline{\text{STRxC}}$, $\overline{\text{TRxC}} \uparrow \rightarrow \overline{\text{SYNC}}$ setup time		T_{SSYRC}	COP external synchronization	0	2	t_{CYK}

Communication control:

Parameter		Symbol	Condition	Rated Value		Unit
				MIN.	MAX.	
Transmit enable command ($\overline{\text{WR}} \uparrow$, $\overline{\text{CTS}} \downarrow$) $\rightarrow$ TxD delay time		t_{DTETD1}	ASYNC, COP		3	t_{CYC}
		t_{DTETD2}	BOP	4	7	t_{CYC}
Receive enable command ($\overline{\text{DCD}} \downarrow$) setup time (vs. start bit, $\overline{\text{STRxC}} \uparrow$, $\overline{\text{TRxC}} \uparrow$ of sync character) ^{Note}		t_{SRERC}		1		t_{CYC}
Receive enable command ($\overline{\text{DCD}} \downarrow$) hold time (vs. $\overline{\text{STRxC}} \uparrow$, $\overline{\text{TRxC}} \uparrow$) ^{Note}		t_{HRCRE1}	ASYNC	7		t_{CYK}
		t_{HRCRE2}	COP	$20t_{\text{CYC}}$ + $8t_{\text{CYK}}$		
		t_{HRCRE3}	BOP	$3t_{\text{CYC}}$ + $8t_{\text{CYK}}$		
Receive clock ($\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$) ^{Note} hold time (vs. stop bit, MSB of CRC, MSB of end flag)		t_{HRDRC1}	ASYNC	1		Bit
		t_{HRDRC2}	COP	22		t_{CYC}
		t_{HRDRC3}	BOP	5		t_{CYC}
Receive clock ($\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$) ^{Note} setup time (vs. start bit, sync character)		t_{SRCRD1}	ASYNC	1		Bit
		t_{SRCRD2}	COP, BOP	1		t_{CYC}

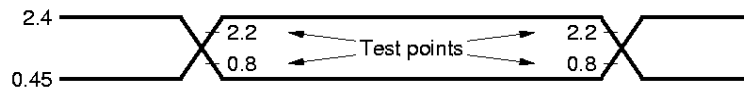
Note Of $\overline{\text{STRxC}}$ and $\overline{\text{TRxC}}$, the one used as the receive clock.

Crystal oscillation and reset

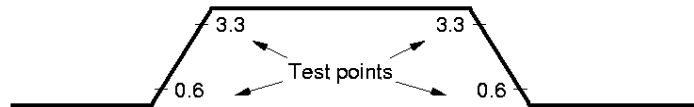
Parameter		Symbol	Condition	Rated Value		Unit
				MIN.	MAX.	
XI1 input cycle time		t_{CYX}		90	2000	ns
$\overline{\text{RESET}}$ pulse width		t_{WRSL}		2		t_{CYK}

Caution The system clock cycle in all modes must be five times that of the data rate.

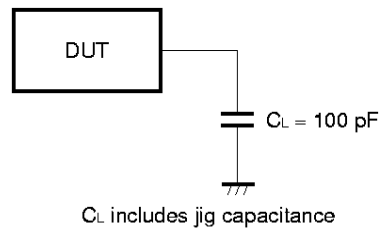
AC Test Input/Output Waveform (except clock)



AC Test Clock Input Waveform



Load Condition



Caution If the load capacitance exceeds 100 pF due to the configuration of the circuit, keep the load capacitance of this device to within 100 pF by inserting a buffer or by some other means.

Remark DUT: Tested device

(2) μ PD72001-A8Absolute Maximum Ratings ($T_A = 25\text{ }^\circ\text{C}$)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +7.0	V
Input voltage	V_I		-0.5 to $V_{DD} + 0.5$	V
Output voltage	V_O		-0.5 to $V_{DD} + 0.5$	V
★ Operating temperature	T_A		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-0 to +150	$^\circ\text{C}$

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

DC Characteristics ($T_A = -40\text{ to }+85\text{ }^\circ\text{C}$, $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IHC}	CLK, $\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$	0.8 V_{DD}		$V_{DD} + 0.5$	V
	V_{IH}	Other pins	1.8		$V_{DD} + 0.5$	V
Low-level input voltage	V_{ILC}	CLK, $\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$	-0.5		0.15 V_{DD}	V
	V_{IL}	Other pins	-0.5		+0.6	V
High-level output voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	2.2			V
Low-level output voltage	V_{OL}	$I_{OL} = 2.0\text{ mA}$			0.5	V
High-level input leakage current	I_{LIH}	$V_I = V_{DD}$			10	μA
Low-level input leakage current	I_{LIL}	$V_I = 0\text{ V}$			-10	μA
High-level output leakage current	I_{LOH}	$V_O = V_{DD}$			10	μA
Low-level output leakage current	I_{LOL}	$V_O = 0\text{ V}$			-10	μA
Supply current	I_{DD}	At 8 MHz		5	20	mA
		In standby mode ^{Note}			1	mA

Note System clock : 8 MHz ($T_A = -10\text{ to }+70\text{ }^\circ\text{C}$)/7.14 MHz ($T_A = -40\text{ to }+85\text{ }^\circ\text{C}$)

Input pin : Inactive

- High-level input voltage : ($V_{DD} - 0.3\text{ V}$) to ($V_{DD} + 0.5\text{ V}$)

- Low-level input voltage : 0 V to 0.3 V

Output pin : Leave unconnected.

Capacitance ($T_A = 25\text{ }^\circ\text{C}$, $V_{DD} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{IN}	$f_c = 1\text{ MHz}$		10	pF
I/O capacitance	C_{IO}	Pins other than test pin: 0 V		20	pF

AC Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 3.3$ V $\pm$ 0.3 V)

★ System interface:

Parameter	Symbol	Condition	Rated Value		Unit
			MIN.	MAX.	
Clock cycle	t_{CYK}	$T_A = -10$ to $+70$ °C	125	2000	ns
		$T_A = -40$ to $+85$ °C	140	2000	ns
Clock high-pulse width	t_{WKH}		50	1000	ns
Clock low-pulse width	t_{WKL}		50	1000	ns
Clock rise time	t_{KR}	1.5 V $\rightarrow$ 2.2 V		10	ns
Clock fall time	t_{KF}	2.2 V $\rightarrow$ 1.5 V		10	ns
Address setup time (vs. $\overline{RD}$ $\downarrow$)	t_{SAR}	$T_A = -10$ to $+70$ °C	0		ns
		$T_A = -40$ to $+85$ °C	5		
Address hold time (vs. $\overline{RD}$ $\uparrow$)	t_{HRA}	$T_A = -10$ to $+70$ °C	0		ns
		$T_A = -40$ to $+85$ °C	5		
$\overline{RD}$ pulse width	t_{WRL}	$T_A = -10$ to $+70$ °C	150		ns
		$T_A = -40$ to $+85$ °C	155		
Address $\rightarrow$ data output delay time	t_{DAD}	$T_A = -10$ to $+70$ °C		120	ns
		$T_A = -40$ to $+85$ °C		125	
$\overline{RD} \rightarrow$ data output delay time	t_{DRD}	$T_A = -10$ to $+70$ °C		120	ns
		$T_A = -40$ to $+85$ °C		125	
$\overline{RD} \rightarrow$ data float delay time	t_{FRD}		10	120	ns
Address setup time (vs. $\overline{WR}$ $\downarrow$)	t_{SAW}		0		ns
Address hold time (vs. $\overline{WR}$ $\uparrow$)	t_{HWA}	$T_A = -10$ to $+70$ °C	0		ns
		$T_A = -40$ to $+85$ °C	5		
$\overline{WR}$ pulse width	t_{WWL}	$T_A = -10$ to $+70$ °C	150		ns
		$T_A = -40$ to $+85$ °C	155		
Data setup time (vs. $\overline{WR}$ $\uparrow$)	t_{SDW}	$T_A = -10$ to $+70$ °C	120		ns
		$T_A = -40$ to $+85$ °C	125		
Data hold time (vs. $\overline{WR}$ $\uparrow$)	t_{HWD}	$T_A = -10$ to $+70$ °C	0		ns
		$T_A = -40$ to $+85$ °C	5		
Recovery time between $\overline{RD}$ and $\overline{WR}$	t_{RV}	$T_A = -10$ to $+70$ °C	180		ns
		$T_A = -40$ to $+85$ °C	190		

Serial control:

Parameter	Symbol	Condition		Rated Value		Unit
				MIN.	MAX.	
Transmit/receive data cycle	t _{cyD}			5		t _{cyK}
$\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$ input clock cycle	t _{cyC}	T _A = −10 to +70 °C		125	DC	ns
		T _A = −40 to +85 °C		140	DC	ns
$\overline{\text{STRxC}}$, $\overline{\text{TRxC}}$ input clock pulse width	t _{wCH}	High level	T _A = −10 to +70 °C	50	DC	ns
			T _A = −40 to +85 °C	55	DC	ns
	t _{wCL}	Low level	T _A = −10 to +70 °C	60	DC	ns
			T _A = −40 to +85 °C	65	DC	ns
$\overline{\text{STRxC}}$, $\overline{\text{TRxC}}\downarrow \rightarrow$ delay time	t _{DTCTD1}	×1 mode, COP, BOP	T _A = −10 to +70 °C		140	ns
			T _A = −40 to +85 °C		145	ns
	t _{DTCTD2}	×16, 32, 64 mode	T _A = −10 to +70 °C		300	ns
			T _A = −40 to +85 °C		305	ns
$\overline{\text{TRxC}}\downarrow \rightarrow$ TxD delay time	t _{DTCTD3}	$\overline{\text{TRxC}}$ is output		0	100	ns
RxD setup time (vs. $\overline{\text{STRxC}}$, $\overline{\text{TRxC}}\uparrow$)	t _{SRDRG}	When DPLL is not used	T _A = −10 to +70 °C	0		ns
			T _A = −40 to +85 °C	5		ns
RxD hold time (vs. $\overline{\text{STRxC}}$, $\overline{\text{TRxC}}\uparrow$)	t _{HRGRD}	When DPLL is not used	T _A = −10 to +70 °C	140		ns
			T _A = −40 to +85 °C	145		ns
RxD $\rightarrow$ TxD delay time	t _{DRD1}	ECHO BACK mode			100	ns
	t _{DRD2}	Without SDLC Loop delay			100	ns
TxD $\rightarrow$ $\overline{\text{INT}}$ delay time	t _{TDIQ}	Tx INT mode		4	6	t _{cyK}
TxD $\rightarrow$ DRQTx delay time	t _{TDQ}	Tx DMA mode		4	6	t _{cyK}
$\overline{\text{RxC}}\uparrow$ Note $\rightarrow$ $\overline{\text{INT}}$ delay time	t _{DRCIQ}	Rx INT mode		7	11	t _{cyK}
$\overline{\text{RxC}}\uparrow$ Note $\rightarrow$ DRQRx delay time	t _{DRCDQ}	Rx DMA mode		7	11	t _{cyK}
$\overline{\text{RD}}\downarrow \rightarrow$ DRQRx $\downarrow$ delay time	t _{DRDQ}				140	ns
$\overline{\text{WR}}\downarrow \rightarrow$ DRQTx $\downarrow$ delay time	t _{WDQ}				140	ns

Note Of $\overline{\text{STRxC}}$ and $\overline{\text{TRxC}}$, the one used as the receive clock.

Interrupt control:

Parameter	Symbol	Condition		Rated Value		Unit
				MIN.	MAX.	
$\overline{\text{INTAK}}$ low-pulse width	t_{WIAL}			150		ns
$\overline{\text{INTAK}}$ high-pulse width	t_{WIAH}			150		ns
$\overline{\text{PRI}} \rightarrow \overline{\text{PRO}}$ delay time	t_{DPIPO}				50	ns
$\overline{\text{INT}}\downarrow \rightarrow \overline{\text{PRO}}\uparrow$ delay time	t_{DIQPO}			−20	+50	ns
2nd $\overline{\text{INTAK}}\downarrow \rightarrow \overline{\text{INT}}\uparrow$ delay time	t_{DIAIQ}	$\overline{\text{INT}}$ output level = 0.8 V ^{Note}			120	ns
		$\overline{\text{INT}}$ output level = 1.8 V ^{Note}			300	ns
SR2B read $\overline{\text{RD}}\downarrow \rightarrow \overline{\text{INT}}\uparrow$ delay time	t_{DRDIQ}	$\overline{\text{INT}}$ output level = 0.8 V ^{Note}	$T_{\text{A}} = -10$ to $+70\text{ }^{\circ}\text{C}$		170	ns
			$T_{\text{A}} = -40$ to $+85\text{ }^{\circ}\text{C}$		180	ns
		$\overline{\text{INT}}$ output level = 1.8 V ^{Note}			350	ns
$\overline{\text{PRI}}$ setup time (vs. $\overline{\text{INTAK}}\downarrow$)	t_{SPIIA1}	When vector output is enabled		0		ns
$\overline{\text{PRI}}$ hold time (vs. $\overline{\text{INTAK}}\uparrow$)	t_{HIAP11}			20		ns
$\overline{\text{PRI}}$ setup time (vs. $\overline{\text{INTAK}}\downarrow$)	t_{SPIIA2}	When vector output is disabled		20		ns
$\overline{\text{PRI}}$ hold time (vs. $\overline{\text{INTAK}}\uparrow$)	t_{HIAP12}		$T_{\text{A}} = -10$ to $+70\text{ }^{\circ}\text{C}$	20		ns
			$T_{\text{A}} = -40$ to $+85\text{ }^{\circ}\text{C}$	25		ns
$\overline{\text{INTAK}} \rightarrow$ data output delay time	t_{DIAD}				120	ns
$\overline{\text{INTAK}} \rightarrow$ data float delay time	t_{FIAD}			10	130	ns

Note Measured value with 2-k Ω pull-up resistor and 100-pF load capacitance connected

Modem control:

Parameter		Symbol	Condition	Rated Value		Unit
				MIN.	MAX.	
$\overline{\text{CTS}}, \overline{\text{DCD}}, \overline{\text{SYNC}}$ pulse width	High	t_{WMH}		2		t _{cyk}
	Low	t_{WML}		2		t _{cyk}
$\overline{\text{CTS}}, \overline{\text{DCD}}, \overline{\text{SYNC}} \rightarrow \overline{\text{INT}}$ delay time		t_{DMIQ}			2	t _{cyk}
$\overline{\text{STRxC}}, \overline{\text{TRxC}} \uparrow \rightarrow \overline{\text{SYNC}}$ setup time		t_{SSYRC}	COP external synchronization	0	2	t _{cyk}

Communication control:

Parameter	Symbol	Condition	Rated Value		Unit
			MIN.	MAX.	
Transmit enable command ($\overline{WR} \uparrow$, $\overline{CTS} \downarrow$) $\rightarrow$ TxD delay time	tDTETD1	ASYNC, COP		3	t _{cyc}
	tDTETD2	BOP	4	7	t _{cyc}
Receive enable command ($\overline{DCD} \downarrow$) setup time (vs. start bit, $\overline{STRxC} \uparrow$, $\overline{TRxC} \uparrow$ of sync character) ^{Note}	tSRERC		1		t _{cyc}
Receive enable command ($\overline{DCD} \downarrow$) hold time (vs. $\overline{STRxC} \uparrow$, $\overline{TRxC} \uparrow$) ^{Note}	tHRCRE1	ASYNC	7		t _{cyc}
	tHRCRE2	COP	20 t _{cyc} + 8t _{cyc}		
	tHRCRE3	BOP	3t _{cyc} + 8t _{cyc}		
Receive clock ($\overline{STRxC}$, $\overline{TRxC}$) ^{Note} hold time (vs. start bit, MSB of CRC, MSB of end flag)	tHRDRC1	ASYNC	1		Bit
	tHRDRC2	COP	22		t _{cyc}
	tHRDRC3	BOP	5		t _{cyc}
Receive clock ($\overline{STRxC}$, $\overline{TRxC}$) ^{Note} setup time (vs. start bit, sync character)	tSRCRD1	ASYNC	1		Bit
	tSRCRD2	COP, BOP	1		t _{cyc}

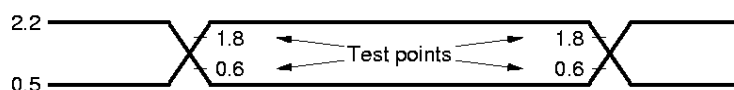
Note Of $\overline{STRxC}$ and $\overline{TRxC}$, the one used as the receive clock.

Crystal oscillation and reset:

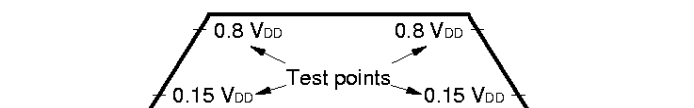
Parameter	Symbol	Condition	Rated Value		Unit
			MIN.	MAX.	
XI1 input cycle time	t _{cyc}	T _A = -10 to +70 °C	125	1000	ns
		T _A = -40 to +85 °C	140	1000	
$\overline{RESET}$ pulse width	t _{WRSL}		2		t _{cyc}

Caution The system clock cycle in all modes must be five times that of the data rate.

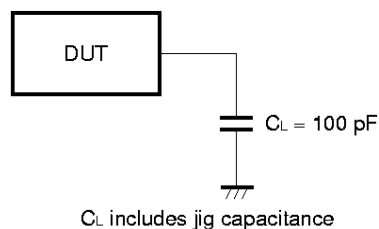
AC Test Input Waveform (except clock)



AC Test Clock Input Waveform



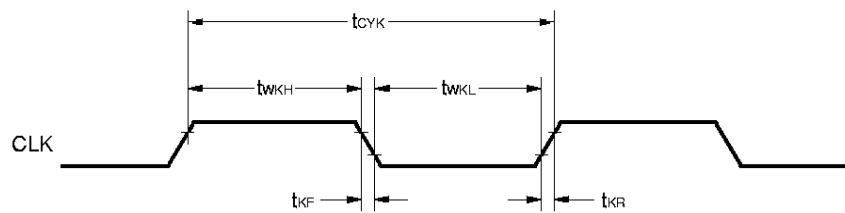
Load Condition



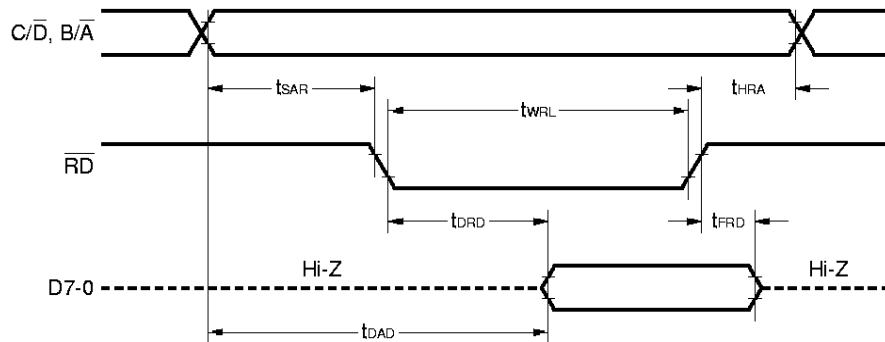
Caution If the load capacitance exceeds 100 pF due to the configuration of the circuit, keep the load capacitance of this device to within 100 pF by inserting a buffer or by any other means.

Remark DUT: Tested device

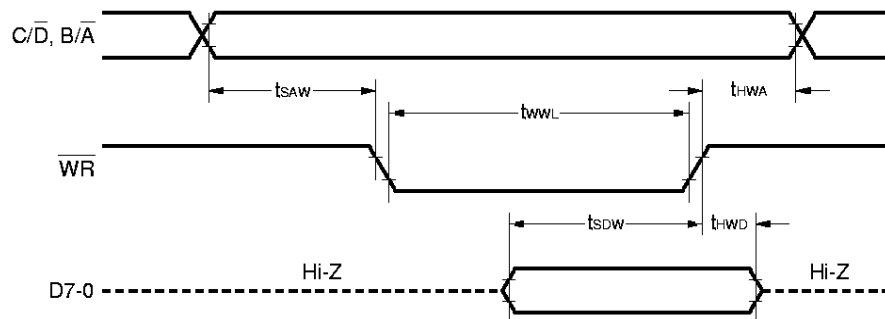
Clock Timing



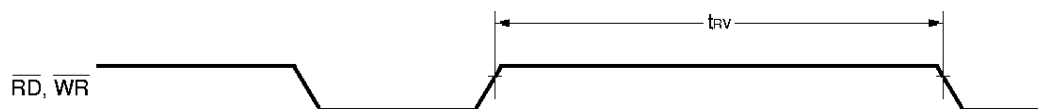
Read Cycle Timing



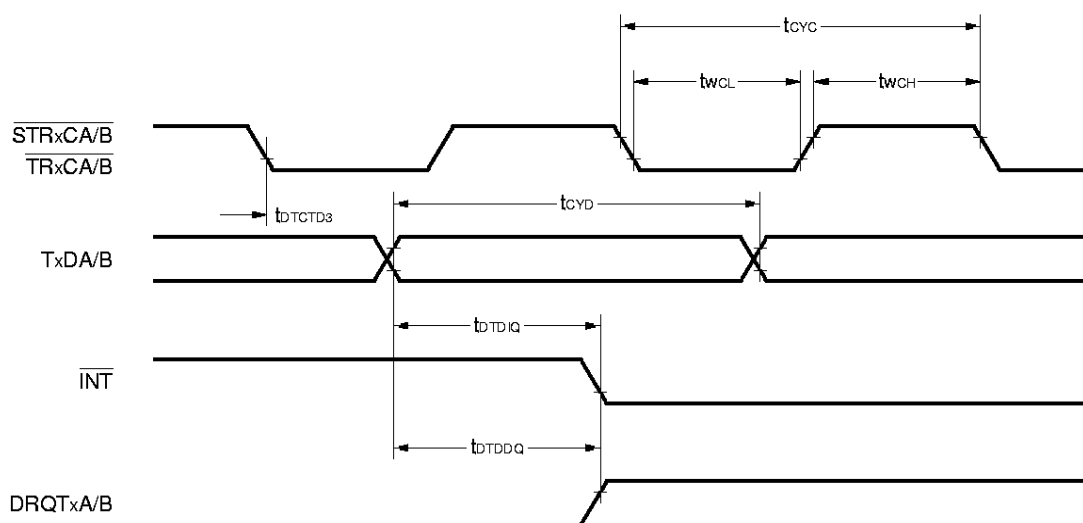
Write Cycle Timing



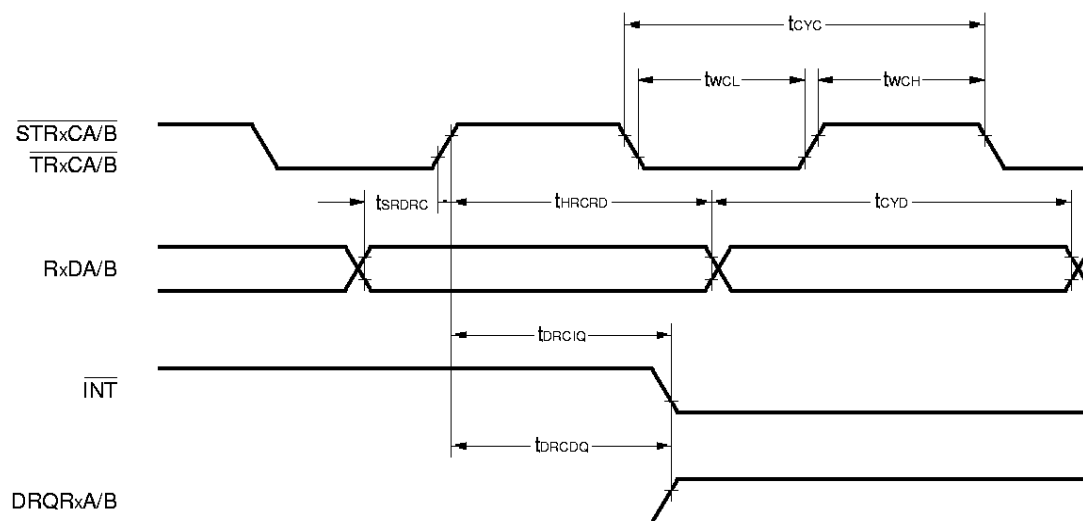
Read/Write Cycle Timing (except transfer of transmit/receive data)



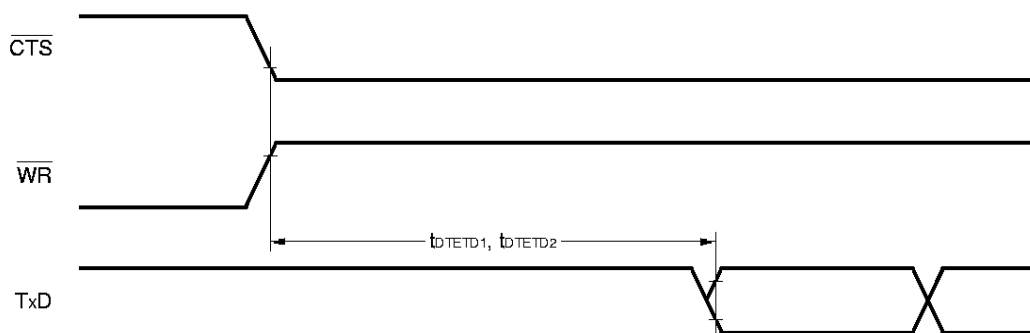
Transmit Cycle Timing



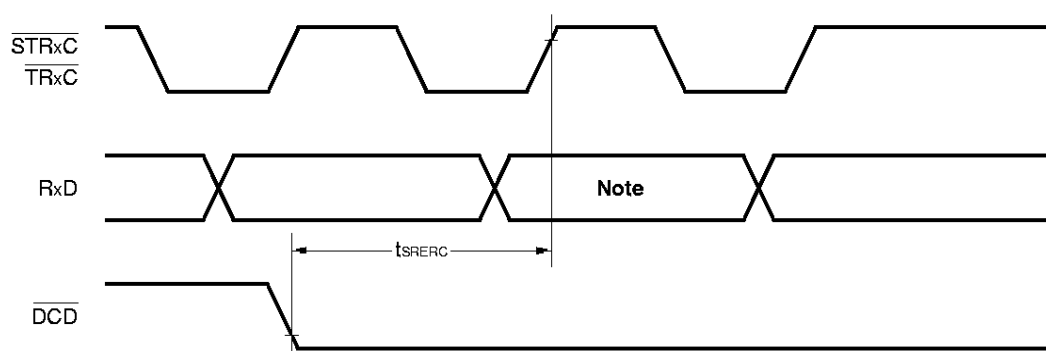
Receive Cycle Timing



Transmitter Enable Timing



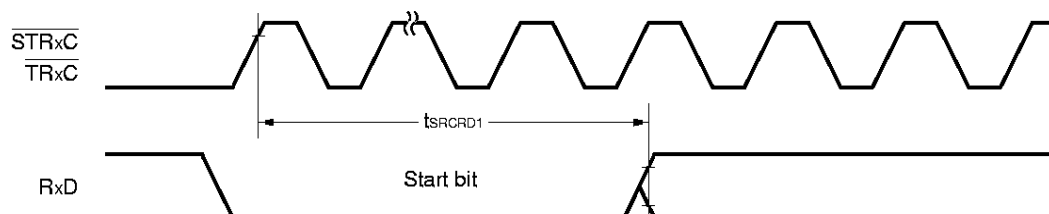
Receiver Enable Timing



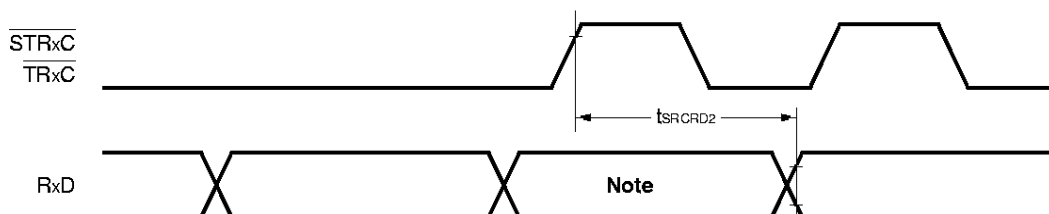
Note LSB of the first receive data (SYNC, flag)

Receive Clock Setting Timing

a. In ASYNC mode



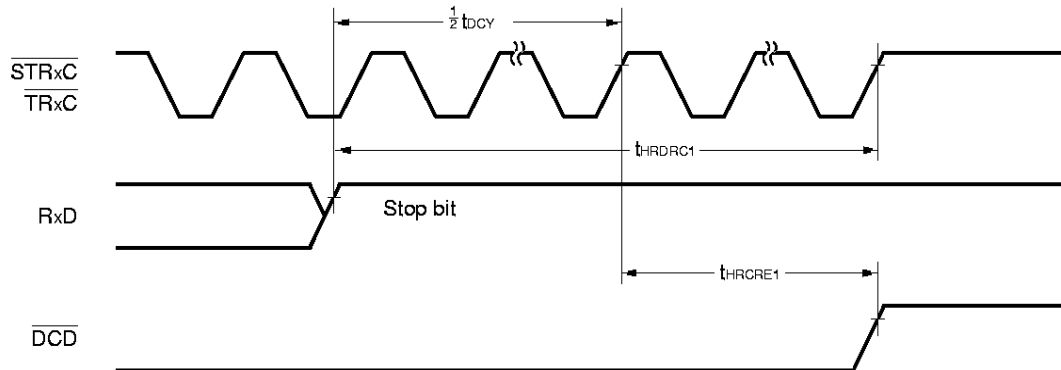
b. In COP/BOP mode



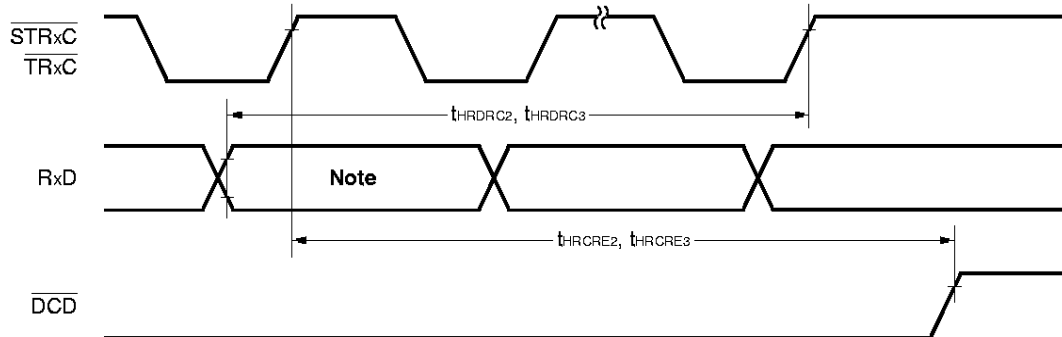
Note LSB of sync pattern (SYNC, flag)

DCD Timing, Receive Clock Hold Timing

a. In ASYNC mode

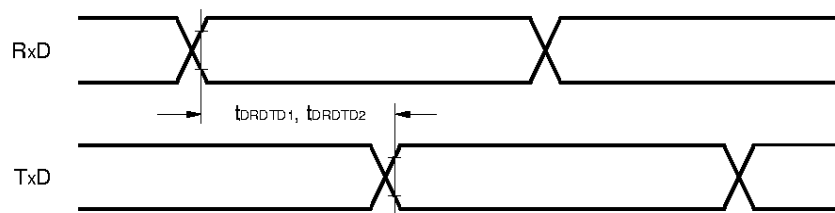


b. COP/BOP mode

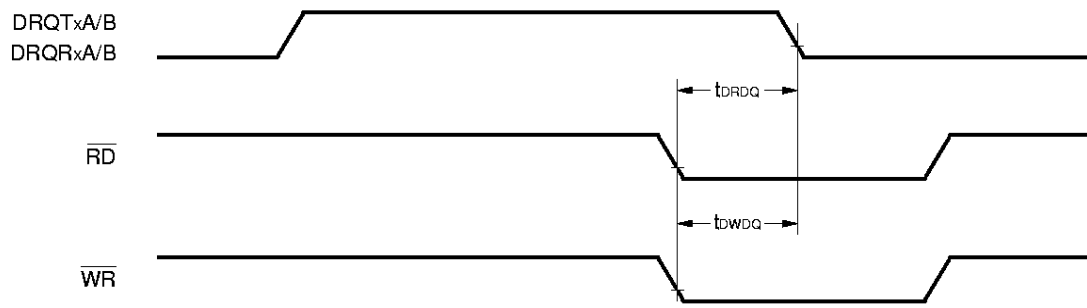


Note This bit is the MSB of BCS in the COP mode and MSB of the end flag in the BOP mode.

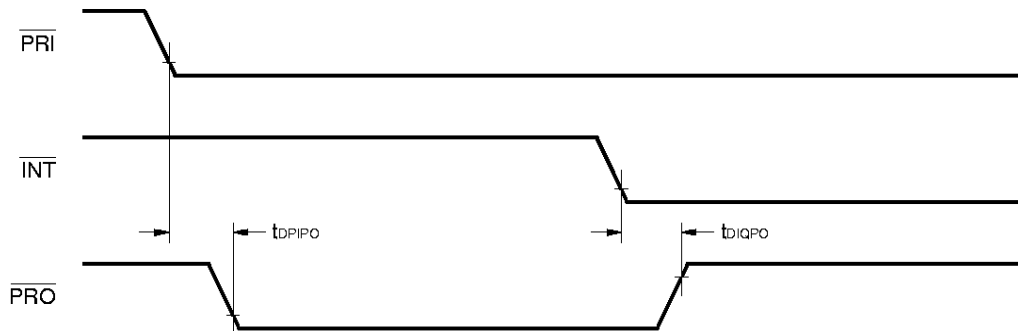
In ECHO BACK Mode and LOOP Mode



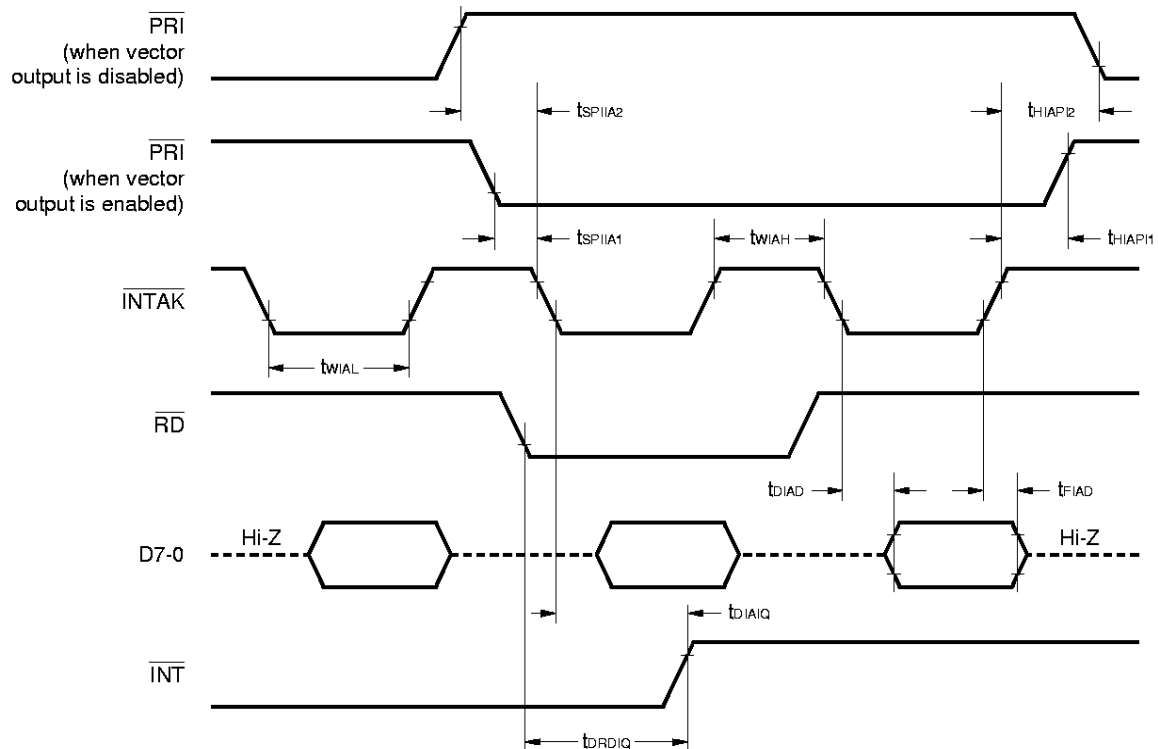
DMA Cycle Timing



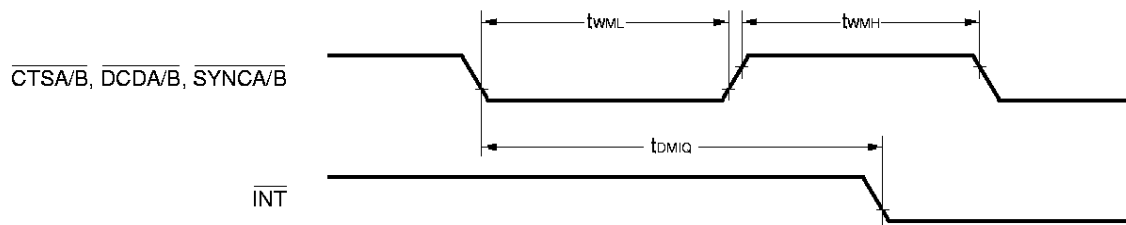
$\overline{\text{PRO}}$ Output Timing



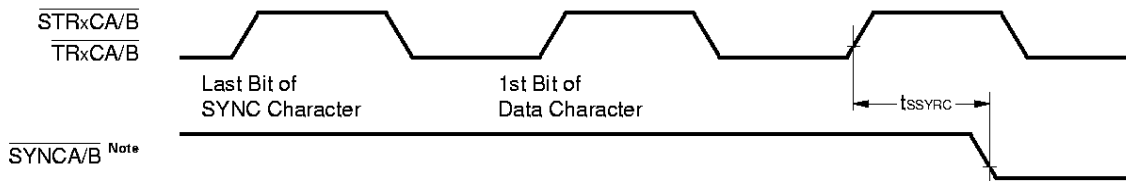
$\overline{\text{INTAK}}$ Cycle Timing



E/S Timing

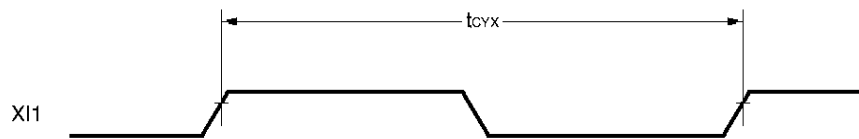


SYNC Input Timing (external synchronization mode)

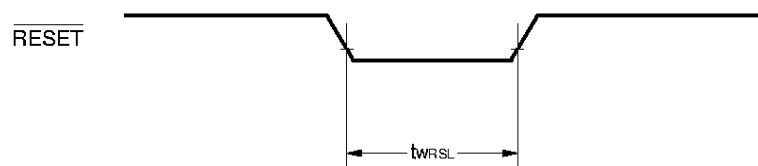


Note $\overline{\text{SYNCA/B}}$ input must be cleared to "0" at the rising edge of $\overline{\text{RxC}}$ two clock cycles after the last bit of the SYNC character.

XI1 Input Timing

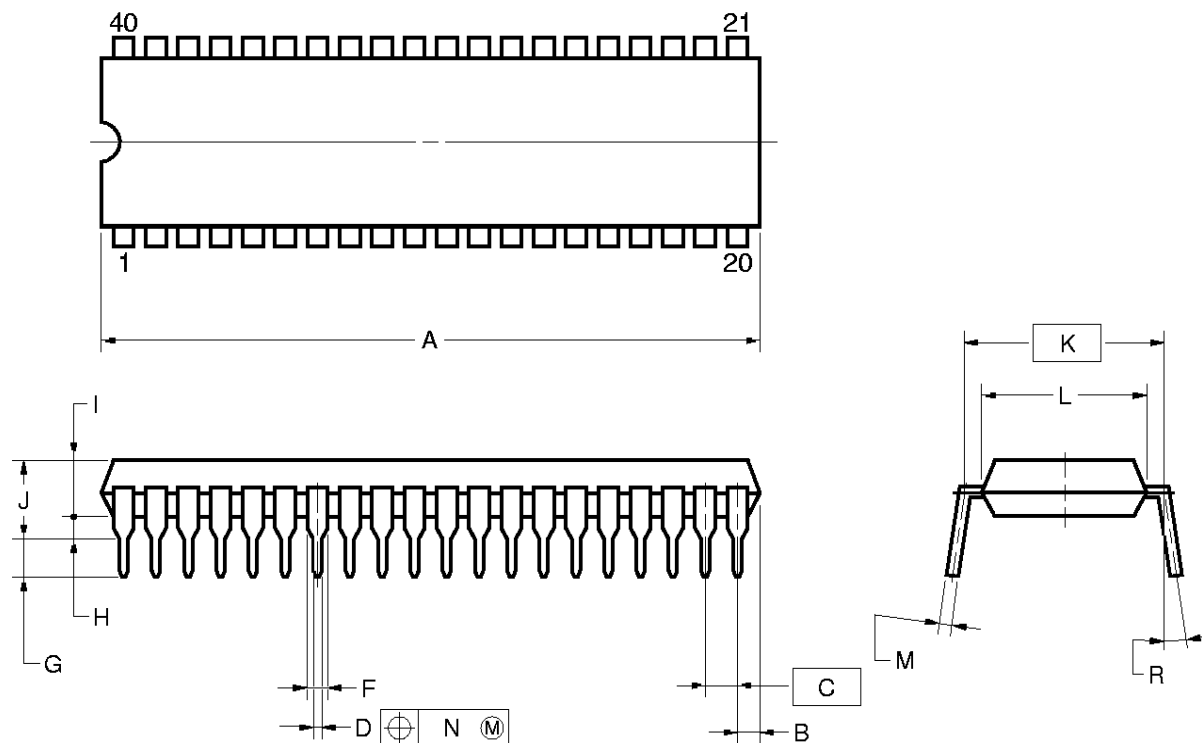


RESET Pulse



4. PACKAGE

40PIN PLASTIC DIP (600 mil)



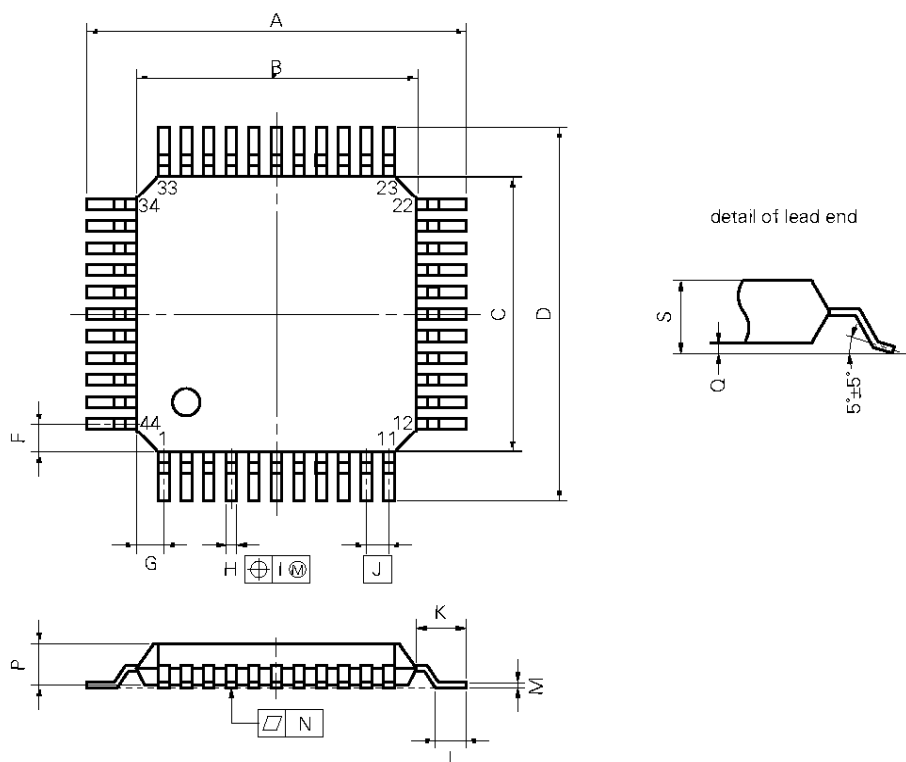
NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	1.2 MIN.	0.047 MIN.
G	3.6±0.3	0.142±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.25	0.01
R	0~15°	0~15°

P40C-100-600A-1

44 PIN PLASTIC QFP (□10)



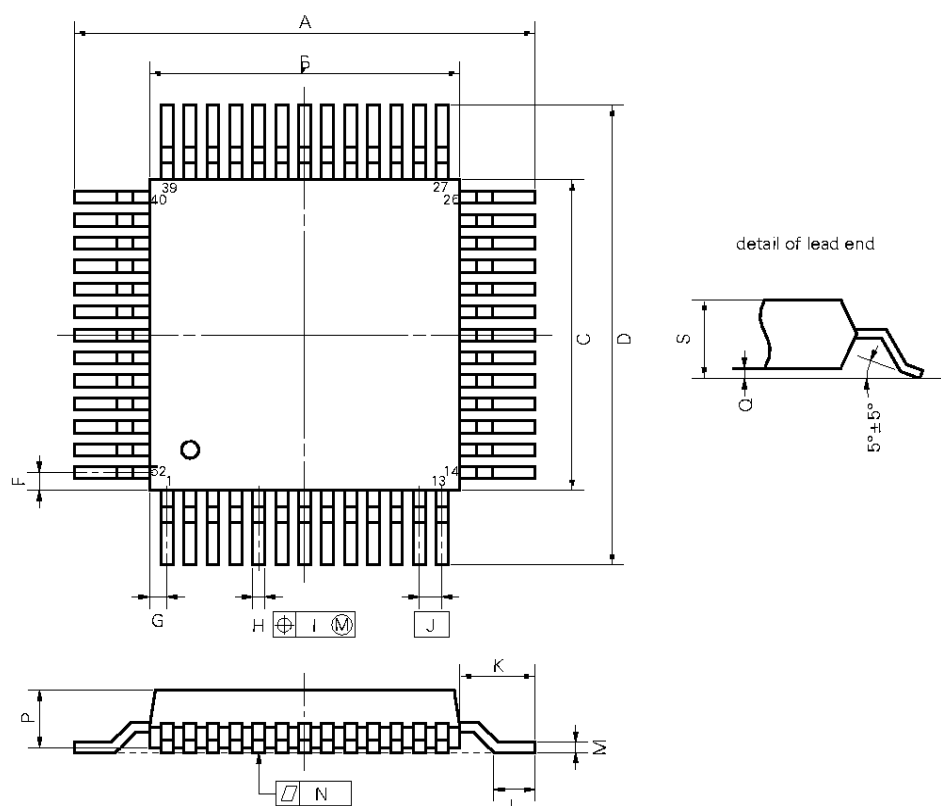
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P44G-80-22-2

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	0.535 ^{+0.017} _{-0.016}
B	10.0±0.2	0.394 ^{+0.008} _{-0.009}
C	10.0±0.2	0.394 ^{+0.008} _{-0.009}
D	13.6±0.4	0.535 ^{+0.017} _{-0.016}
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	1.0±0.2	0.039 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.15	0.006
P	1.45±0.1	0.057 ^{+0.005} _{-0.004}
Q	0.05±0.05	0.002±0.002
S	1.65 MAX.	0.065 MAX.

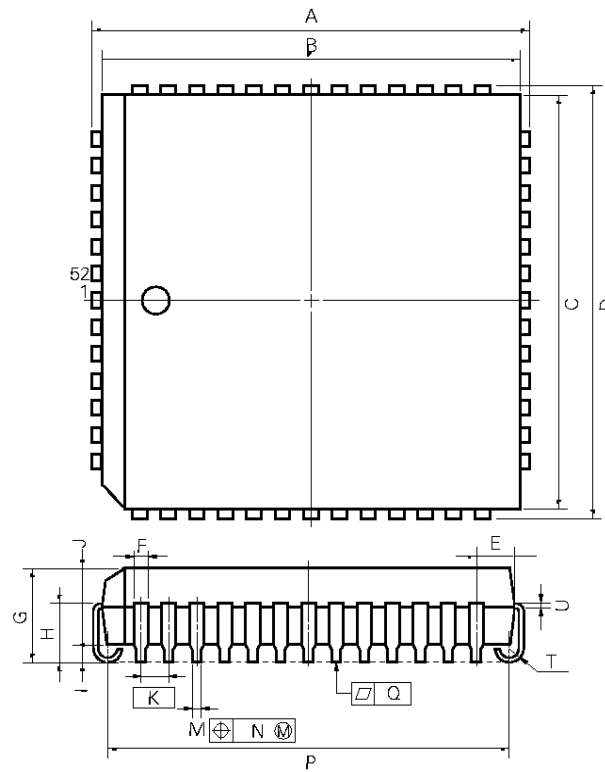
52 PIN PLASTIC QFP (□14)

**NOTE**

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

P52GC-100-3P6,3BH-2

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	0.016 ^{+0.004} _{-0.005}
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

52 PIN PLASTIC QFJ ($\square$ 750 mil)**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P52L-50A1-2

ITEM	MILLIMETERS	INCHES
A	20.1 $\pm$ 0.2	0.791 $^{+0.009}_{-0.008}$
B	19.12	0.753
C	19.12	0.753
D	20.1 $\pm$ 0.2	0.791 $^{+0.009}_{-0.008}$
E	1.94 $\pm$ 0.15	0.076 $^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4 $\pm$ 0.2	0.173 $^{+0.009}_{-0.008}$
H	2.8 $\pm$ 0.2	0.110 $^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40 $\pm$ 0.10	0.016 $^{+0.004}_{-0.005}$
N	0.12	0.005
P	18.04 $\pm$ 0.20	0.710 $^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	0.20 $^{+0.10}_{-0.05}$	0.008 $^{+0.004}_{-0.002}$

5. RECOMMENDED SOLDERING CONDITIONS

It is recommended to solder this product under the following conditions.

For details on the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Surface mount type

- μPD72001G-11-22 : 44-pin plastic QFP (10 × 10 mm)
- μPD72001G-A8-22 : 44-pin plastic QFP (10 × 10 mm)

Soldering Method	Soldering Condition	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX. (210 °C MIN.), Number of times: 2 MAX., Number of days: 7 ^{Note} (After that, prebaking for 10 hours at 125 °C is necessary.) <Precaution> Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	IR35-107-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX. (200 °C MIN.), Number of times: 2 MAX., Number of days: 7 ^{Note} (After that, prebaking for 10 hours at 125 °C is necessary.) <Precaution> Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	VP15-107-2
Wave soldering	Solder bath temperature: 260 °C MAX., Time: 10 seconds MAX., Number of times: 1, Preheating temperature: 120 °C MAX. (package surface temperature), Number of days: 7 ^{Note} (After that, prebaking for 10 hours at 125 °C is necessary.) <Precaution> Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	WS60-107-1
Partial heating	Pin temperature: 300 °C MAX., Time: 3 seconds MAX. (per side of device)	—

Note The number of days the product can be stored at 25 °C, 65 % RH MAX. after the dry pack has been opened.

Caution Do not use two or more soldering methods in combination (except partial heating).

- μ PD72001GC-11-3B6 : 52-pin plastic QFP (14 × 14 mm)
 μ PD72001GC-A8-3B6 : 52-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Condition	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX. (210 °C MIN.), Number of times: 3 MAX.	IR35-00-3
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX. (200 °C MIN.), Number of times: 3 MAX.	VP15-00-3
Wave soldering	Solder bath temperature: 260 °C MAX., Time: 10 seconds MAX., Number of times: 1 Preheating temperature: 120 °C MAX. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C MAX., Time: 3 seconds MAX. (per side of device)	—

Caution Do not use two or more soldering methods in combination (except partial heating).

- μ PD72001L-11: 52-pin plastic QFJ (750 × 750 mil)

Soldering Method	Soldering Condition	Recommended Condition Symbol
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX. (200 °C MIN.), Number of times: 1	VP15-00-1
Partial heating	Pin temperature: 300 °C MAX., Time: 3 seconds MAX. (per side of device)	—

Through-hole type

- μ PD72001C-11 : 40-pin plastic DIP (600 mil)
 μ PD72001C-A8 : 40-pin plastic DIP (600 mil)

Soldering Method	Soldering Condition
Wave soldering (pins only)	Solder bath temperature: 260 °C MAX., Time: 10 seconds MAX.
Partial heating	Pin temperature: 300 °C MAX., Time: 3 seconds MAX. (per pin)

Caution When soldering this product using of wave soldering, exercise care that the solder does not come in direct contact with the package.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.