MOS INTEGRATED CIRCUIT

μPD9325C

CLOCK GENERATOR LSI (CKG) FOR IMPROVED DEFINITION TV

DESCRIPTION

The μPD9325C is the clock generator (CKG) LSI for the improved definition TV (IDTV). This LSI generates the clock supplied to the system LSIs and controls the timing of the system operation. In combination with five LSIs (YCS, YCP, YCI, MDP, and CDU), this LSI can be used to configure an IDTV signal processing system.

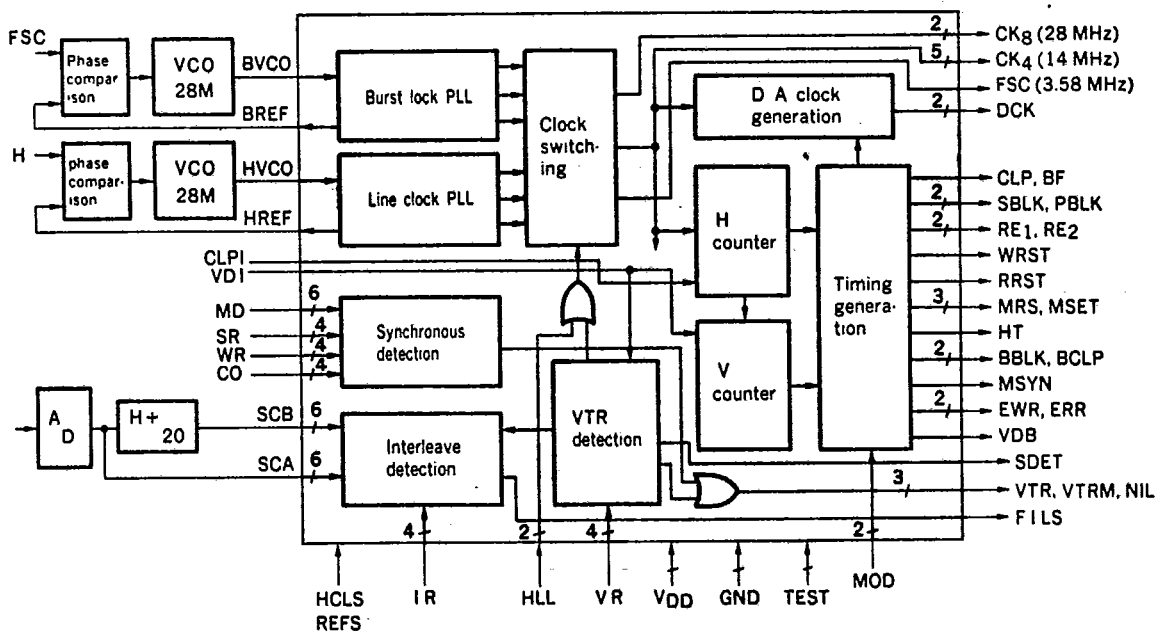
FEATURES

- Two built-in clock circuits:
  - Burst synchronization clock
  - Line synchronization clock
- Various built-in timing generator circuits.
- Built-in nonstandard signal detection circuit.
- +5 volts single power supply.
- Low power consumption due to CMOS circuitry.

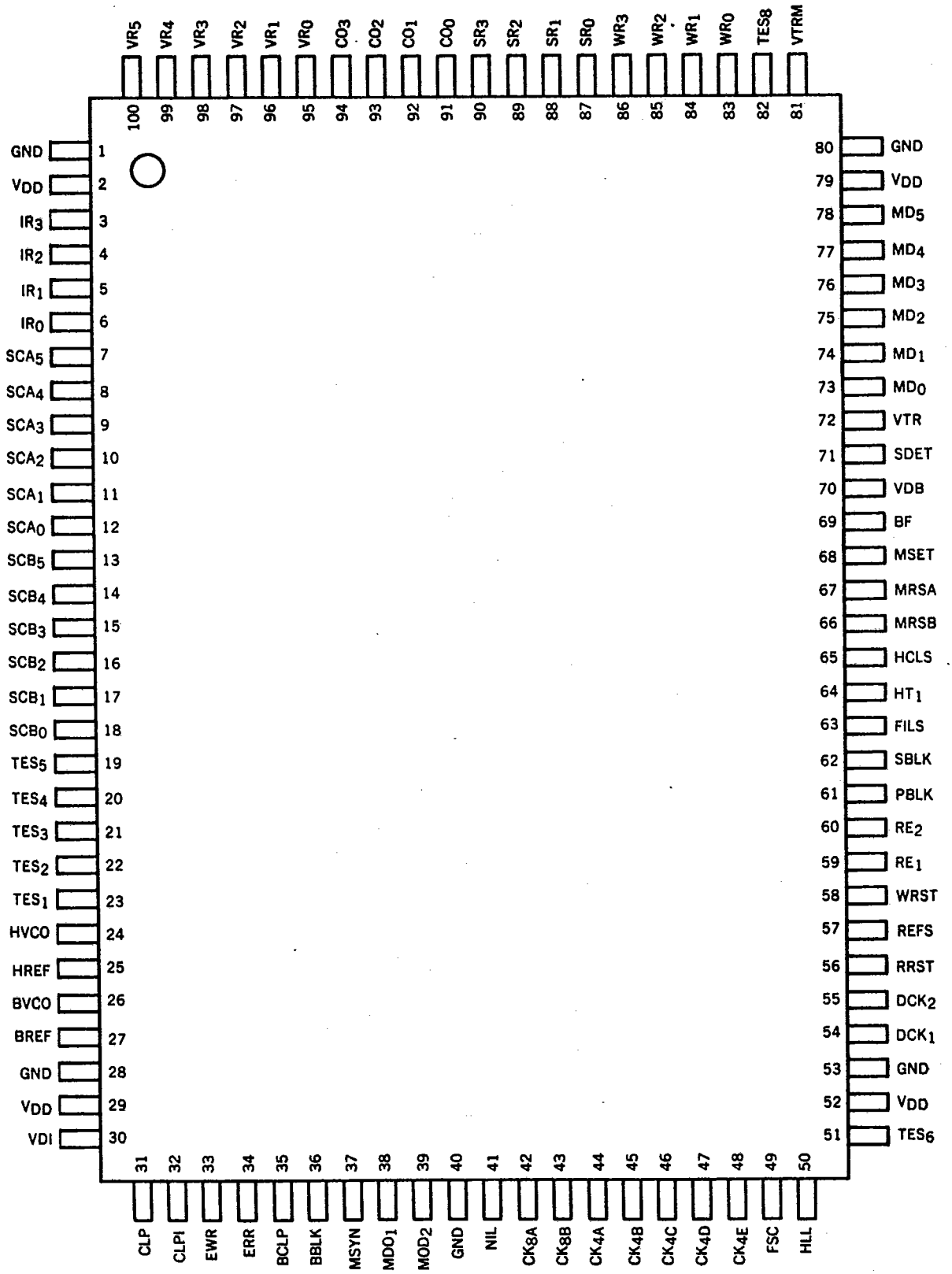
ORDERING INFORMATION

Part Number	Package
μPD9325CGF-3BA	100 PIN PLSTIC QFP (14 x 20)

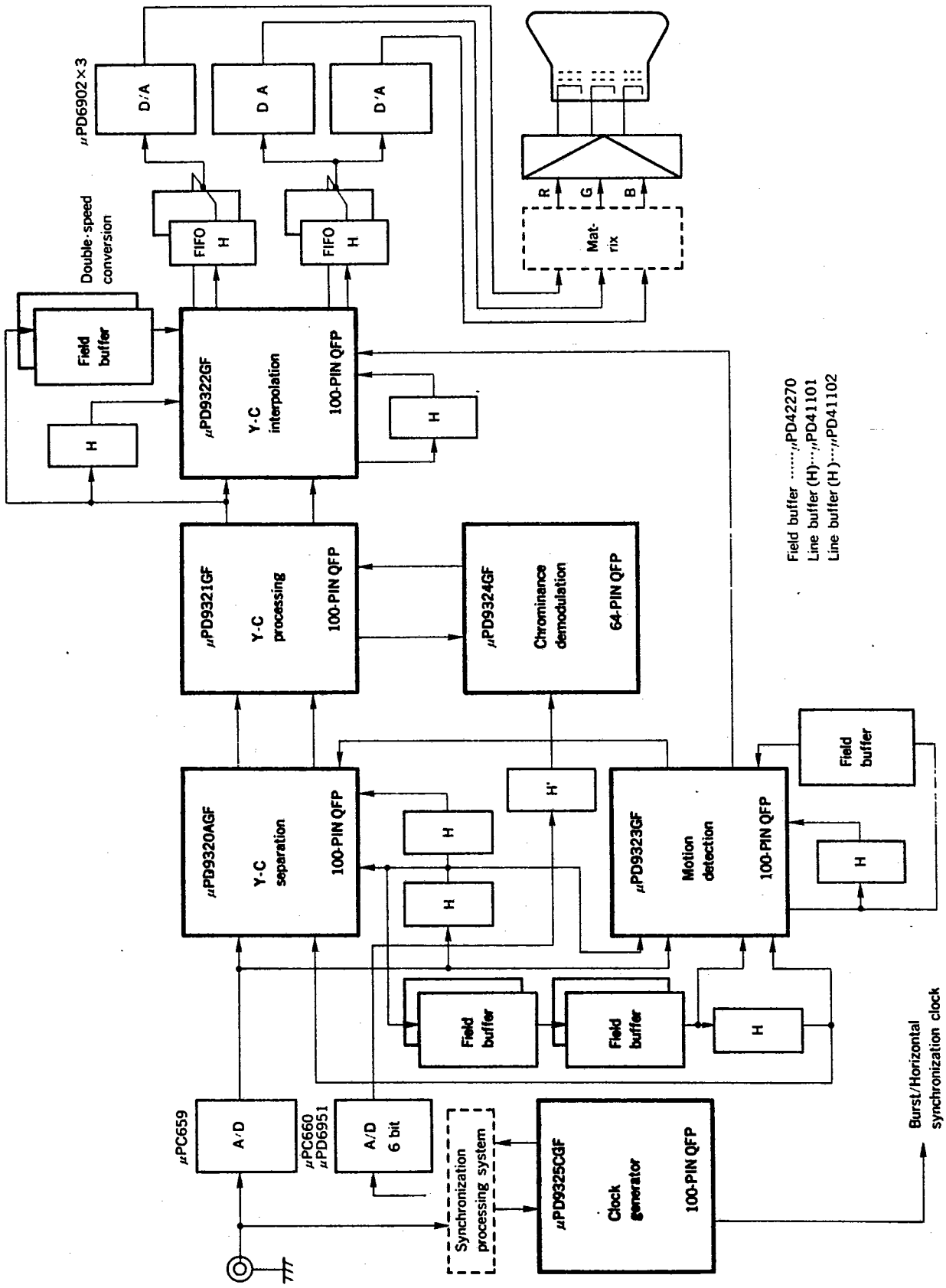
BLOCK DIAGRAM



TERMINAL CONNECTION DIAGRAM (Top View)



LSI SYSTEM CONFIGURATION FOR THE IDTV



ELECTRICAL RATINGS OF THE μPPD9325B

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Source Voltage	V_{DD}	−0.5 to 7.0	V
Input Voltage	V_{IN}	−0.5 to V_{DD} + 0.5	V
Output Current	I_{OUT}	20	mA
Package Allowable Dissipation	P_D	400	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITION (T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	V_{DD}	4.5	5.0	5.5	V	
Low-level Input Voltage	V_{IL}	0		0.3 V_{DD}	V	Input terminals: Y, C, MI, and CLK (CMOS input)
High-level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Low-level Input Voltage	V_{IL}	0		0.8	V	Input terminals: YH, YF, and CH (TTL input)
High-level Input Voltage	V_{IH}	2.4		V_{DD}	V	
Clock Frequency	F_{CLK}		28.6		MHz	Input terminals: BVCO and HVCO

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ±10 %, T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Source Current	I_{DD}		30		mA	
Low-level Output Current	I_{OL}	4	11		mA	V_{OL} = 0.4 V
High-level Output Current	$-I_{OH}$	4	8		mA	$V_{OH} = V_{DD} - 0.4$ V
Input Current	$\pm I_I$			10	μA	$V_I = V_{DD}$ or GND
Output Delay Time	T_d		6		ns	$CK_8 \rightarrow CK_4$
Output Delay Time	T_d		16		ns	$CK_4 \rightarrow$ Output
Input Terminal Capacitance	C_{IN}			10	pF	$V_{DD} = V_I = 0$ f = 1 MHz
Output Terminal Capacitance	C_{OUT}			15	pF	

TERMINAL DESCRIPTION: CKG

TERMINAL SYMBOL	TERMINAL NAME	TERMINAL NUMBER	FUNCTION	
BVCO	Burst VCO oscillation input	26	Input (CMOS)	Inputs the VCO oscillation clock for the burst lock PPL. The input is 8 f_{SC} (28.6 MHz).
BREF	Burst PLL reference output	27	Output (CMOS)	Output the reference signal to the burst lock PLL. The output is a signal of f_{SC}(3.58 MHz).
HVCO	H-VCO oscillation input	24	Input (CMOS)	Inputs the VCO oscillation clock for the line lock PLL. The input is a signal of 1 820 f_H (28.6 MHz).
HREF	H-PLL reference output	25	Output (CMOS)	Outputs the reference signal to the line lock PLL. The output is a signal of f_H (15.73 kHz).
CK_{8A} CK_{8B}	28 MHz clock	42 43	Output (CMOS)	This clock, with 8 f_{SC} (28.6 MHz), is used for the double-speed conversion.
CK_{4A} CK_{4B} CK_{4C} CK_{4D} CK_{4E}	14 MHz clock	44 45 46 47 48	Output (CMOS)	System clock (4 f_{SC} (14.3 MHz))
FSC	Subcarrier output	49	Output (CMOS)	The output is supplied to the YCP and CDU terminals of the FSC. This output is the reference phase output (f_{SC} (3.58 MHz)).
DCK_1 DCK_2	D/A clock	54 55	Output (CMOS)	Clock for the R–Y/B–Y D/A (4 f_{SC} (14.3 MHz)) (DCK_1: R–Y, DCK_2: B–Y)
CLP	Clamper output	31	Output (CMOS)	This output is used for the input video signal clamper. Active "L"
SBLK	YCS blank output	62	Output (CMOS)	This output is supplied to the BLK terminal of the YCS. Active "H"
PBLK	YCP blank output	61	Output (CMOS)	This output is supplied to the BLK terminal of the YCP. Active "H"
BF	Burst flag output	69	Output (CMOS)	This output is supplied to the BF terminal of the YCP. Active "H"
RE_1 RE_2	Read enabling output	59 60	Output (CMOS)	Controls the reading (read enabling) from the double-speed conversion FIFO memory. The phases of RE_1 and RE_2 are opposite.
WRST	Write reset output	58	Output (CMOS)	Resets the place (write pointer) of the double-speed conversion FIFO memory.
RRST	Read reset output	56	Output (CMOS)	Resets the read pointer of the double-speed conversion FIFO memory.
MRSA MRSB	Line memory reset output	67 66	Output (CMOS)	Used for resetting the pointer of the delayed line memory (delayed by 910 bits).
MSET	Line memory setting output	68	Output (CMOS)	This output sets the line memory for delaying the sub-carrier data at 930 bits.
HT	Horizontal timing	64	Output (CMOS)	Horizontal timing output.
BBLK	Double-speed RGB matrix blank output	36	Output (CMOS)	Blank output for the RGB matrix converted in double-speed. Active "H"
BCLP	Double-speed RGB matrix clamper output	35	Output (CMOS)	This output is used for clamping the RGB matrix converted in double-speed. Active "H"
MSYN	Double-speed synchronizing mixed signal	37	Output (CMOS)	Mixed synchronous signal (2H + V) converted in double-speed. Active "L"
EWR	External RGB write reset output	33	Output (CMOS)	Resets the write pointer of the FIFO memory for the external RGB double-speed conversion.
ERR	External RGB read reset output	34	Output (CMOS)	Resets the read pointer of the FIFO memory for the external RGB double-speed conversion.

CKG

TERMINAL SYMBOL	TERMINAL NAME	TERMINAL NUMBER	FUNCTION	
VDB	Vertical synchronization output	70	Output (CMOS)	Outputs the vertical synchronization signal. This output is supplied to the VD terminal of the YCP. Active "L"
VDI	Vertical synchronization input	30	Input (CMOS)	Inputs the vertical synchronization pulse obtained from the video signal through synchronous separation.
MOD_1 MOD_2	Output timing mode	38 39	Input (CMOS)	Used to switch the amount of delay in timing of the signal output beyond the YCP. In normal operation, connect the MOD_1 to the GND terminal and MOD_2 to the V_{DD} terminal.
$SCA_0 - SCA_5$	Subcarrier data input A	12 to 7	Input (TTL)	Inputs the six-bit output from the subcarrier A/D. Used as the input for interleave detection. (SCA_0: LSB, SCA_5: MSB)
$SCB_0 - SCB_5$	Subcarrier data input B	18 to 13	Input (TTL)	Inputs the subcarrier A/D data delayed by 930 bits. Used as the input for interleave detection. (SCB_0: LSB, SCB_5: MSB)
$MD_0 - MD_5$	Motion data input	73 to 78	Input (CMOS)	Inputs the luminance motion signal output from the MDP. (MD_0: LSB, MD_5: MSB)
$VR_0 - VR_5$	VTR detection reference data	95 to 100	Input (CMOS)	This input is used to set the detection level of nonstandard signal. Used as the VTR detection reference level. In normal operation, this is "H." Reference = 20 H
$IR_0 - IR_3$	Interleave detection refference data	6 to 3	Input (CMOS)	This input is used to set the detection level of nonstandard signal. Used as the interleave detection reference level. In normal operation, this is "H." Reference = 10 H
$SR_0 - SR_3$	Synchronous detection reference data	87 to 90	Input (CMOS)	This input is used to set the nonstandard signal detection level. Used at the synchronous detection reference level. In normal operation, this is "H." Reference = 8 H
$WR_0 - WR_3$	Weak field detection reference data	83 to 86	Input (CMOS)	This input is used to set the nonstandard signal detection level. Used as the weak field detection reference level. In normal operation, this is "H." Reference = 3 H
$CO_0 - CO_3$	Coring level input	91 to 94	Input (CMOS)	This input is used for coring the synchronous/weak field detection. Reference = 5 H
HLL	Forced line lock	50	Input (CMOS)	When this terminal is set to "H," the system forcefully switches to the line lock mode. (0; standard, 1; Line lock)
VTR	Forced motion output	72	Output (CMOS)	The signal is output to the VTR terminal of the MDP.
NIL	Non-interlace flag	41	Output (CMOS)	Detects discrepancies between the burst lock oscillation frequency and the line lock oscillation frequency. When the discrepancy is over a certain magnitude, this terminal becomes "H."
FILS	Filter selection output	63	Output (CMOS)	This output is supplied to the FILS terminal of the YCP. When an interline subcarrier divergence is detected in the interleave detection process, this terminal becomes "H."
$TES_1 - TES_6$	Test input	23 to 19 51	Input (Pull-up R)	Test input terminal. Connect this terminal to V_{DD}.
$TES_7 - TES_8$	Test output	81 82	Output	Test output terminal.
V_{DD}	Power terminal	2 29 52 79		Power input terminal. Apply +5 volts to this terminal.
GND	Grounding terminal	1 28 40 53 80		This is a grounding terminal.

TERMINAL SYMBOL	TERMINAL NAME	TERMINAL NUMBER	FUNCTION	
CLPI	Clamp Pulse Input	32	Input (CMOS)	This pin is selecting pin of clamp pulse and burst flag output. At "L" inputting to this terminal, the outputs of CLP and BF terminals are generated from internal counter. At "Clamping pulse (Active Low)" inputting to this terminal, the outputs of CLP and BF terminals are generated from inputted clamping pulse.
VTRM	Forced Motion Edge Output	81	Output (CMOS)	Output terminal of VTR detected signal. This terminal outputs "H" signal during 3 field, before VTR output changes from "H" to "L".
SDET	Sync Detect Output	71	Output (CMOS)	Output terminal of Sync Detect. Connect with VTR terminal of MDP LSI. This terminal outputs "H" signal when Sync detect circuit detects non-standard signal closely to NTSC signal.
HCLS	H Clear Select	65	Input (Pull-down R)	This terminal is selecting terminal of H·V counter's reset timing. In normal operation, connect to GND.
REFS	HREF Select	57	Input (Pull-down R)	This terminal is selecting terminal of reference position for HREF output. In normal operation, connect to GND.

DESCRIPTION OF FUNCTIONS

The μPD9325C supplies clocks and timing to the IDTV system component LSIs (i.e., the μPD9320A to 9324) and generates various timing signals for the peripheral equipments.

In addition, this LSI selects the optimum clock accordingly to the state of the input signal utilizing the built-in nonstandard signal detection circuit and outputs the signal to switch the signal processing modes.

1. CLOCK GENERATION

The μPD9325C has a built-in frequency divider to generate two kinds of clocks: a clock synchronized to the burst signal and other synchronized to the line signal.

These two clocks are generated constantly. The detection output from the built-in nonstandard signal detection circuit switches these clocks to supply the system clock to the various LSIs.

Burst Lock PLL

The burst lock PLL circuit processes the color subcarrier (3.58 MHz (F_{sc})) that has been gain-locked to the burst signal by the analog synchronization process circuit to generate the phased-locked clock at 28.6 MHz (8 F_{sc}).

The CKG has a built-in octal frequency divider to generate the 3.58 MHz reference clock divided from the 28.6 MHz clock input from the BVCO (output from the BREF output terminal).

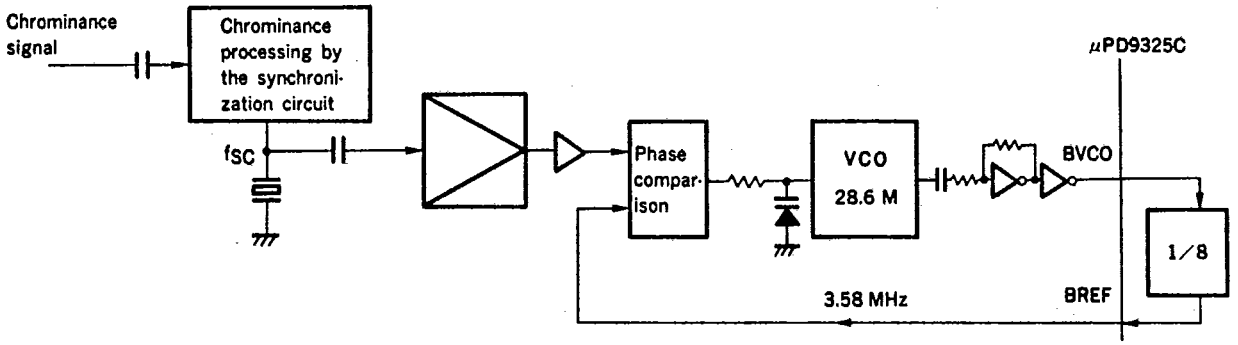
The phase of this clock is compared with that of the color subcarrier clock (3.58 MHz) supplied by the analog synchronization circuit. The output of the comparison result is used to control the VCO at 28.6 MHz. The PLL circuit incorporates this output input to the BVCO terminal of the CKG.

Line Lock PLL

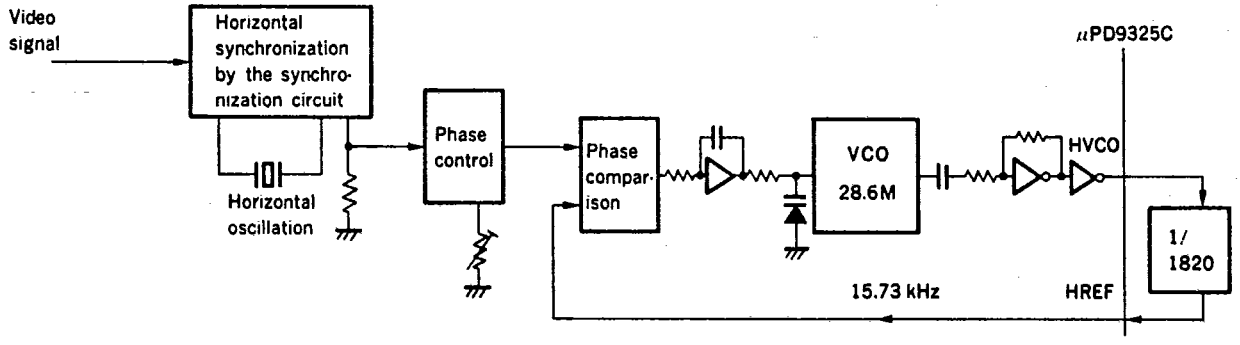
The line lock PLL circuit generates the phase-locked clock (28.6 MHz (1 820 f_H)) which has a frequency 1820 times that of the horizontal oscillation output (15.73 kHz (f_H)) that is generated synchronized with the horizontal synchronization signal from the analog synchronous process circuit.

The CKG has also a 1820 frequency division circuit. The 28.6 MHz clock input from the HVCO is processed into the 15.73 kHz reference clock derived by dividing the above clock by 1820) that is output from the HREF output terminal. The phase of this clock is compared with that of the horizontal oscillation output, a 15.73 kHz clock supplied by the analog synchronization circuit. The comparison result is used to control the VCO in 28.6 MHz. The PLL circuit incorporates in its configuration this output supplied to the HVCO terminal of the CKG.

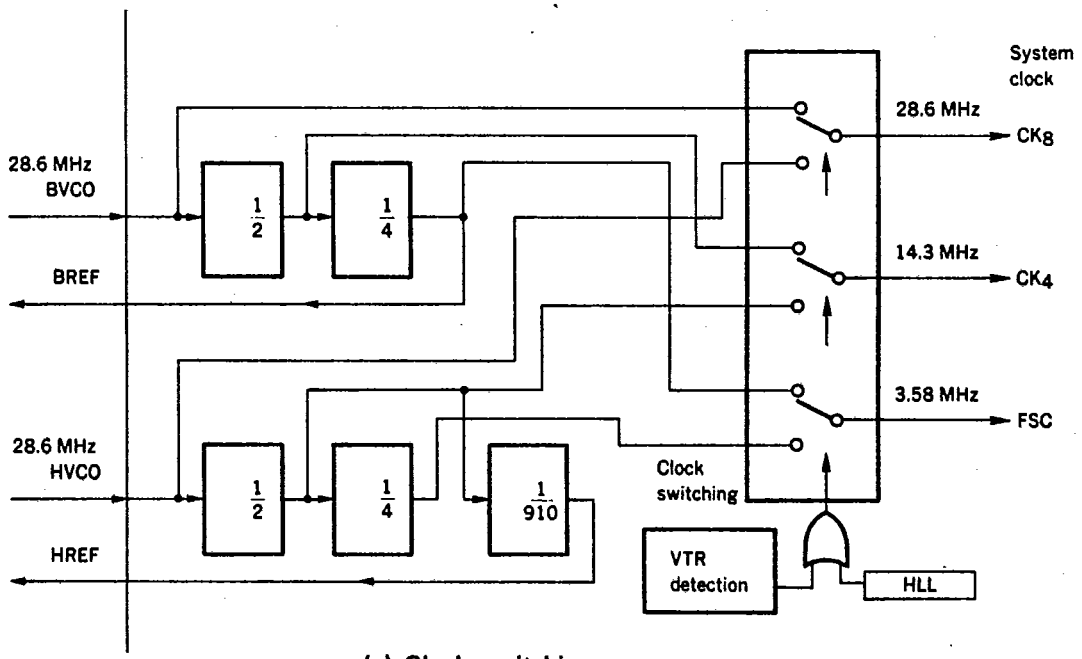
Fig. 1 Block Diagram of Clock Generator Circuit



(a) Burst lock PLL



(b) Line lock PLL



(c) Clock switching

2. TIMING GENERATOR CIRCUIT

Using the system clock generated by the clock generator, this circuit generates various timing signals required for the IDTV signal processing.

There are four timing signals that can be set with the output timing mode switching feature (MOD_1, MOD_2). In normal operation, the MODC is used.

The reference timing "0" is set at approximately 30 μs after the rise of the H-SYNC. Since this output is used for comparing the phase of this output with that of the HREF output, this point is also the "0" of the timing of the internal horizontal counter.

A/D	CLP
YCS	SBLK
YCP	PBLK, BF, FSC, VDB
CDU	FSC
Double-speed conversion, D/A	RE_1, RE_2, WRST, RRST, RRS_2, DCK_1, DCK_2
Double-speed RGB matrix	BBLK, BCLP
External RGB double-speed processing	EWR, ERR
Others	MSYN, MRS, MSET, HT

MODA ($MOD_1 = 0, MOD_2 = 0$)

With CDU — Provided with Additional Features

Terminal Abbr.	H Clock 1st		H Clock 2nd		V Scanning Lines	
	↗	↘	↗	↘	↗	↘
CLP	534	484				
SBLK	399	571			0.5	21.5
PBLK	412	580			0.5	21.5
BF	511	559				
HT	514	59				
WRST	532.5	531.5				
RRST	532.5	531.5	77.5	76.5		
RE_1	76	531				
RE_2	531	76				
MSYN	531	40	76	495	6.5	4
EBLK	546	390			21.5	0.5
EWR	479	478				
ERR	532.5	531.5	77.5	76.5		
BCLP	535	555	80	100		
BBLK	486	564	31	109	0.5	21.5
VDB					6.5	4

MODB ($MOD_1 = 0, MOD_2 = 0$)

Without CDU — Provided with Additional Features

Terminal Abbr.	H Clock 1st		H Clock 2nd		V Scanning Lines	
	↗	↘	↗	↘	↗	↘
CLP	534	484				
SBLK	399	571			0.5	21.5
PBLK	412	580			0.5	21.5
BF	504	552				
HT	507	52				
WRST	525.5	524.5				
RRST	525.5	524.5	70.5	69.5		
RE_1	524.5	524				
RE_2	524	69				
MSYN	524	33	69	488	6.5	4
EBLK	546	390			21.5	0.5
EWR	479	478				
ERR	525.5	524.5	70.5	69.5		
BCLP	528	548	73	93		
BBLK	478	557	24	102	0.5	21.5
VDB					6.5	4

MODC (MOD_1 = 0, MOD_2 = 0)
With CDU

No Additional Features

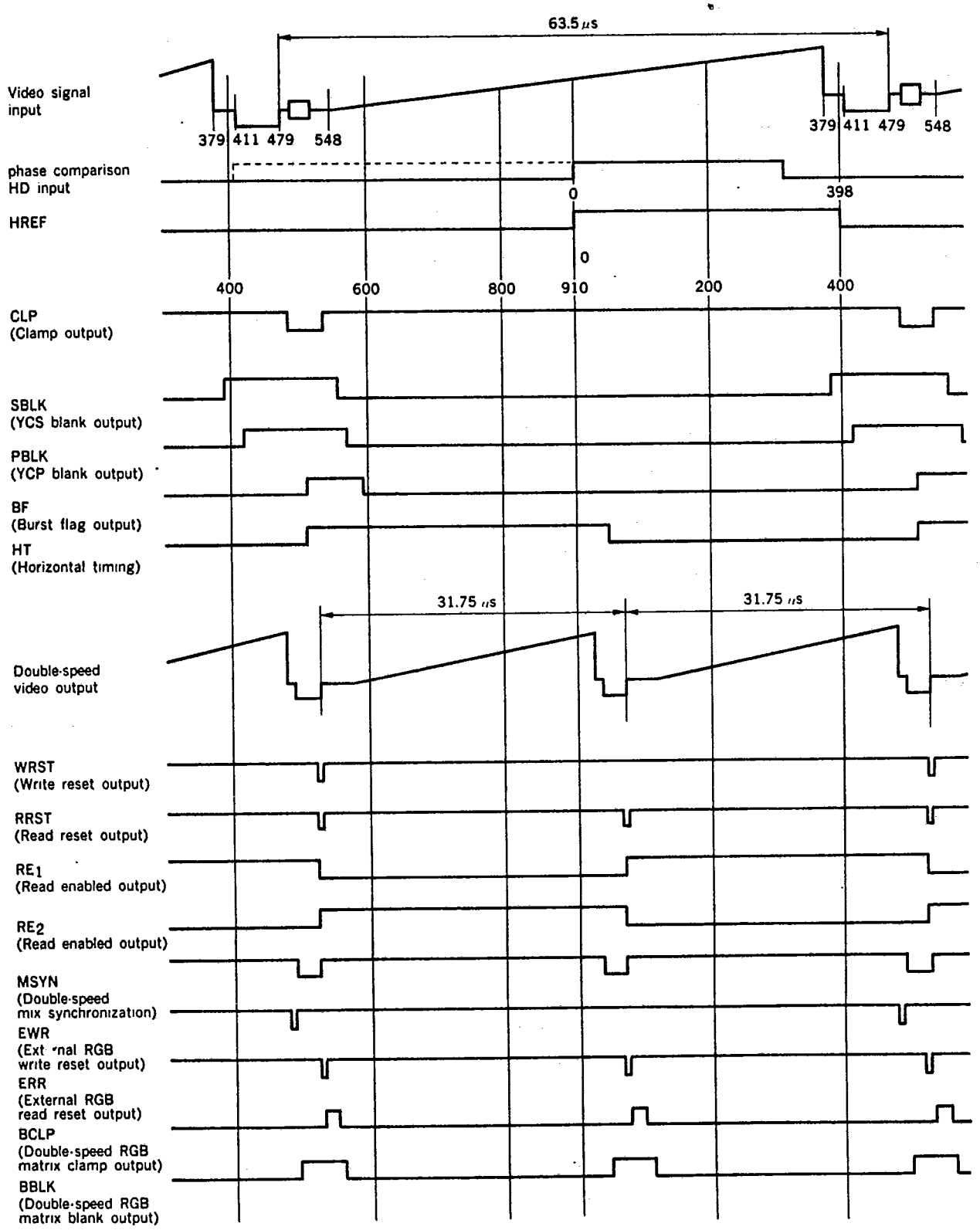
Terminal Abbr.	H				V	
	1st		2nd		Clock	Scanning Lines
	↗	↘	↗	↘	↗	↘
CLP	534	484				
SBLK	399	571			0.5	21.5
PBLK	412	580			0.5	21.5
BF	511	559				
HT	514	59				
WRST	522.5	521.5				
RRST	522.5	521.5	67.5	66.5		
RE_1	66	521				
RE_2	521	66				
MSYN	521	30	66	485	6.5	4
EBLK	546	390			21.5	0.5
EWR	479	478				
ERR	522.5	521.5	67.5	66.5		
BCLP	525	545	70	90		
BBLK	476	554	21	99	0.5	21.5
VDB					6.5	4

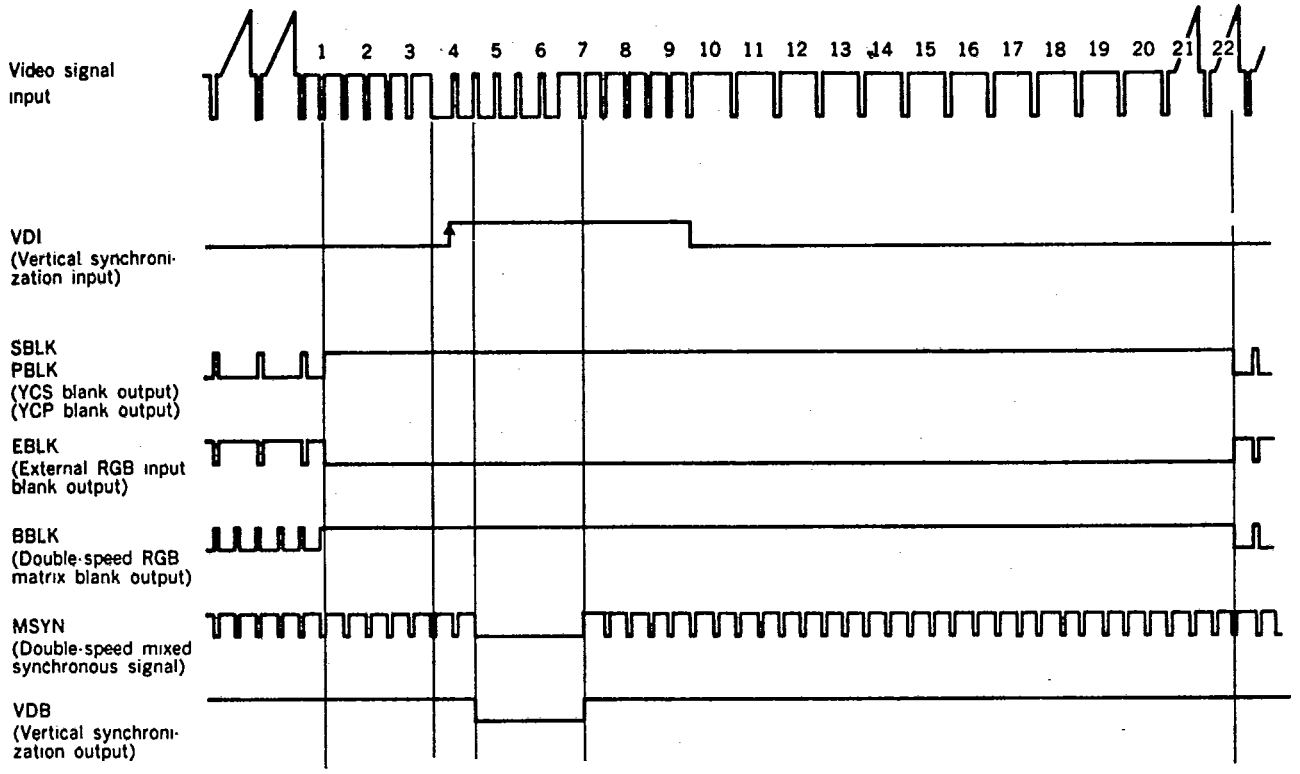
MODD (MOD_1 = 0, MOD_2 = 0)
Without CDU

No Additional Features

Terminal Abbr.	H				V	
	1st		2nd		Clock	Scanning Lines
	↗	↘	↗	↘	↗	↘
CLP	534	484				
SBLK	399	571			0.5	21.5
PBLK	412	580			0.5	21.5
BF	504	552				
HT	507	52				
WRST	515.5	514.5				
RRST	515.5	514.5	60.5	59.5		
RE_1	59	514				
RE_2	514	59				
MSYN	514	23	59	478	6.5	4
EBLK	546	390			21.5	0.5
EWR	479	478				
ERR	515.5	514.5	60.5	59.5		
BCLP	518	538	63	83		
BBLK	468	547	14	92	0.5	21.5
VDB					6.5	4

Fig. 2 Output Timing Waveform




Video signal input
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
VDI (Vertical synchronization input)
SBLK
PBLK
(YCS blank output)
(YCP blank output)
EBLK
(External RGB input blank output)
BBLK
(Double-speed RGB matrix blank output)
MSYN
(Double-speed mixed synchronous signal)
VDB
(Vertical synchronization output)

3. NONSTANDARD SIGNAL DETECTION CIRCUIT

This nonstandard signal detection circuit detects signals that are not based on the NTSC format. This circuit is composed of the following three circuits:

(1) VTR Detection Circuit
This circuits detects signals that have no interframe interleave correlation between the burst frequency and the horizontal synchronization frequency, such as the VTR signal.

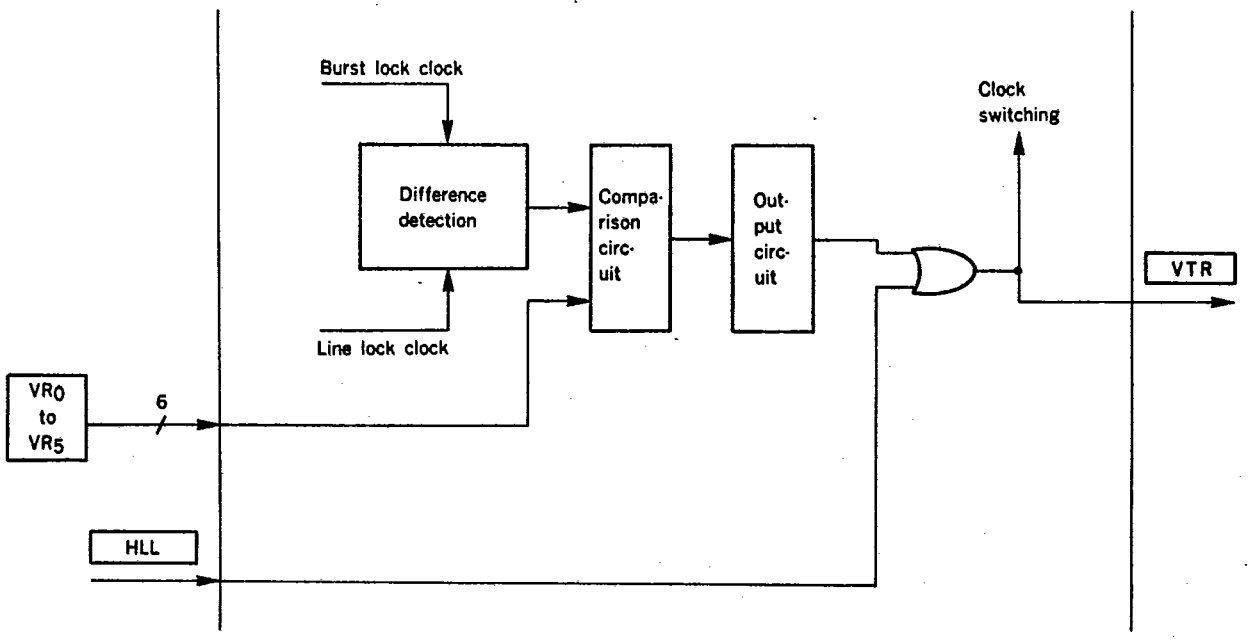
(2) Synchronous Detection Circuit
This circuit detects signals that differ from the correct NTSC signal even though they have no interframe or interleave correlation between the burst frequency and the horizontal synchronization frequency, such as the still picture VD.

(3) Interleave Detection Circuit
This circuit detects signals whose horizontal synchronous frequency differ significantly from the standard signal and whose interline Y/C interleave relationship is not correctly maintained, as in the case of VTR picture search or the family computer.

3-1 VTR Detection Circuit

This circuit detects signals that does not maintain interleave between the interframe Y and C signals due to lack of correlation between the burst frequency and the horizontal synchronous frequency, as in the case of the VTR signal.
This circut detects the difference in frequency between the brust lock clock and the line lock clock, compares it with the output from the VR terminal (VTR detection reference data), and, when the difference exceeds this data, sets the value of its output to "1."
This operation switches the system clock to the line lock. By connecting this VTR terminal with MSL of YCS LSI (μPD9320A) the YC separation is selected to with-in-field separation when VTR output is "H."

Fig. 3 Block Diagram of VTR Detection Circuit



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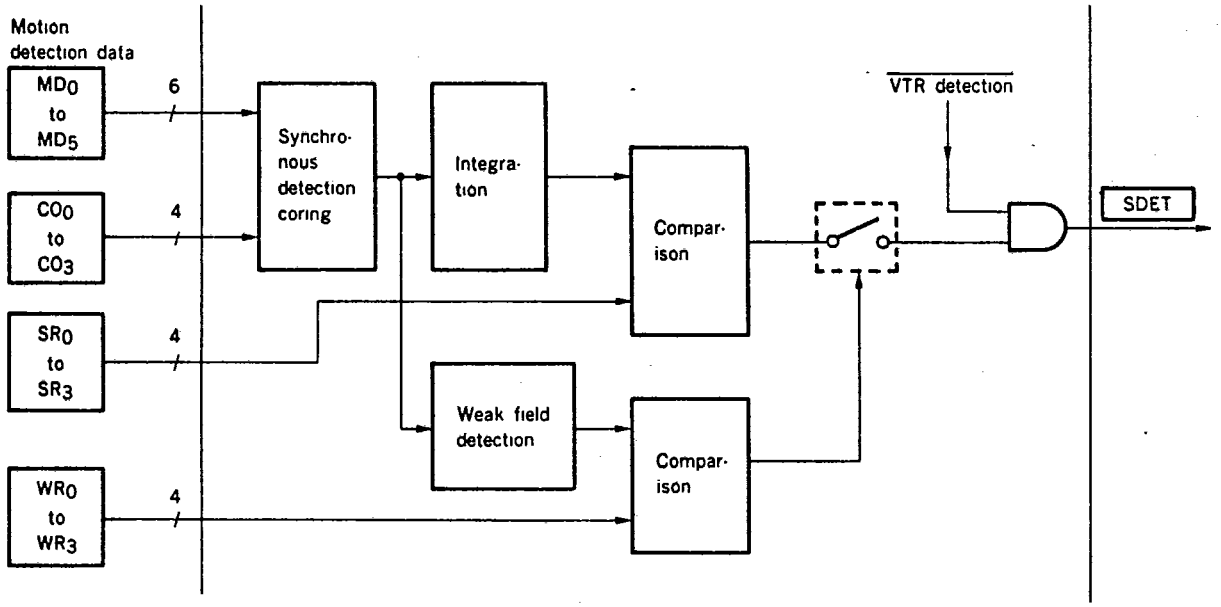
3-2 Synchronous Detection Circuit

This circuit detects signals that have no consistent interframe interleave correlation between the burst frequency and horizontal synchronization frequency, although it has some small correlation, or signals that differ from the correct NTSC signal, such as VD still picture signal.

This circuit detects the motion in the synchronous signal part of the luminance motion detection signal output from the motion detection LSI (MDP) and compares it with the set reference data (SR). When the difference exceeds the set data, this circuit sets it output to "H."

This circuit has a weak field detection circuit which prohibits synchronous detection in the weak field to achieve reliable operation of the synchronous detection circuit. When VTR output is "H", the SDET output becomes "L" compulsorily. By connecting this SDET terminal with VTR terminal of MDP LSI (μPD9323), the YC separation and the Y interpolation are selected to with-in-field processing when SDET output is "H."

Fig. 4 Block Diagram of Synchronous Detection Circuit



3-3 Interleave Detection Circuit

When the horizontal synchronous frequency differs significantly from the standard signal, the interline interleave relationship between the luminance and color signals is not correctly maintained, as in the case of VTR picture search or the family computer.

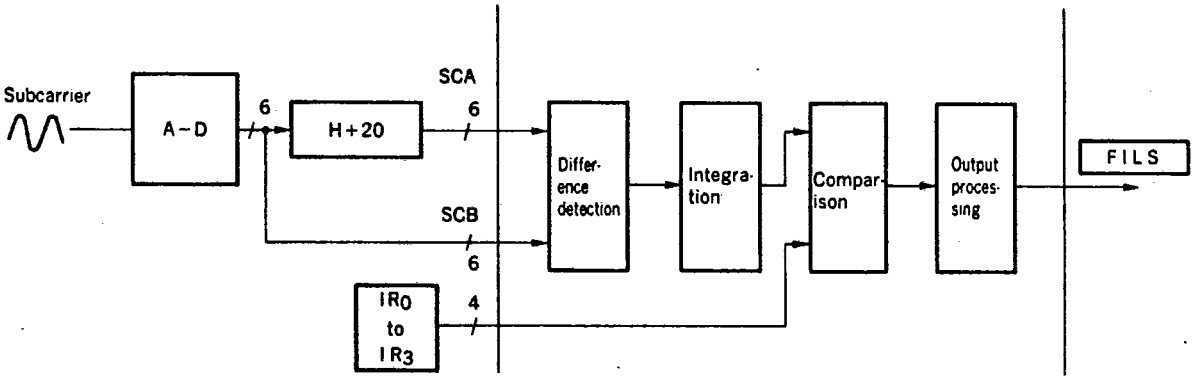
When the input signal has interline Y/C separation, the picture has no color.

To solve this problem, the system detects the interline interleave state in real time by means of an interleave detection circuit.

By sharing the function of the subcarrier waveform delay line in color demodulation (CDU), this circuit detects the phases at both ends of the line. When the difference between these ends exceeds the set value (IR), the output of the FILS terminal is set to "H."

This FILS terminal is connected to the filter selection terminal of the YC separation LSI, and switches between the interline YC separation and the frequency YC separation (BPF) when in-the-field YC separation mode is being selected. This process realizes the optimum YC separation to suit the signal.

Fig. 5 Block Diagram of Interleave Detection Circuit



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4. EXTERNAL CLAMPING PULSE INPUT

By inputting clamping pulse (Active Low) to CLPI terminal, the outputs of CLP and BF terminals are generated from inputted clamping pulse.
With this process clamping and burst gating are operated certainly.
When does not use external clamping operation, CLPI terminal must be connected to GND. At this time CLP and BF output signals are generated from internal counter.

Fig. 6 CLPI input timing

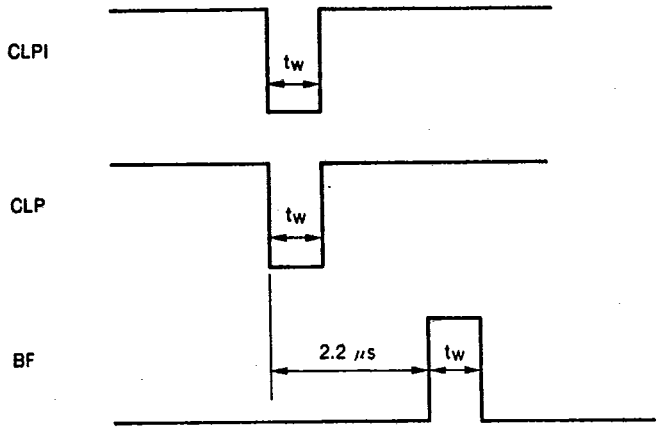
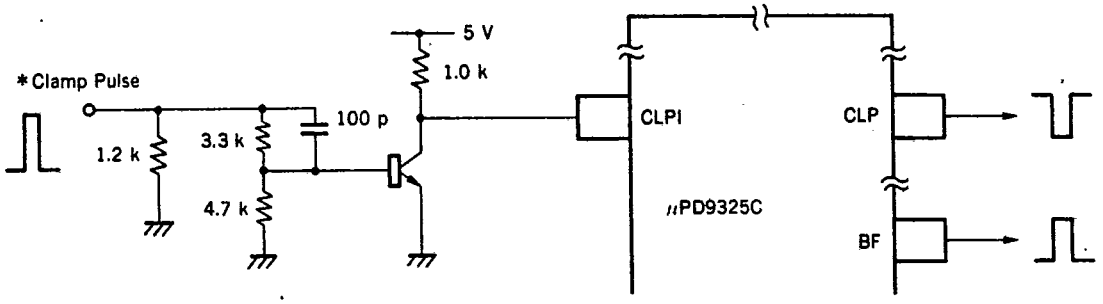
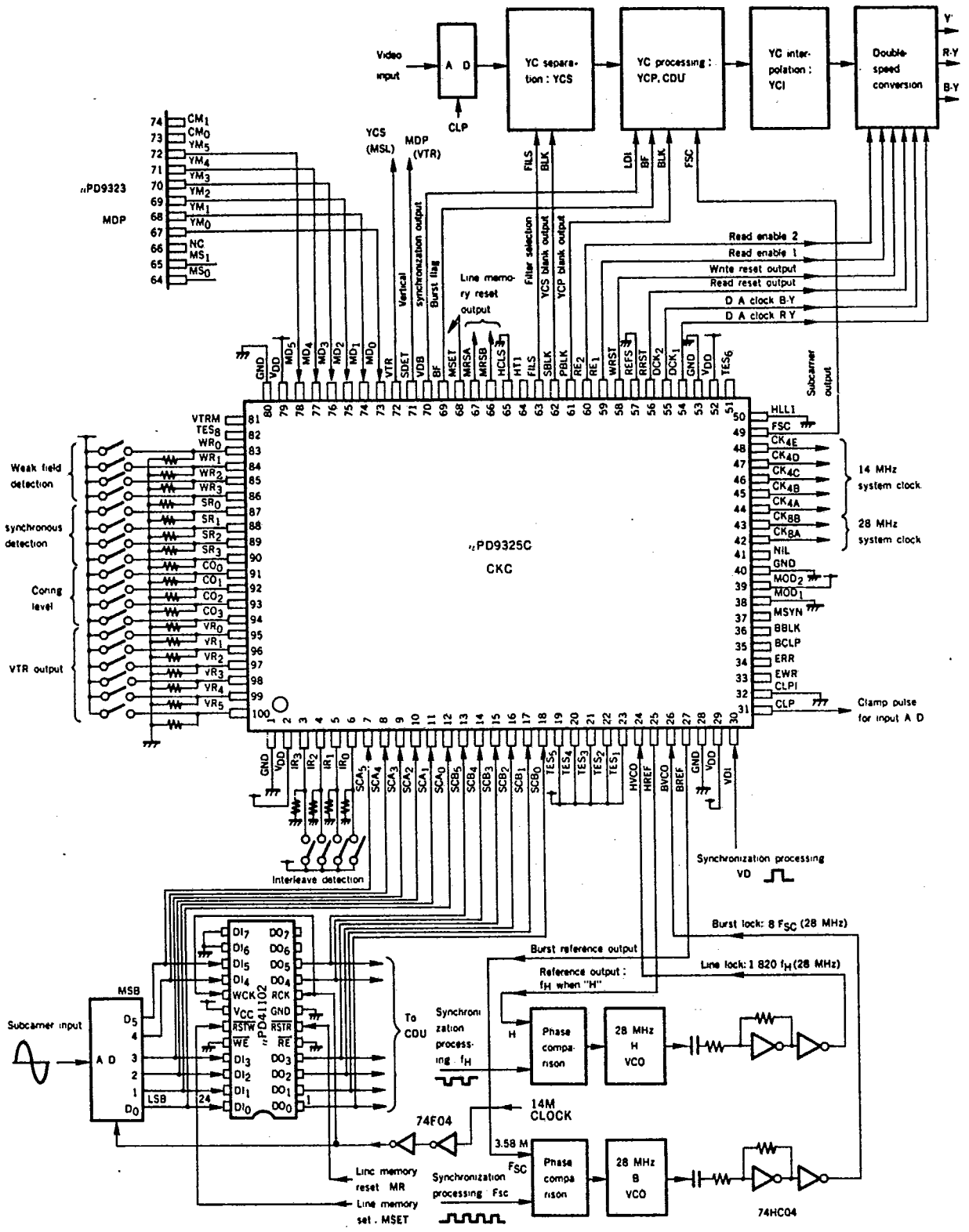


Fig. 7 External Clamping Operation Application Circuit

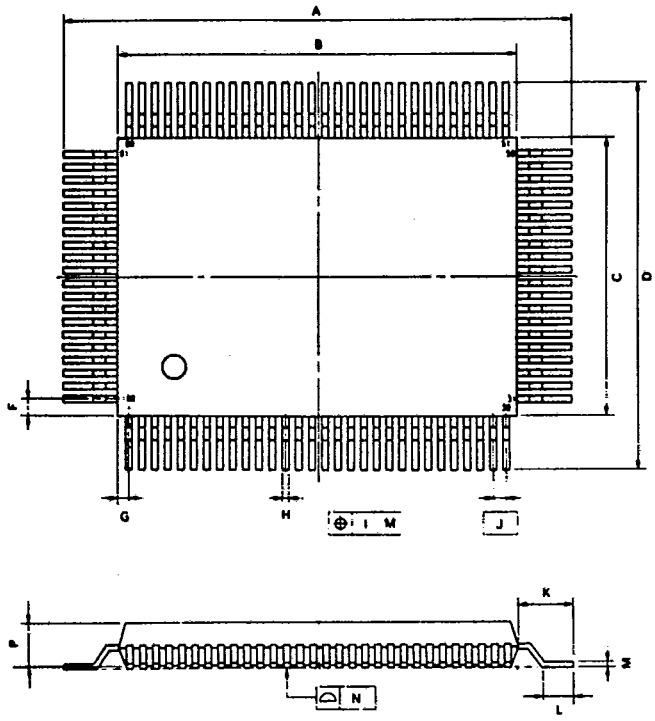


* Clamp Pulse must be input during also vertical interval.

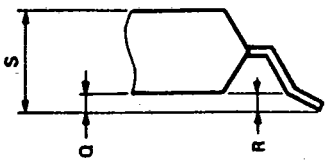
APPLICATION CIRCUIT:



100PIN PLASTIC QFP (14×20)



detail of lead end



P100GF-65-3BA-1

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.6^{+0.4}$	$0.929^{+0.016}$
B	$20.0^{+0.2}$	$0.795^{+0.009}_{-0.008}$
C	$14.0^{+0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.6^{+0.4}$	$0.693^{+0.016}$
F	0.8	0.031
G	0.6	0.024
H	$0.30^{+0.10}$	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	$1.8^{+0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{\pm0.2}$	$0.031^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm0.1}$	$0.004^{\pm0.004}$
R	$0.1^{\pm0.1}$	$0.004^{\pm0.004}$
S	3.0 MAX.	0.119 MAX.