

VM61012

12-CHANNEL, HIGH-PERFORMANCE, MAGNETO-RESISTIVE HEAD, READ/WRITE PREAMPLIFIER

950801

PRELIMINARY

August, 1995

FEATURES

- Read Gain = 450 V/V
- MR Bias Current Range = 8 - 18 mA
- Low Input Noise = 0.55 nV/√Hz Maximum
- Write Current Range = 10 - 35 mA
- Head Inductance Range = 100 - 700 nH
- Low Idle Power = 126 mW Maximum
- Rise Time = 5 ns Typical
- Power Supply Fault Protection
- +5V, -4.5V Power Supplies
- Write Unsafe Detection
- Head-to-Disk Contact Monitor
- Mask-Selectable Write Damping Resistor
- Reduced Mode and Head Selection Delays in FAST Mode
- Disk Voltage Monitor
- Differential PECL Write Data Inputs
- Current Sense Configuration

FUNCTIONAL DESCRIPTION

The VM61012 is an integrated bipolar read/write preamplifier designed for use in high-performance hard disk drive applications using 4-terminal magneto-resistive (MR) recording heads. The VM61012 contains a thin-film head writer, an MR reader and associated fault circuitry to address up to 12 heads. It also provides bias current and control loops for setting the DC voltages on the MR element.

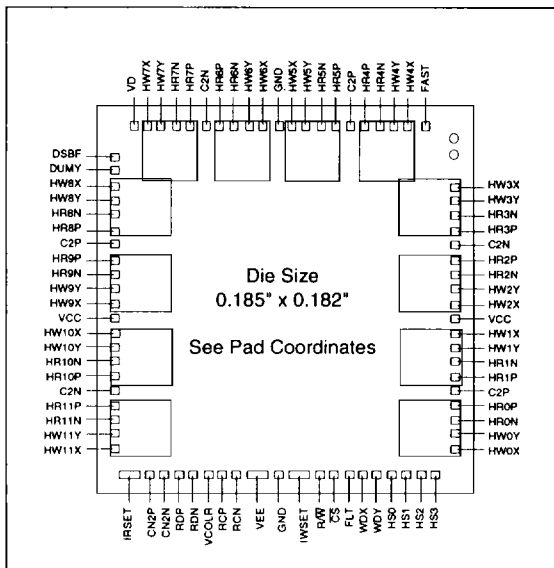
The VM61012 has two modes of operation. In read mode, the device operates as a low-noise differential preamplifier which senses resistance changes in the MR element that correspond to flux changes on the disk. The amplitude of the sense current is set either by an external resistor or by a current source and has a current gain of 20 mA/mA. In write mode, the circuit operates as a thin-film head write current switch, driving the thin-film write element of the MR head. The write current is externally programmed either by a resistor or an external current source and has a current gain of 20 mA/mA.

Fault protection is provided so during power sequencing, voltage faults or an invalid head select, the write current generator is disabled protecting the disk from potential transients. For added data protection, internal pull-up resistors are connected to the mode select lines, \overline{CS} and R/\overline{W} , to prevent accidental writing due to open lines and to ensure the device will power-up in a non-writing condition.

The VM61012 operates from a +5V, -4.5V power supply. Low power dissipation is achieved through the use of high-speed bipolar processing and innovative circuit design techniques. When deselected, the device enters a sleep mode which reduces the power dissipation to only 126mW.

The VM61012 is available in die form for chip-on-flex applications or in several package configurations. Please consult VTC for details.

DIE PAD DIAGRAM



ABSOLUTE MAXIMUM RATINGS

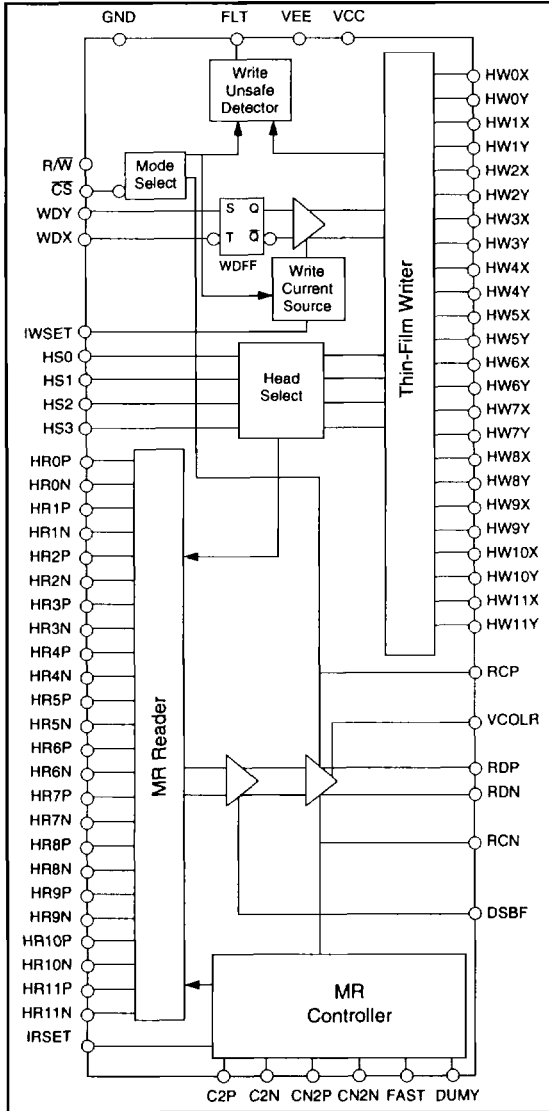
| | |
|--------------------------------------|------------------------------|
| Power Supply Voltage: | |
| V_{CC} | -0.3V to +7V |
| V_{EE} | -7V to +0.3V |
| Input Voltages: | |
| Digital Input Voltage V_{IN} | -0.3V to ($V_{CC} + 0.3V$) |
| Storage Temperature T_{stg} | -65° to 150°C |
| Junction Temperature T_J | 150°C |

RECOMMENDED OPERATING CONDITIONS

| | |
|----------------------------------|--------------|
| Power Supply Voltage: | |
| V_{CC} | +5V ± 10% |
| V_{EE} | -4.5V ± 10% |
| Junction Temperature T_J | 0°C to 125°C |



BLOCK DIAGRAM



CIRCUIT OPERATION

In all modes of operation, the VM61012 controls the common mode potential of all MR elements. This is necessary because the MR element cannot be insulated, so that a small voltage differential will cause arcing to the disk and damage the heads. Head voltages are held within $\pm 250\text{mV}$ of the voltage on the VD pin, which monitors the disk potential of the drive. Thus, the disk may be grounded, as is done in disk drives having conventional thin film or ferrite recording heads, or isolated as the application may require.

In read mode, the VM61012 activates the MR bias current source, which then drives the selected MR element. The read bias current magnitude is determined by an external resistor

connected between the IRSET pin and GND. An internally-generated 2.5 volt reference is present at the IRSET pin. The magnitude of the MR bias current is:

$$I_{MR} = 50/R_{RSET} \quad (\text{eq. 1})$$

where R_{RSET} is the resistor connected at IRSET.

The fault output pin, FLT, is high to indicate a non-fault condition. If the voltage drops below a certain threshold on either supply, FLT will be pulled low to indicate a fault. Also, if a head-to-disk contact occurs, the thermal asperity in the MR element will result in an abnormally high readback signal, which is monitored by detection circuitry and will be also flagged by a low FLT output.

The read preamplifier is activated and connected to the selected head. The write current source and write unsafe detection circuitry is deactivated. RDP and RDN outputs are emitter follower and are in phase with the HRnP and HRnN head ports. These outputs should be AC-coupled to the load. The output common mode voltage is maintained in the write mode, thereby substantially reducing the write-to-read recovery delay in the subsequent pulse detection circuitry.

Internal second stage resistors may be optionally removed at wafer test, allowing external resistors to be used in the application. The internal resistors are removed by blowing a pair of fuse links, and the discrete resistors are then connected from open collector output RCP to VCOLR, and from RCN to VCOLR. This provision allows tighter tolerance of read gain because of better tolerances available on discrete resistors. It also allows the user to choose the gain required for the application. The output can be taken at the emitter follower pair RDP-RDN, or at the open collector pair RCP-RCN if preferred.

In write mode, the preamplifier is shut off and the VM61012 is converted to a current switch. However, MR bias current is maintained in order to minimize the write-to-read delay. The write current source is activated and drives the thin film element of the selected head. The polarity of the current is initially into the WCN port following a read-to-write transition. Write current polarity is reversed on low-to-high transitions of the write data input (WDX low-to-high). Circuitry is activated to detect various fault conditions. If any of the faults occur, they will be flagged as a high voltage output on the FLT pin. In addition, if a VCC fault occurs, the write current source is deactivated in order to protect recorded data.

The write current magnitude is determined by an external resistor connected between the IWSET pin and GND. An internally-generated 2.5 volt reference is present at the IWSET pin. The magnitude of the write current (0-peak) is:

$$I_W = 50 / \left[R_W \times \left(1 + \frac{R_H}{R_D} \right) \right] \quad (\text{eq. 2})$$

where R_W is the resistor connected at IWSET, R_H is the series resistance of the head, and R_D is an internal damping resistor of 400Ω .

Power supply fault protection provides data security by disabling the write current generator during a VCC fault or power-up/down. The writer is independent of VEE, so VEE faults do not affect it. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin

FLT. Two positive transitions of write data may be required to clear the fault after the safe condition is restored.

- No write current
- Open write head
- Write Data frequency too low
- Device in read or idle mode
- Head shorted to ground

Fast mode is utilized during head-to-head and idle-to-read transitions. When the FAST mode pin is high, the unity-gain frequency of the offset control loop is increased such that it is inside the passband of the reader, allowing the delay to be reduced to less than 5µs. This pin must be brought low before read data is valid.

A DUMMY mode pin allows the selection of a dummy head in read or write mode. MR bias current is routed to an internal resistor, and the write current source is deactivated. This mode is optionally used during power-up/down and following head-to-disk contacts. When the DUMMY pin is high, the write current source is disabled to protect recorded data. An internal pull-up resistor is provided in event of an accidental open. If this pin is not used it should be grounded for normal operation.

In idle mode, the MR bias and write current sources are deactivated, and the device enters a low-power mode in which power dissipation is less than 126mW. Write and read fault detection circuitry is disabled. MR common mode and offset control loops still receive power in order to reduce idle-to-read mode recovery.

Mode control and head selection are accomplished via \overline{CS} , R/\overline{W} , and HS0-3 pins. Internal pull-up resistors are provided on \overline{CS} and R/\overline{W} pins to force the device into a non-writing condition if either control line is opened accidentally. In addition, invalid head select codes disable the writer and select head HS00. Truth tables for mode and head selection are shown in Table 1 and Table 2, respectively.

Table 1: Mode Select Logic

| R/W | \overline{CS} | MODE |
|-----|-----------------|-------|
| 0 | 0 | Write |
| 1 | 0 | Read |
| X | 1 | Idle |

Table 2: Head Select Logic

| HS3 | HS2 | HS1 | HS0 | DUMMY | HEAD |
|-----|-----|-----|-----|-------|-------|
| X | X | X | X | 1 | DUMMY |
| 0 | 0 | 0 | 0 | 0 | 00 |
| 0 | 0 | 0 | 1 | 0 | 01 |
| 0 | 0 | 1 | 0 | 0 | 02 |
| 0 | 0 | 1 | 1 | 0 | 03 |
| 0 | 1 | 0 | 0 | 0 | 04 |
| 0 | 1 | 0 | 1 | 0 | 05 |
| 0 | 1 | 1 | 0 | 0 | 06 |
| 0 | 1 | 1 | 1 | 0 | 07 |
| 1 | 0 | 0 | 0 | 0 | 08 |
| 1 | 0 | 0 | 1 | 0 | 09 |
| 1 | 0 | 1 | 0 | 0 | 10 |
| 1 | 0 | 1 | 1 | 0 | 11 |
| 1 | 1 | X | X | 0 | 00 |

PIN_FUNCTION LIST AND DESCRIPTION

- | | | |
|---------------------|------|---|
| 1) \overline{CS} | (I) | Chip select: a low level enables the device. |
| 2) R/\overline{W} | (I*) | Read/Write: a high level enables read mode. |
| 3) HS0-HS3 | (I*) | Head Select: selects one of the twelve heads. |
| 4) DUMMY | (I*) | A high level enables the dummy mode. |
| 5) FAST | (I*) | A high level enables fast settling of the reader. |
| 6) FLT | (O*) | Write/Read Fault: A high level indicates a fault in write mode. A low level indicates a fault in read mode. |
| 7) WDX, WDY | (I*) | Differential Pseudo-ECL write data in: a positive edge on WDX toggles the direction of the head current. |
| 8) HR0P-HR11P | (I) | MR head connections, positive end. |
| 9) HR0N-HR11N | (I) | MR head connections, negative end. |
| 10) HW0X-HW11X | (O) | Write head connections, positive end. |
| 11) HW0Y-HW11Y | (O) | Write head connections, negative end. |
| 12) RDP, RDN | (O*) | Read Data: Differential read signal outputs. |
| 13) IWSET | (*) | Write current pin: used to set the magnitude of write current. |
| 14) IRSET | (*) | MR bias reference pin: used to set the magnitude of MR bias current. |
| 15) C2P,C2N | (*) | Compensation capacitor for the MR head current loop. |
| 16) CN2P, CN2N | (*) | Noise bypass for the MR bias current generator. |
| 17) VD | (I*) | Analog reference for the disk bias. |
| 18) DSBF | (*) | Disables disk contact detector if tied to GND. |
| 19) RCP, RCN | | Differential output for connection of external gain-setting resistors. |
| 20) VCOLR | (*) | Common mode output for connection of external resistors RCP, RCN. |
| 21) VEE | - | -4.5V supply |
| 22) VCC | - | +5V supply |
| 23) GND | - | Ground |

* When more than one device is used, these signals can be wire OR'ed together
 I = Input pin
 O = Output pin



STATIC (DC) CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, $0^{\circ}\text{C} < T_A < 80^{\circ}\text{C}$, $4.5\text{V} < V_{\text{CC}} < 5.5\text{V}$, $-5.0\text{V} < V_{\text{EE}} < -4.0\text{V}$.

| PARAMETER | SYM | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|------------------|---|-------|-----|-------|---------------|
| V_{CC} Power Supply Current | I_{CC} | Read Mode, $I_{\text{MR}} = 16\text{mA}$ | | | 95 | mA |
| | | Write Mode, $I_{\text{W}} = 20\text{mA}$, $I_{\text{MR}} = 16\text{mA}$ | | | 140 | mA |
| | | Idle Mode | | | 12 | mA |
| V_{EE} Power Supply Current | I_{EE} | Read Mode, $I_{\text{MR}} = 16\text{mA}$ | | | 70 | mA |
| | | Write Mode, $I_{\text{W}} = 20\text{mA}$, $I_{\text{MR}} = 16\text{mA}$ | | | 65 | mA |
| | | Idle Mode | | | 12 | mA |
| Power Supply Dissipation | P_{d} | Read Mode, $I_{\text{MR}} = 16\text{mA}$ | | | 873 | mW |
| | | Write Mode, $I_{\text{W}} = 20\text{mA}$, $I_{\text{MR}} = 16\text{mA}$ | | | 1095 | mW |
| | | Idle Mode | | | 126 | mW |
| Input High Voltage | V_{IH} | PECL | 3.27 | | 4.27 | V |
| | | CMOS | 3.5 | | | V |
| Input Low Voltage | V_{IL} | PECL | 3.05 | | 3.55 | V |
| | | CMOS | | | 1.65 | V |
| Disk Reference Voltage Range | V_{D} | | -250 | | 250 | mV |
| Input High Current | I_{IH} | PECL | | | 120 | μA |
| | | CMOS | -160 | | 160 | μA |
| Input Low Current | I_{IL} | PECL | | | 120 | μA |
| | | CMOS | -160 | | 160 | μA |
| Output High Current | I_{OH} | FLT: $V_{\text{OH}} = 5.0\text{V}$ | | | 50 | μA |
| Output Low Voltage | V_{OL} | FLT: $I_{\text{OL}} = 4\text{mA}$ | | | 0.5 | V |
| V_{CC} Fault Threshold | V_{DTH} | | 3.75 | | 4.25 | V |
| V_{EE} Fault Threshold | V_{ETH} | | -3.75 | | -3.25 | V |

**DYNAMIC (AC) CHARACTERISTICS**

READ MODE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0^{\circ}\text{C} < T_A < 80^{\circ}\text{C}$, $4.5\text{V} < V_{CC} < 5.5\text{V}$, $-5.0\text{V} < V_{EE} < -4.0$.

| PARAMETER | SYM | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|------------------|--|----------------|----------------|----------------|------------------|
| MR Head Current Range | I_{MR} | | 8 | | 18 | mA |
| MR Head Current Tolerance | I_{MR} | $8 < I_{MR} < 18\text{ mA}$ | -5 | | +5 | % |
| MR Bias Reference Voltage | V_{RSET} | $2775 < R_{RSET} < 6250\Omega$ | | 2.5 | | V |
| IRSET to MR Bias Current Gain | A_{IMR} | $2775 < R_{RSET} < 6250\Omega$ | | 20 | | mA/mA |
| Differential Voltage Gain | A_V | $V_{IN} = 1\text{mV}_{pp}$ @ 10MHz, R_L (RDP, RDN) = 1kW, $I_{MR} = 16\text{mA}$, $R_{MR} = 12\Omega$ | 340 | 450 | 560 | V/V |
| Passband Upper Frequency Limit | f_{HR} | -1dB: $R_{MR} = 13\Omega$; $L_{MR} = 20\text{nH}$ | | 40 | | MHz |
| | | -3dB | 60 | | | |
| Passband Lower -3dB Frequency Limit | f_{LR} | $R_{MR} = 12\Omega$; $L_{MR} = 20\text{nH}$ | 0.1 | | 0.5 | MHz |
| Equivalent Input Noise | e_n | $R_{MR} = 13\Omega$; $I_{MR} = 16\text{mA}$; $1 < f < 20\text{ MHz}$ | | | 0.55 | nV/√Hz |
| Differential Input Capacitance | C_{IN} | $R_{MR} = 12\Omega$; $I_{MR} = 16\text{mA}$ | | | 10 | pF |
| Differential Input Resistance | R_{IN} | $I_{MR} = 16\text{mA}$ | | | 4 | Ω |
| Dynamic Range | DR | AC input V where A_V falls to 90% of its value at $V_{IN} = 1\text{mV}_{pp}$ @ $f = 10\text{ MHz}$ | 4 | | | mV_{pp} |
| Common Mode Rejection Ratio | CMRR | $V_{CM} = 100\text{mV}_{pp}$, $I_{MR} = 16\text{mA}$, $R_{MR} = 12\Omega$, $1 < f < 50\text{ MHz}$ | 30 | | | dB |
| Power Supply Rejection Ratio | PSRR | 100mV_{pp} @ 5MHz, on V_{CC} or V_{EE} , $I_{MR} = 16\text{mA}$, $R_{MR} = 12\Omega$, $1 < f < 50\text{ MHz}$ | 30 | | | dB |
| Channel Separation | CS | Unselected Channels: $V_{IN} = 100\text{mV}_{pp}$ @ 5MHz, $1 < f < 50\text{ MHz}$ | 30 | | | dB |
| Output Offset Voltage | V_{OS} | $I_{MR} = 16\text{mA}$, $R_{MR} = 12\Omega$ | | | 100 | mV |
| Common Mode Output Voltage | V_{OCM} | | $V_{CC} - 2.4$ | $V_{CC} - 2.1$ | $V_{CC} - 1.8$ | V |
| Common Mode Output Voltage Difference | ΔV_{OCM} | $V_{OCM}(\text{READ}) - V_{OCM}(\text{WRITE})$ | -350 | | 350 | mV |
| Single-Ended Output Resistance | R_{SEO} | | | | 40 | Ω |
| Output Current | I_O | AC Coupled Load, RDP to RDN | ± 1.5 | | | mA |
| Total Harmonic Distortion | THD | $V_{in} = 4\text{mV}_{pp}$; ten harmonics | | | 0.5 | % |
| MR Head-to-Disk Contact Current | I_{DISK} | Extended contact, $R_{DISK} = 10\text{M}\Omega$ | | | 100 | μA |
| | | Maximum peak discharge, $C_{DISK} = 300\text{pF}$, $R_{DISK} = 10\text{M}\Omega$ | | | 20 | mA |
| MR Head Potential | V_{MR} | $I_{MR} = 16\text{mA}$, $R_{MR} = 12\Omega$ | -400 | | 400 | mV |



WRITE MODE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.
 $0^{\circ}\text{C} < T_A < 80^{\circ}\text{C}$, $4.5\text{V} < V_{CC} < 5.5\text{V}$, $-5.0 < V_{EE} < -4.0$, $I_W = 20\text{mA}$, $L_H = 500\text{nH}$, $R_H = 30\Omega$, $f_{\text{DATA}} = 5\text{MHz}$.

| PARAMETER | SYM | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------|-----------------------------------|-----|-----|-----|---------------------------|
| I_{WSET} Pin Voltage | V_{WSET} | | | 2.5 | | V |
| I_{WSET} to Write Current Gain | A_I | | | 20 | | mA/mA |
| Write Current Constant | K_W | $K_W = V_{\text{WSET}} \cdot A_I$ | 46 | 50 | 54 | V |
| Write Current Range | I_W | | 6 | | 30 | mA |
| Write Current Tolerance | ΔI_W | $6 < I_W < 30 \text{ mA}$ | -8 | | +8 | % |
| Differential Head Voltage Swing | V_{DH} | Open head | 4.5 | 6.5 | | V_{pp} |
| Unselected Head Transition Current | I_{UH} | $I_W = 30\text{mA}$ | | | 50 | μA_{pk} |
| Differential Output Capacitance | C_O | | | | 6 | pF |
| Differential Output Resistance | R_O | Internal damping resistance | 320 | 400 | 480 | Ω |
| Write Data Frequency for Safe Condition | f_{DATA} | FLT = Low | 1.0 | | | MHz |



SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified. $0^{\circ}\text{C} < T_A < 80^{\circ}\text{C}$, $4.5\text{V} < V_{CC} < 5.5\text{V}$, $-5.0 < V_{EE} < -4.0$, $I_W = 20\text{mA}$, $L_H = 500\text{nH}$, $R_H = 30\Omega$, $f_{\text{DATA}} = 5\text{MHz}$.

| PARAMETER | SYM | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|-------------------|---|-----|-----|-----|---------------|
| R \overline{W} to Write Mode | t_{RW} | To 90% of write current | | | 0.5 | μs |
| R \overline{W} to Read Mode | t_{WR} | To 90% of envelope | | | 0.5 | μs |
| CS to Read Mode | t_{CS} | To 90% of envelope; FAST = low | | | 50 | μs |
| | | † Fast = high for 3.5 μs | | | 5 | μs |
| $\overline{\text{CS}}$ to Write Mode | t_{CS} | To 90% of write current | | | 0.5 | μs |
| HS0 - HS3 to Any Head | t_{HS} | To 90% of envelope; FAST = low | | | 50 | μs |
| | | † FAST = high for 3.5 μs | | | 5 | μs |
| DUMMY Mode to Any Head | t_{DH} | To 90% of envelope; FAST = low | | | 50 | μs |
| | | † FAST = high for 3.5 μs | | | 5 | μs |
| $\overline{\text{CS}}$ to Unselect | t_{RI} | To 10% of read envelope or write current | | | 0.6 | μs |
| Safe to Unsafe* | t_{D1} | 50% WDX to 50% FLT | 0.6 | | 3.6 | μs |
| Unsafe to Safe* | t_{D2} | 50% WDX to 50% FLT | | | 1 | μs |
| Head Current Propagation Delay* | t_{D3} | From 50% points | | | 30 | ns |
| Asymmetry | A_{SYM} | Write Data has 50% duty cycle & 1ns rise/fall time, $L_H = 0$, $R_H = 0$ | | | 1.0 | ns |
| Rise/Fall Time | t_r / t_f | 20-80%; $I_W = 20\text{mA}$; $L_H = 550\text{nH}$, $R_H = 40\Omega$ | | 4.8 | 6 | ns |
| | | $L_H = 0$, $R_H = 0$; $I_W = 20\text{mA}$ | | | 3 | ns |
| Settling Time | T_{WSET} | $I_{\text{WC}} = 20\text{mA}$, $L_H = 550\text{nH}$, $R_H = 40\Omega$; to $\pm 10\%$ | | | 15 | ns |
| Overshoot | W_{COV} | $I_{\text{WC}} = 20\text{mA}$; $L_H = 550\text{nH}$, $R_H = 40\Omega$ | | 25 | | % |

*See Figure 1 for write mode timing diagram.

† See Figure 2 for read mode timing diagram.

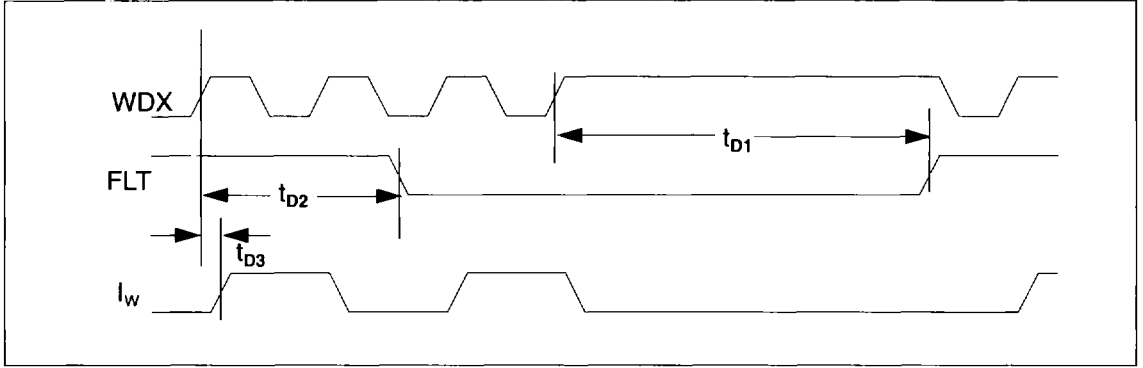


Figure 1: Write Mode Timing Diagram

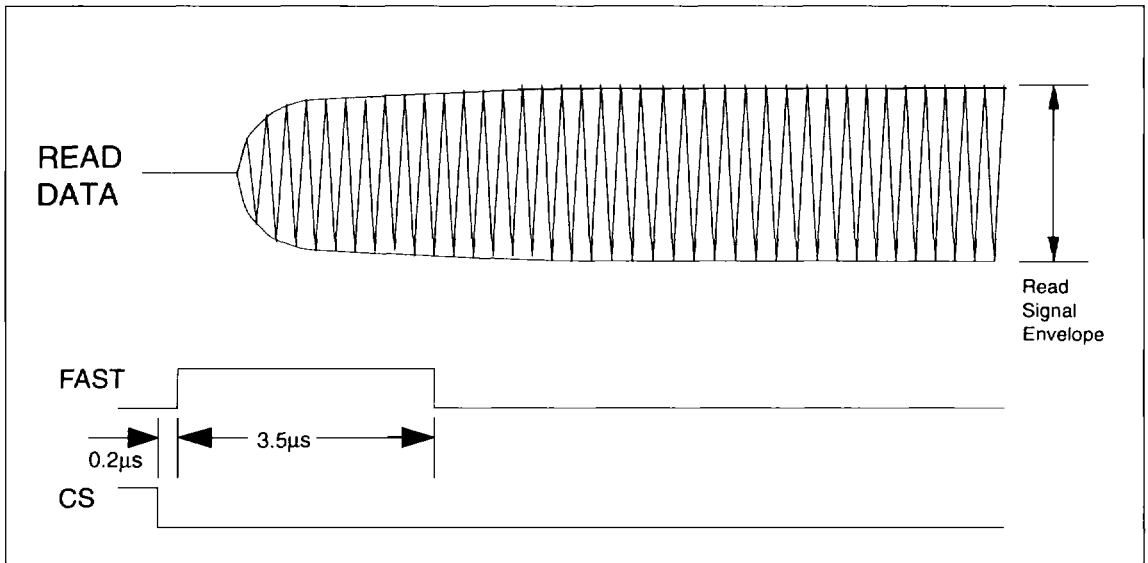
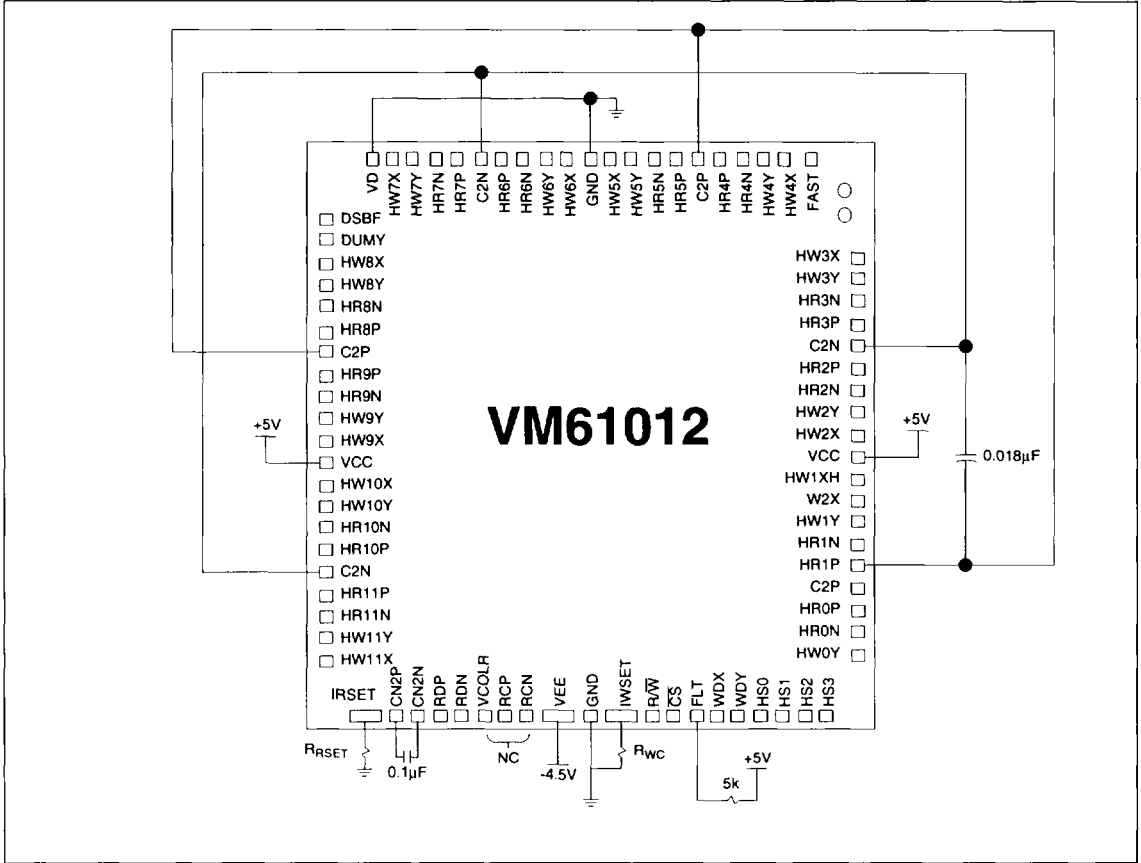


Figure 2: Read Mode Timing Diagram. Also applies to DUMY and HS0 - HS3.



TYPICAL CONNECTION DIAGRAM



Note 1: $IRSET = MR \text{ Bias Current} = 50/R_{RSET}$

Note 2: $I_{WSET} = \text{Write Current} = 50/R_{WC}(1 + R_H/360)$, $R_H = \text{Head Series Resistance}$

Note 3: $V_{CC} = +5V$, $GND = \text{Ground}$, $V_{EE} = -4.5V$



VM61012 PAD COORDINATES

| PIN NAME | X AXIS | Y AXIS |
|--------------------|----------|----------|
| HW11X | -2063.25 | -1809.00 |
| HW11Y | -2063.25 | -1629.00 |
| HR11N | -2063.25 | -1449.00 |
| HR11P | -2063.25 | -1269.00 |
| C2N | -2063.25 | -1089.00 |
| HR10P | -2063.25 | -909.00 |
| HR10N | -2063.25 | -729.00 |
| HW10Y | -2063.25 | -549.00 |
| HW10X | -2063.25 | -369.00 |
| V _{CC} :P | -2063.25 | -189.00 |
| HW9X | -2063.25 | -9.00 |
| HW9Y | -2063.25 | 171.00 |
| HR9N | -2063.25 | 351.00 |
| HR9P | -2063.25 | 531.00 |
| C2P | -2063.25 | 711.00 |
| HR8P | -2063.25 | 891.00 |
| HR8N | -2063.25 | 1071.00 |
| HW8Y | -2063.25 | 1251.00 |
| HW8X | -2063.25 | 1431.00 |
| DUMMY | -2063.25 | 1618.00 |
| DSBF | -2063.25 | 1814.75 |
| VD | -1820.00 | 2172.00 |
| HW7X | -1620.00 | 2172.00 |
| HW7Y | -1440.00 | 2172.00 |
| HR7N | -1260.00 | 2172.00 |
| HR7P | -1080.00 | 2172.00 |
| C2N | -900.00 | 2172.00 |
| HR6P | -720.00 | 2172.00 |
| HR6N | -540.00 | 2172.00 |
| HW6Y | -360.00 | 2172.00 |
| HW6X | -180.00 | 2172.00 |
| V _{CC} | 0.00 | 2172.00 |
| HW5X | 180.00 | 2172.00 |
| HW5Y | 360.00 | 2172.00 |
| HR5N | 540.00 | 2172.00 |
| HR5P | 720.00 | 2172.00 |
| C2P | 900.00 | 2172.00 |
| HR4P | 1080.00 | 2172.00 |
| HR4N | 1260.00 | 2172.00 |
| HW4Y | 1440.00 | 2172.00 |
| HW4X | 1620.00 | 2172.00 |
| FAST | 1860.00 | 2172.00 |
| HW3X | 2063.25 | 1431.00 |
| HW3Y | 2063.25 | 1251.00 |
| HR3N | 2063.25 | 1071.00 |
| HR3P | 2063.25 | 891.00 |
| C2N | 2063.25 | 711.00 |
| HR2P | 2063.25 | 531.00 |
| HR2N | 2063.25 | 351.00 |
| HW2Y | 2063.25 | 171.00 |
| HW2X | 2063.25 | -9.00 |
| V _{CC} | 2063.25 | -189.00 |
| HW1X | 2063.25 | -369.00 |
| HW1Y | 2063.25 | -549.00 |
| HR1N | 2063.25 | -729.00 |
| HR1P | 2063.25 | -909.00 |
| C2P | 2063.25 | -1089.00 |
| HR0P | 2063.25 | -1269.00 |

| | | |
|-----------------|----------|----------|
| HR0N | 2063.25 | -1449.00 |
| HW0Y | 2063.25 | -1629.00 |
| HW0X | 2063.25 | -1809.00 |
| HS3 | 1896.50 | -2171.75 |
| HS2 | 1716.50 | -2171.75 |
| HS1 | 1536.50 | -2171.75 |
| HS0 | 1356.50 | -2171.75 |
| WDY | 1176.50 | -2171.75 |
| WDX | 996.50 | -2171.75 |
| FLT | 816.50 | -2171.75 |
| CSN | 636.50 | -2171.75 |
| RNW | 456.50 | -2171.75 |
| IWSET | 206.50 | -2171.75 |
| GND | -53.50 | -2171.75 |
| V _{EE} | -308.50 | -2171.75 |
| RCN | -563.50 | -2171.75 |
| RCP | -743.50 | -2171.75 |
| VCOLR | -923.50 | -2171.75 |
| RDN | -1103.50 | -2171.75 |
| RDP | -1283.50 | -2171.75 |
| CN2N | -1463.50 | -2171.75 |
| CN2P | -1643.50 | -2171.75 |
| IRSET | -1897.50 | -2171.75 |

1. Octagonal pins are for factory use only.
2. The die was designed so only one C2N pad needs to be bonded out. This is currently being verified.
3. The die was designed so only one C2P pad needs to be bonded out. This is currently being verified.
4. The capacitor connected to CN2N must also be connected to V_{EE}.