ADVANCE INFORMATION

Features/Benefits

- **20 inputs; 12 external, 8 feedback**
- **6 ns max. propagation delay**
- **32 product terms**
- **Product term sharing**
- **Programmable output polarity**
- **10KH ECL compatible**
- **24-pin SKINNYDIP®**
- **50Ω termination drive**
- **Input pull-down resistors**
- **Voltage compensated**
- **Compatible with TTL programmers**

Description

This ECL PAL® device has a 20P8 architecture, is ECL 10KH compatible, and has a simple programming algorithm. The 10HPAL20P8 is a 20-input, 8-output PAL part. Outputs have a polarity fuse and can drive a 50 Ω termination to -2.0 V.

Product term sharing allows the choice of one of two outputs for the given product term. Product terms are grouped in multiples of eight per output pair allowing up to eight product terms to be associated with any output term.

Features

The following description explains some of the features of the 10HPAL20P8. Features to be programmed into the PAL device are completely specified by the Boolean equations and automatically configured by the PAL assembler (PALASM)™.

Product Term Sharing

The basic configuration is eight product terms shared between two output cells. For each output a product term can be used by either output, but since the product term sharing is exclusive, a product term can be used by only one output, not both. If the same product term is needed by the same output pair, then two product terms are generated, one for each output.

Programmable Polarity

Output polarity is defined by comparison of the pin list and the equations. If the logic sense of a specific output is different from the logic sense of that output as defined by its equation, the output is inverted. If the logic sense of a specific output is the same as the logic sense of that output as defined by its equation, the output is active high polarity.

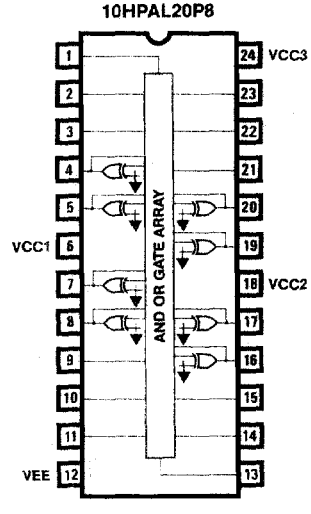
Preliminary Data

- 6 ns maximum propagation delay
- ~230 mA maximum I_{EE} current

Areas of Application

- High-performance communication equipment
- High-speed test instrumentation
- Mainframes or Super-minis
- Computer-aided graphics

Pin Configuration



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* Patent pending.

Logic Diagram

10HPAL20P8