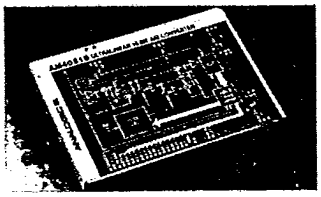
T-51-10-16



ANALOGIC

AM30516/ AM40516

Wide Dynamic Range High-Speed, 16-Bit Sampling A/D Converters

Performance Features

The AM30516/AM40516 16-bit A/D converter, designed with a unique sub-ranging architecture, achieves excellent speed, accuracy, and linearity. For digitizing fast time-varying signals, the AM40516 has a built-in sample-and-hold amplifier; for applications with multiplexed "dc" signals or an external sample-and-hold, the more economical AM30516 is available with a high impedance input buffer in place of the sample-and-hold. With 125 kHz sampling rate, the AM40516 can digitize input signals containing frequency components as high as the theoretical 62.5 kHz Nyquist rate. The high sampling rate and the superior zero-crossing linearity of the AM40516 optimize this converter for digitizing multiplexed signals in professional audio equipment. With its low distortion and 96 dB dynamic range, the AM30516/AM40516 is ideal for digitizing signals in frequency-division-multiplexed (FDM) telecommunications systems.

The AM30516/AM40516's sub-ranging architecture uses a three-pass recycling technique in a design

(continued)

Features

- 16-Bit Resolution
- No Missing Codes
- Wide Dynamic Range: 96 dB
- Signal to Noise Ratio: 95 dB (1 kHz)
- Peak Distortion: −98 dB (1 kHz)
- Total Harmonic Distortion: −88 dB (1 kHz)
- ±0.5 LSB Differential Non-Linearity Around Zero
- 200 kHz Conversion Rate (AM30516)
- 125 kHz Throughput Rate (AM40516)
- Ease of Use
- Built-In S/H Amplifier (AM40516)
- TTL Compatibility
- Low Cost
- High Input Impedance ($10^8\Omega$)
- Low Power
- Electromagnetic/Electrostatic Shielding

Applications

- Professional Audio Encoding
- Digital Telecommunications
- Automatic Test Equipment
- High-Resolution Imaging
- Seismic Instrumentation
- Medical Data Acquisition
- Satellite Communications
- Multiplexed Data Acquisition

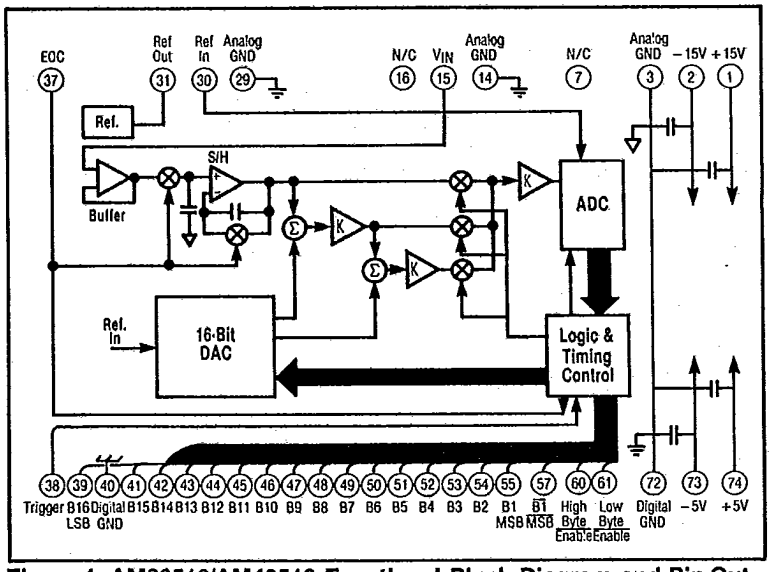


Figure 1. AM30516/AM40516 Functional Block Diagram and Pin-Out.

SPECIFICATIONS(1) T-51-10-16

ANALOG INPUT

Input Range
±5V (2)

Input Bias Current
500 nA

Input Capacitance
10 pF

Input Impedance
100 MΩ

DIGITAL INPUTS

Logic Levels
Logic "0"
0.8V Max.

Logic "1"
2.0V Min.

Logic Currents
Logic "0"
−0.4 mA

Logic "1"
20 μA

Trigger Pulse Width
50 ns Min.

High Byte Enable
Active Low B1-B8, B1

Low Byte Enable
Active Low B9-B16

DIGITAL OUTPUTS

Fan-Out
2 TTL Loads Max.

Output Coding
Complementary Offset Binary

Output Voltage
Logic "0"
0.4V Max.

Logic "1"
2.4V Min.

End of Conversion (EOC)
High During Conversion

REFERENCE

Internal Reference Output Voltage
−6.5V (1 mA external load)

Recommended Input (3)
−6.5V

Input Impedance
1.6 kΩ

DYNAMIC CHARACTERISTICS

Maximum Throughput Rate
AM30516
125 kHz Min.

AM40516
200 kHz Min.

A/D Conversion Time
5 μs Max.

Signal to Noise Ratio (4,7,8)
1 kHz
95 dB Typ., 90 dB Min.

22 kHz
86 dB

45 kHz
86 dB

Peak Distortion (5,7,8)
1 kHz
−98 dB Min.

22 kHz
−94 dB

45 kHz
−86 dB

Total Harmonic Distortion (6,7,8)
1 kHz
−88 dB Min.

22 kHz
−86 dB

45 kHz
−84 dB

S/H Acquisition
3 μs Max.

S/H Aperture Delay
30 ns Typ., 60 ns Max.

S/H Aperture Jitter
0.2 ns Typ., 0.4 ns Max.

S/H Feedthrough (9)
−86 dB Max.

TRANSFER CHARACTERISTICS

Resolution
16 bits

Quantization Error
±0.5 LSB

Integral Non-Linearity
0.003 % FSR Max.

Differential Non-Linearity
Input ≤ 0.25 FSR
±0.25 LSB Typ.
±0.5 LSB Max.

Input > 0.25 FSR
±0.25 LSB Typ.
±0.75 LSB Max.

Offset Error (10, 11, 12)
±1 mV Max.

Gain Error (10, 11, 12)
0.01% FSR Max.

No Missing Codes
Guaranteed from 0°C to 60°C

A/D Converter Noise
30 μV rms AM30516
40 μV rms AM40516

STABILITY (0°C to 60°C)

Differential Non-Linearity
±0.5 ppm FSR/°C Max.

Offset Voltage
±10 ppm FSR/°C Max.
Gain
±10 ppm FSR/°C Max.
Warm-Up Time
5 minutes Max.
Supply Rejection
Offset
±5 ppm FSR/%
Gain
±5 ppm FSR/%

POWER REQUIREMENTS

Supply Range
±15V Supplies
11.65V Min., 15.45V Max.
±5V Supplies
4.75V Min., 5.25V Max.
±15V Current Drain
AM40516
50 mA
AM30516
40 mA
+5V Current Drain
35 mA
−5V Current Drain
70 mA
Power Consumption
AM40516
2.025W
AM30516
1.725W

ENVIRONMENTAL & MECHANICAL

Temperature Range
Rated Performance
0°C to 60°C
Storage
−25°C to 80°C
Relative Humidity
0 to 85% Non-condensing up to 40°C
Dimensions
3" x 4" x 0.44"
Shielding
Electromagnetic 5 sides
Electrostatic 6 sides
Case Potential
Ground

Notes

1. Unless otherwise noted, all specifications apply at 25°C.
   Supplies are ±15V and ±5V. Full-scale range is ±5V.
2. For 0-10V range, consult factory.
3. Reference input is optional. If it is not used, Ref In must be jumpered to Ref Out.
4. Signal to Noise Ratio represents the ratio of the rms value of the signal to the total rms noise below the Nyquist rate. The total rms noise is computed by: (1) summing the noise power in all frequency bins not correlated with the test signal; (2) estimating the total noise power contained in all harmonic frequency bins; and (3) computing the rms noise from the sum of (1) and (2).
5. Peak Distortion represents the ratio of the highest spurious frequency component below the Nyquist rate to the signal. Note that in computing Peak Distortion the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 3.
6. Total Harmonic Distortion represents the ratio of the rms sum of all harmonics up to the 40th harmonic to the rms value of the signal.
   Note that in computing Total Harmonic Distortion the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 3.
7. 3.5V rms input signal.
8. AM30516 tested and guaranteed with Analogic's SHA2400 Sample-and-Hold.
9. Measured with 10V step with 20V/μs rise time.
10. For external offset and gain adjust option, consult factory.
11. Refer to "Output Coding and Trim Procedure" for field adjustable gain and offset procedures.
12. With use of internal reference only.
13. Includes noise from S/H and A/D converter.

Performance Features (cont.)

that both minimizes parts count and yields unprecedented stability, linearity, and accuracy. To achieve its superior performance, the AM30516/AM40516 relies on a proprietary reference D/A converter that has inherent 16-bit accuracy and linearity. The D/A converter, in conjunction with logic circuitry in a specialized gate array, detects and corrects inaccuracies and linearity errors that could arise from the flash A/D converter and amplifier circuitry in the conversion path. For users who wish to effect a fine trim of the AM30516/AM40516's offset and gain parameters, the converter has easily accessible offset-trim and gain-trim potentiometers. The AM30516/ AM40516 comes in a convenient 3" X 4" module with 0.1" pin spacings for easy installation on printed-circuit boards. The specifications of the AM30516/AM40516 are fully ensured by thorough, computer-controlled factory tests.

Output Coding and Trim Procedure

Figure 2 shows the output coding of the AM30516/AM40516 A/D converter. The coding format is complementary offset binary. The term "complementary" applies because the output codes change from 0000000000000000 toward 1111111111111111 as the analog input varies from its most positive toward its most negative full-scale value. The term "offset" applies because the input range is bipolar; i.e., the major transition (0111111111111111 to 1000000000000000) occurs at 0V. The input range is therefore "offset" by an amount equal to one-half the full-scale range. The symbol * in Figure 2 indicates a bit that is undergoing a 0-to-1 or 1-to-0 code transition at the indicated analog input voltage.

To trim the offset of the AM30516/AM40516, apply 76 μV to the analog input. Adjust the offset trim potentiometer such that all 16 output lines alternate equally between 0 and 1.

To trim the gain of the AM30516/AM40516, apply 4.999924V to the analog input. Adjust the gain trim potentiometer such that the LSB alternates equally between 0 and 1.

In a particular application the user may prefer to trim −full scale instead of +full scale. In this case, apply −4.999771V to the analog input; adjust the gain trim potentiometer such that the LSB alternates equally between 0 and 1.

TRUTH TABLE		
INPUT VOLTAGE	DIGITAL OUTPUTS MSB	LSB
5.000000V	0000000000000000	
4.999924V	000000000000000*	
4.999847V	0000000000000001	
.	.	
.	.	
0.000153V	0111111111111111	
+0.000076V	**********	
0.000000V	1000000000000000	
.	.	
.	.	
−4.999695V	1111111111111110	
−4.999771V	111111111111111*	
−4.999847V	1111111111111111	

Figure 2. Output Coding for the AM30516/AM40516.

Timing Considerations

The timing diagram in Figure 3 shows the timing characteristics of the AM30516/AM40516 A/D converter. Upon a low-to-high transition of the Trigger input, the EOC (end of conversion) line also switches high. The EOC line in turn switches the internal sample-and-hold amplifier to Hold mode; the S/H amplifier remains in Hold mode for the 5 μs duration of the A/D conversion period. At the end of the 5 μs A/D conversion period, the EOC line goes low and switches the sample-and-hold amplifier to Sample mode. At the 125 kHz throughput rate shown in Figure 3, the sample-and-hold amplifier then has 3 μs to sample (acquire) a new signal level for the next conversion cycle. The TTL-level Trigger input should have a minimum pulse width of 50 ns. Note that the data for a given conversion cycle becomes valid approximately 20 ns before the respective high-to-low transition of the EOC line.

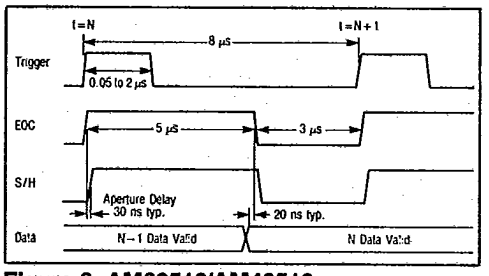


Figure 3. AM30516/AM40516 Timing Diagram.

Layout Considerations

Because of the extremely high resolution of the AM30516/AM40516 A/D converter, it is necessary to pay careful attention to the printed-circuit layout for the device. It is, for example, important to separate the analog and digital grounds and to return them separately to the system power supply. Digital grounds are often noisy or "glitchy", and these glitches can have adverse effects on the performance of the AM30516/AM40516 if they are introduced to the analog portions of the A/D converter's circuitry. At 16-bit resolution, the size of the voltage step between one code transition and the succeeding one is only 153 μV, so it is evident that any noise in the analog ground return can result in erroneous or missing codes. It is therefore important to configure a low-impedance ground-plane return on the printed-circuit board. Note that the ground-potential metal case used for the AM30516/AM40516 provides shielding against electromagnetic interference on 5 sides and against electrostatic interference on 6 sides.

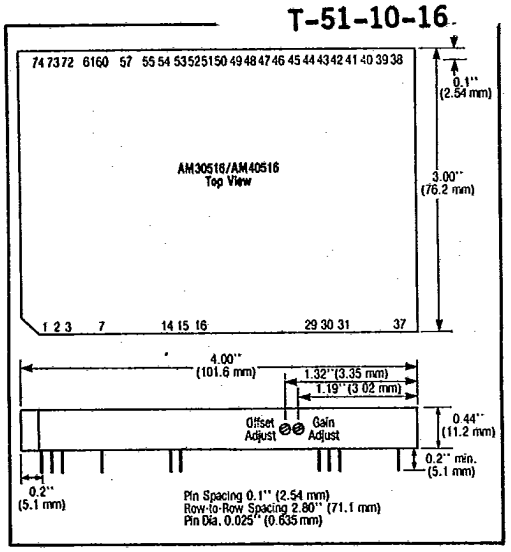


Figure 4. AM30516/AM40516 Outline Drawing & Pinouts.

Principles of Operation

To understand the operating principles of the AM30516/AM40516 A/D converter, refer to Figure 5. The simplified block diagrams in paths a, b, and c in Figure 5 illustrate the three successive passes in the subranging conversion scheme of the AM30516/AM40516. For all three passes, the lines labeled "From Input" come either from the output of the sample-and-hold amplifier (in the AM40516) or from the output of the input buffer amplifier (in the AM30516). In the first pass (a), a switched-gain amplifier attenuates the input signal by a factor of five. It thus converts the 10V full-scale range of the input to the 2V full-scale range of the 6-bit flash A/D converter. The 6-bit A/D converter then digitizes the six MSBs of the input signal. The outputs of the A/D converter drive the six MSBs of the D/A converter. The six output lines of the A/D converter are latched into the logic circuitry of a specialized gate array, which drives the input lines of the D/A converter.

In the second pass (b), a difference amplifier subtracts the D/A converter's output voltage from the input voltage, then amplifies this difference by a factor of 3.2. The switched-gain amplifier now has a gain of two, and thus amplifies the difference voltage further. The output of the switched-gain amplifier again provides the input signal for the 6-bit flash A/D converter. The A/D converter's outputs are latched into the gate array, which supplies the next lower-order bits of the D/A converter. In the gate array, the A/D converter's MSB in the second pass "overlaps" the LSB from the first pass. The resolution of the A/D conversion in the second pass is thus 11 bits (not 12).

In the third pass (c), the gain-of-3.2 difference amplifier subtracts the D/A converter's output voltage from the input voltage. In this pass, an amplifier with a gain of 32 provides additional amplification of the difference signal. The six outputs of the 6-bit flash A/D converter are latched into the gate array; the MSB of this conversion cycle "overlaps" the LSB of the previous cycle.

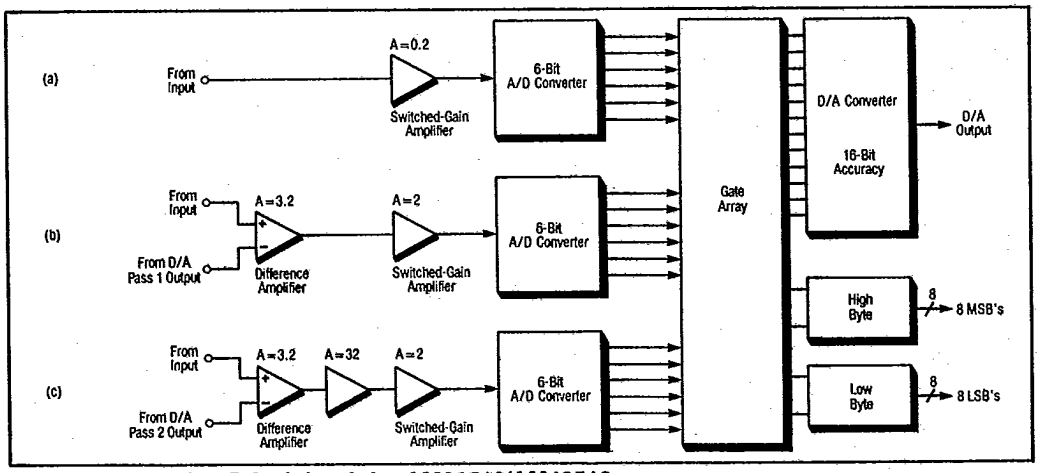


Figure 5. Operating Principle of the AM30516/AM40516.

The effective resolution of the conversion is thus 6 + 5 + 5, or 16 bits. Using the "overlap" structure, logic circuitry in the gate array adds the digital words produced in the three passes and produces the corrected output word. This digital error-correction technique thus provides an output word that is accurate and linear to within the full resolution of the A/D converter. The method corrects for any gain and linearity errors in the amplifying circuitry, as well as in the 6-bit flash A/D converter. Without the error-correction technique, it would be necessary that all the components in the AM30516/AM40516—the difference amplifier, the switched-gain amplifier, and the 6-bit flash A/D converter—be accurate and linear to a 16-bit level. While such a design might be possible to realize on a laboratory benchtop, it would be clearly impractical to achieve in production. The key to the AM30516/AM40516's conversion scheme is the 16-bit-linear D/A converter, which serves as a reference element for the conversion passes as well as for the error-correction mechanism.

The AM30516/AM40516 has a 3-state output structure. Users can enable the eight MSB's, eight LSB's or both, by using the High-Byte Enable and Low-Byte Enable pins (both pins are active low). This feature makes it possible to transfer data from the AM30516/AM40516 to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered; see Figure 10.

Performance Testing

To further instill confidence in our customers, Analogic supplies with each AM30516 or AM40516 a data sheet as proof of 100% testing performed on each device prior to shipping. Such data sheets reflect testing performed both in the "Frequency Domain" and in the "Amplitude Domain".

Amplitude Domain Testing

The Amplitude Domain Testing is performed by proprietary automatic test equipment that includes a 22-bit duty-cycle digital-to-analog converter. A simplified block diagram outlining our Amplitude Domain Test System is shown in Figure 6. The data sheet generated provides the end customer with detailed results on integral linearity, A/D converter noise, absolute accuracy, conversion time, power supply current and power supply rejection. A typical data sheet for the AM40516 is shown in Figure 7. Although the above specifications appear to be straight-forward, a great deal of attention should be placed by the customer in order to ensure that the parameters are properly tested. Following is a list of Analogic's major definitions as tested with our "Amplitude Domain" test systems:

A/D Converter Noise: Errors at the output code caused by signals present other than the signal source. In the AM40516, A/D converter noise includes noise from the S/H and the A/D converter; in the AM30516, A/D converter noise includes noise from the input buffer and the A/D converter.

Integral Linearity: A measure of the maximum deviation (after calibration) of the output digital codes from the best-fit straight line through the transfer function, expressed as a percentage of the full scale range. A least squares algorithm is used to determine best fit.

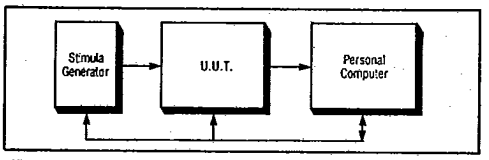


Figure 6. "Amplitude Domain" Test System.

Differential Linearity: A measure of the maximum deviation of any particular code width from the ideal code width,expressed as a fraction of an LSB.

$$\text{Differential Linearity} = \left| \frac{V_{MAX} - V_{LSB}}{V_{LSB}} \right| \text{LSB's}$$

where: V_{MAX} = maximum (or minimum) code width

Absolute Accuracy Error: A measure of the largest static difference between the actual output code and that predicted by the ideal transfer function, a worst case summation of all error sources, expressed as a percentage of full scale.

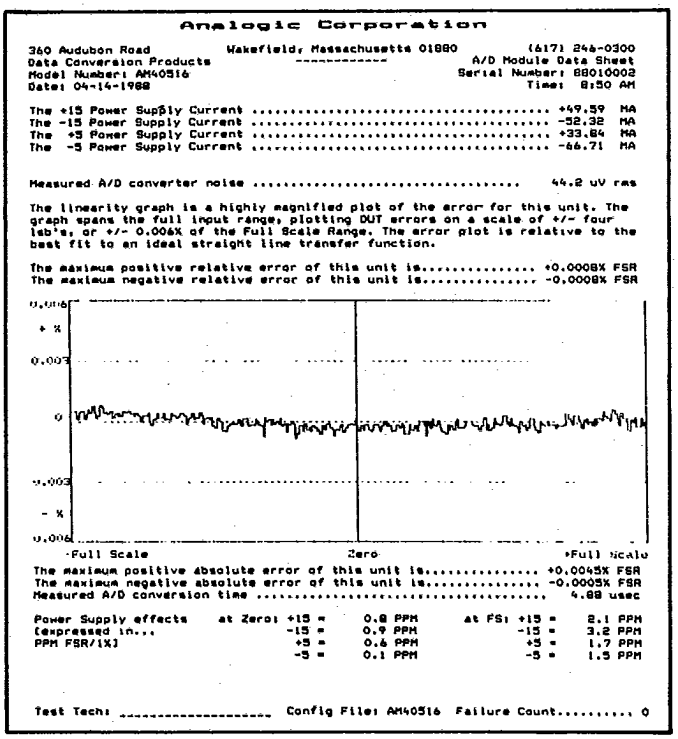
Absolute Accuracy measurements must be referenced to a standard traceable to the NBS with at least an order of magnitude more accuracy than the unit under test.

A/D Conversion Time: Time measured from the rising edge of EOC (the time when the T/H goes into hold) to the falling edge of

EOC. The maximum limit is based on allowing sampling rates up to 125 kHz including a T/H.

Frequency Domain Testing

The Frequency Domain Testing is performed by means of proprietary automatic test equipment inclusive of an ultra-high speed Array Processor manufactured by Analogic. The power of the processor provides us with a great deal of flexibility in both gathering and formatting the data. While a Rosenfeld window is applied on a standard basis, other types of windows such as Blackman-Harris and Blackman are available for customized testing. The number of samples can be varied from 512 to 8192, and the system can average up to 64 FFT's. A block diagram of the "Frequency Domain" test system is shown in Figure 8; a typical data sheet of an AM40516 tested over frequency is shown in Figure 9.



Analogic Corporation

360 Audubon Road Wakefield, Massachusetts 01880 (617) 246-0300
Data Conversion Products A/D Module Data Sheet
Model Number: AM40516 Serial Number: 88010002
Date: 04-14-1988 Time: 8:50 AM

The +15 Power Supply Current ..... +49.59 MA
The -15 Power Supply Current ..... -52.32 MA
The +5 Power Supply Current ..... +33.84 MA
The -5 Power Supply Current ..... -66.71 MA

Measured A/D converter noise ..... 44.2 uV rms

The linearity graph is a highly magnified plot of the error for this unit. The graph spans the full input range, plotting OUT errors on a scale of +/- four lsb's, or +/- 0.006% of the Full Scale Range. The error plot is relative to the best fit to an ideal straight line transfer function.

The maximum positive relative error of this unit is..... +0.0008% FSR
The maximum negative relative error of this unit is..... -0.0008% FSR

0.006
+ %
0.003
0
-0.003
- %
-0.006
-Full Scale Zero +Full Scale

The maximum positive absolute error of this unit is..... +0.0045% FSR
The maximum negative absolute error of this unit is..... -0.0005% FSR
Measured A/D conversion time ..... 4.88 usec

Power Supply effects (expressed in... PPM FSR/1%)	at Zero:		at FS:	
	+15 =	0.8 PPM	+15 =	2.1 PPM
	-15 =	0.9 PPM	-15 =	3.2 PPM
	+5 =	0.6 PPM	+5 =	1.7 PPM
	-5 =	0.1 PPM	-5 =	1.5 PPM

Test Tech: _____ Config File: AM40516 Failure Count..... 0

Figure 7. "Amplitude Domain" Data Sheet.

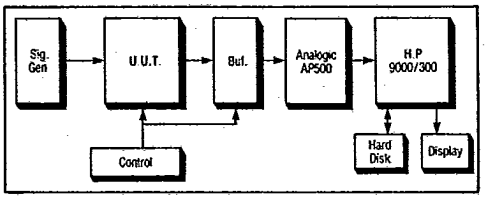


Figure 8. "Frequency Domain" Test System.

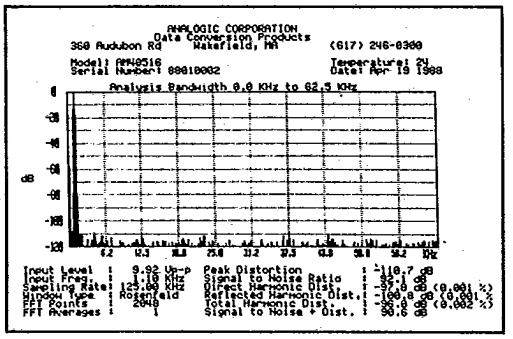


Figure 9. "Frequency Domain" Data Sheet.

Typical Application

Figure 10 shows a typical application circuit for the AM30516/AM40516 16-bit A/D converter. This circuit provides simultaneous sampling of eight bipolar analog-input channels. Simultaneous sampling is a necessity in conversion systems in which the phase, as well as amplitude, relationship between different signals is an important parameter. One example is in seismic measurements, in which it's crucial to know the phase relationship between the signals generated by different sensors. This application circuit performs simultaneous sampling by "freezing" the signal levels of eight analog-input channels at the same instant of time. The differential multiplexer then presents these signal levels, either sequentially or in any user-programmed order, to the AM30516/ AM40516 A/D converter via a differential amplifier. Although the input signals to this circuit are essentially single-ended, the use of a differential multiplexer and a differential amplifier eliminates the possibility of errors arising from common mode voltages.

The minicomputer or microprocessor in Figure 10 provides the sequence and timing information to the control logic. The control logic then performs the task of switching the sample-and-hold amplifiers from Sample to Hold mode and vice-versa, selecting the appropriate input channel and triggering the AM30516/ AM40516 A/D converter. By using two resistors with each SHA2410 sample-and-hold amplifier, a user can program the SHA2410s to provide the gain required to match the input signals to the ±5V full-scale range of the AM30516/AM40516 A/D converter. In the application circuit of Figure 10, for example, the four inputs shown have full-scale ranges of ±1, ±2, ±3, and ±5V. The eighth input channel has the proper full-scale range of ±5V, so gain-setting resistors are not required. Because the SHA2410s provide the sample-and-hold function in this circuit, the AM30516, which does not include a sample-and-hold amplifier, is an appropriate choice.

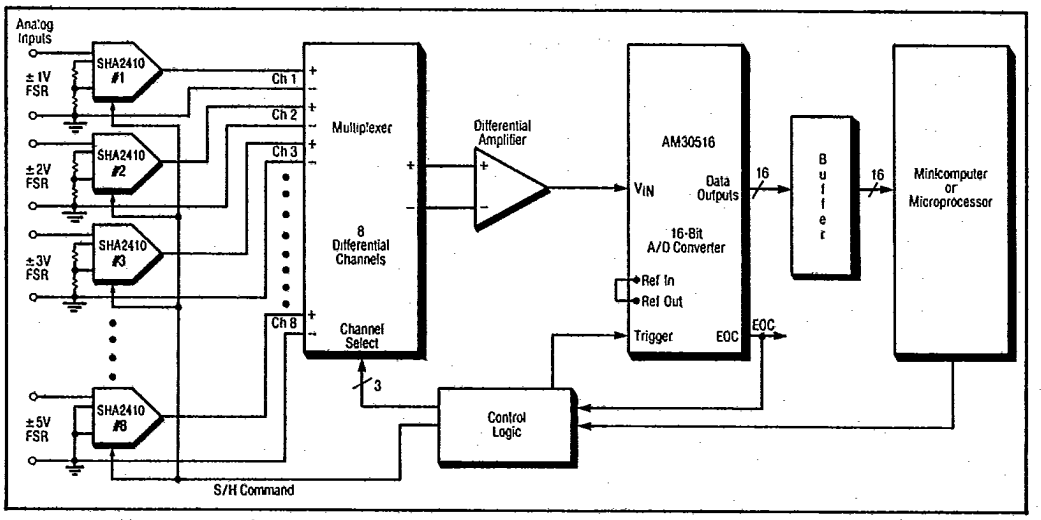


Figure 10. Typical Application Circuit for the AM30516.

ORDERING GUIDE

16-Bit 125 kHz Sampling A/D Converter
Specify **AM40516**

16-Bit 200 kHz A/D Converter
Specify **AM30516**