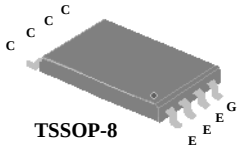
AP28G40GEO

RoHS-compliant Product

Advanced Power Electronics Corp.

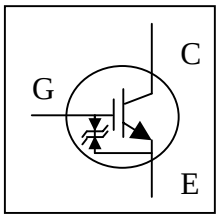
N-CHANNEL INSULATED GATE BIPOLAR TRANSISTOR

- ▼ High Input Impedance
- ▼ High Peak Current Capability
- ▼ Low Gate Drive
- ▼ Strobe Flash Applications



TSSOP-8

V_{CE}	400V
I_{CP}	150A



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CE}	Collector-Emitter Voltage	400	V
V_{GEP}	Peak Gate-Emitter Voltage	± 6	V
I_{CP}	Pulsed Collector Current, V_{GE} @ 2.5V	150	A
P_D@T_A=25℃ [1]	Maximum Power Dissipation	1	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	150	℃

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{GES}	Gate-Emitter Leakage Current	V_{GE}=± 6V, V_{CE}=0V	-	-	±10	uA
I_{CES}	Collector-Emitter Leakage Current	V_{CE}=400V, V_{GE}=0V	-	-	10	uA
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	V_{GE}=2.5V, I_{CP}=150A (Pulsed)	-	5.2	9	V
$V_{GE(th)}$	Gate Threshold Voltage	V_{CE}=V_{GE}, I_C=250uA	0.3	-	1.2	V
Q_g	Total Gate Charge	I_C=40A	-	76	130	nC
Q_{ge}	Gate-Emitter Charge	V_{CE}=200V	-	4	-	nC
Q_{gc}	Gate-Collector Charge	V_{GE}=4V	-	26	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{CC}=320V	-	220	-	ns
t_r	Rise Time	I_C=160A	-	800	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=10Ω	-	1.6	-	μs
t_f	Fall Time	V_{GE}=4V	-	1.5	-	μs
C_{ies}	Input Capacitance	V_{GE}=0V	-	4485	8240	pF
C_{oes}	Output Capacitance	V_{CE}=30V	-	44	-	pF
C_{res}	Reverse Transfer Capacitance	f=1.0MHz	-	40	-	pF
Rth_{JA} [1]	Thermal Resistance Junction-Ambient		-	-	125	℃/W

Notes:

1.Surface mounted on 1 in^2 copper pad of FR4 board, t=10s.

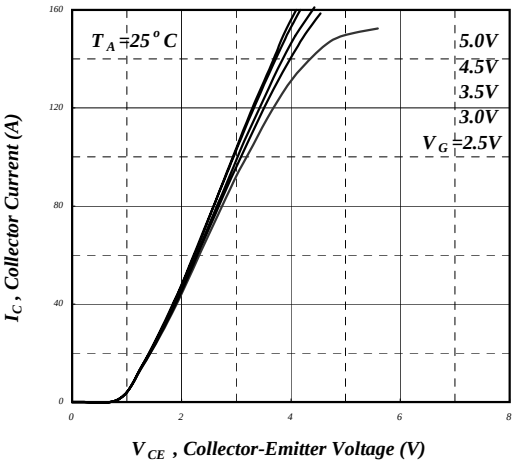


Fig 1. Typical Output Characteristics

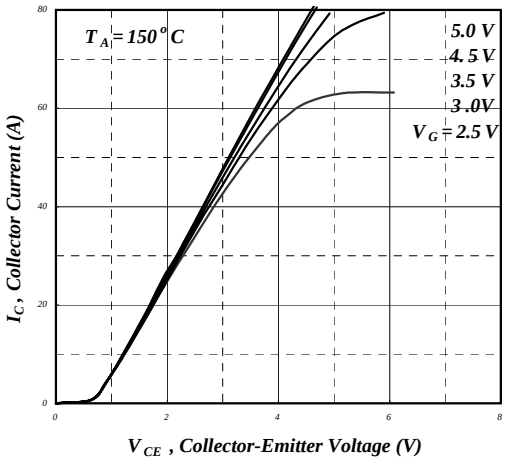


Fig 2. Typical Output Characteristics

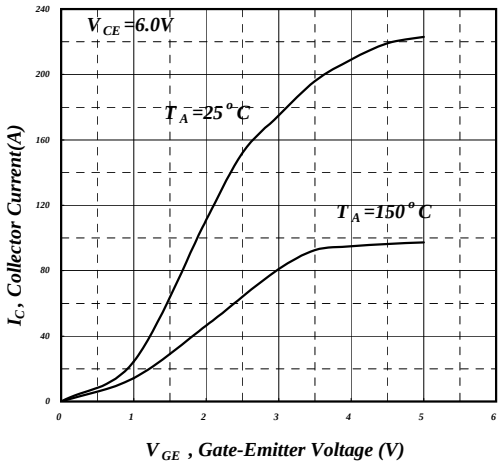


Fig 3. Collector Current v.s. Gate-Emitter Voltage

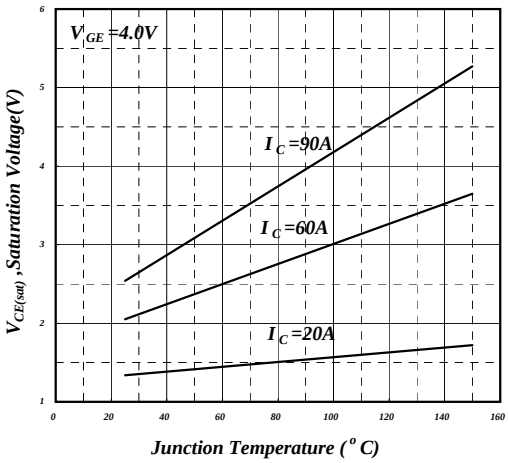


Fig 4. Collector- Emitter Saturation Voltage v.s. Junction Temperature

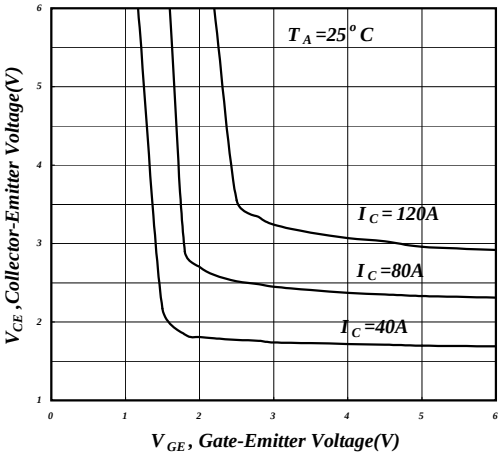


Fig 5. Collector Current v.s. Gate-Emitter Voltage

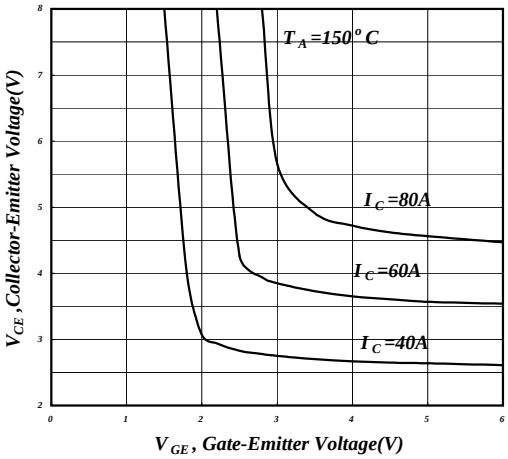


Fig 6. Collector Current v.s. Gate-Emitter Voltage

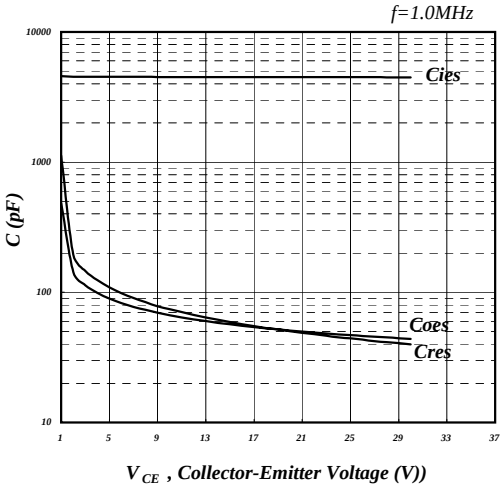


Fig 7. Typical Capacitance Characterisitics

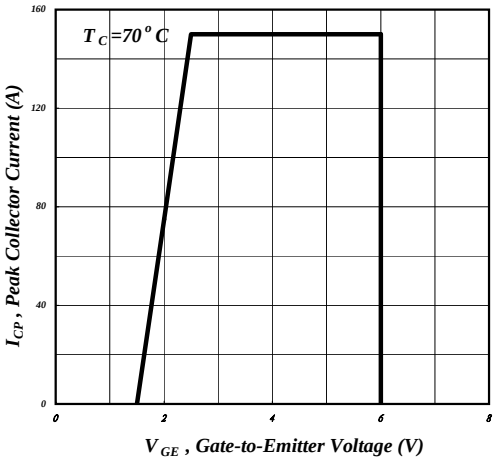


Fig 8. Maximum Pulse Collector Current

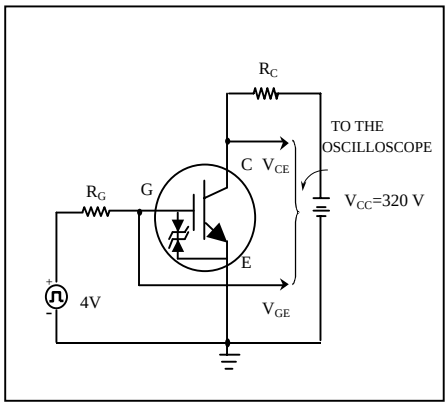


Fig 9. Switching Time Test Circuit

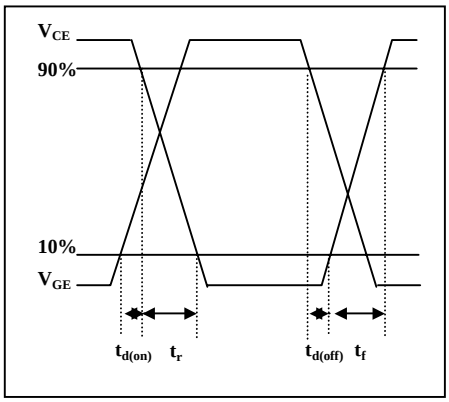


Fig 10. Switching Time Waveform

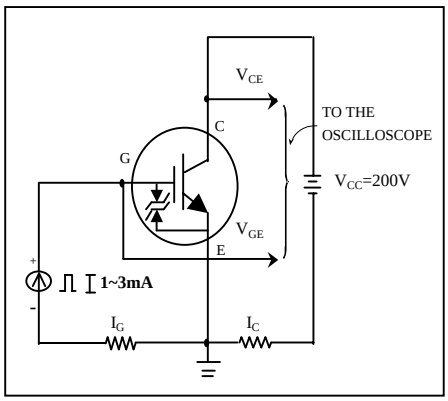


Fig 11. Gate Charge Test Circuit

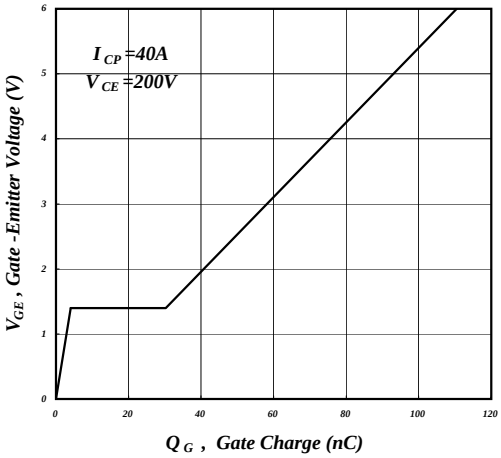


Fig 12. Gate Charge Waveform

dV/dt Design Notice

You should be design dV/dt value is below 400V/us, R_G=30Ω when IGBT turn off.

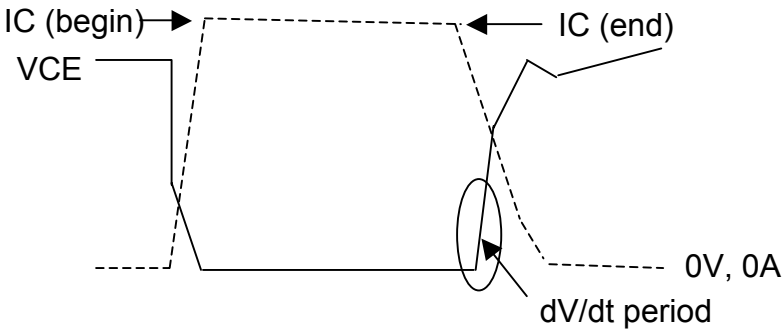
- Definition of dV/dt

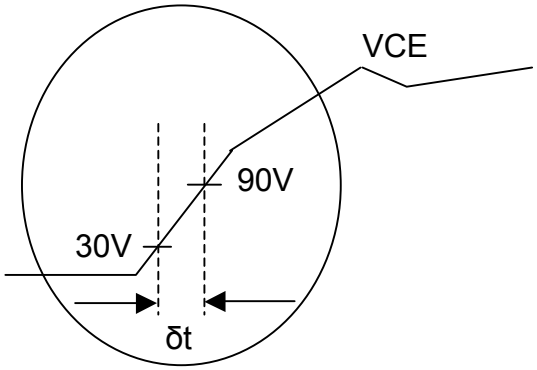
The slope of VCE from 30V to 90V

dv/dt = (90V-30V) / δt)

= 60V / δt

- Waveform





Caution on Usage

This product is senstive to electrostatic discharge, please handle with caution.