Dual Power Management Switches

General Description

The AV9312/9512 Power Management Integrated Switches are designed for 3 and 5 Volt systems that need to switch steady state currents of up to 500mA. These are self contained parts requiring no external components. The AV9312 and AV9512 contain two power switches, and are available in either 14 pin PDIP or 150 mil wide 14 pin SOIC package.

The N-Channel FET switches have a typical 0.2Ω on- resistance, with a maximum of 0.3Ω. For switching currents larger than 500mA, these transistors can be paralleled together. The +2.7V to +3.7V input supply range, the low quiescent current and the automatic power down features make the AV9312 ideal for battery-powered switching and control applications, such as notebook computers, portable medical analyzers and test equipment.

The "soft turn-on" feature of the 9312/9512 ensures that there will be no spikes on the switched power supply when the power turns on to the load.

The 9312 operates with a supply voltage of 2.7 to 3.6V while the 9512 operates with a supply voltage of 4.5 to 5.5V. Either part can switch loads from 2.7V to 5.5V.

Features

- AV9312: 3.0 or 3.3V operating supply voltage
- AV9512: 5V operating supply voltage
- Switches loads from 2.7V to 5.5V
- 0.2Ω typical, 0.3Ω max switch resistance
- Steady state current of 500mA per switch
- Automatic Power Down
- 1 msec FET soft turn on
- No external components required

Applications

- Notebook PC Power Switching
- PCMCIA VCC Switching
- PDA's
- Palmtop Computers
- Hand-Held Medical Instruments

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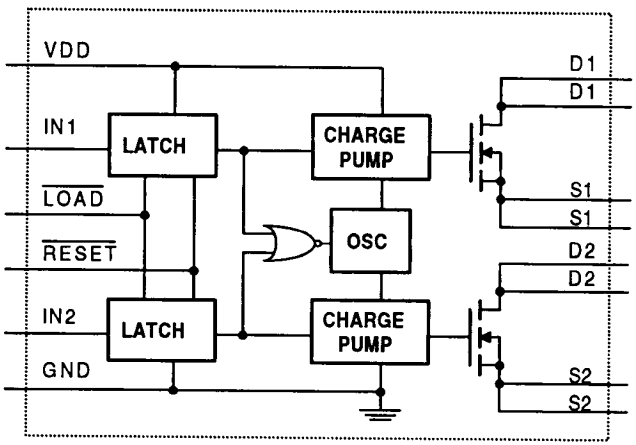
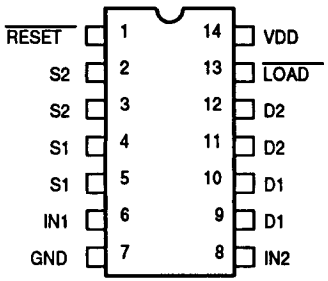
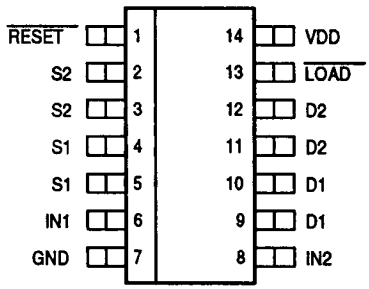
Block Diagram



Pin Configuration



14-Pin DIP (N14)



14-Pin SOIC (M14)

Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	$\overline{\text{RESET}}$	In	Resets input latches and turns all FET switches off when low
2	S2	Out	FET 2 Source, Must be externally connected to Pin 3
3	S2	Out	FET 2 Source, Must be externally connected to Pin 2
4	S1	Out	FET 1 Source, Must be externally connected to Pin 5
5	S1	Out	FET 1 Source, Must be externally connected to Pin 4
6	IN1	In	Logic input to FET 1 driver
7	GND	—	Ground
8	IN2	In	Logic input to FET 2 driver
9	D1	Out	FET 1 Source, Must be externally connected to Pin 10
10	D1	Out	FET 1 Source, Must be externally connected to Pin 9
11	D2	Out	FET 2 Source, Must be externally connected to Pin 12
12	D2	Out	FET 2 Source, Must be externally connected to Pin 11
13	$\overline{\text{LOAD}}$	In	Transparent low latch. A logic "0" on this pin allows data to flow from IN to the FET driver. A logic "1" latches the outputs in their present state.
14	VDD	—	Power Supply for the chip: 2.7 to 3.6V for AV9312 and 4.5 to 5.5V for AV9512

Ordering Information:

Part Number	Temperature Range	Package Type
AV9312CN14	0°C to 70°C	14-lead Plastic DIP (N14)
AV9512CN14	0°C to 70°C	14-lead Plastic DIP (N14)
AV9312CS14	0°C to 70°C	14-lead Plastic SOIC (M14)
AV9512CS14	0°C to 70°C	14-lead Plastic SOIC (M14)

Absolute Maximum Ratings

VDD referenced to GND 7V
Storage temperature ..... –40°C to +125°C
Voltage on I/O pins ..... –.05V to VDD +0.5V
Power dissipation ..... 0.5 Watts

Operating Conditions

Drain Voltage:
AV9312 ..... 2.7V to 5.5V
AV9512 ..... 2.7V to 5.5V
Operating temperature under bias ..... 0°C to +70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

AV9312 (Operating V_{DD}=+2.7 to +3.7V, T_A=0°C to 70°C unless otherwise stated)
AV9512 (Operating V_{DD}=+4.5 to +5.5 V, T_A=0°C to 70°C unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics						
Chip supply	V_{DD}	AV9312	2.7	3.3	3.7	V
Chip supply	V_{DD}	AV9512	4.5	5	5.5	V
Switch Drain Voltage	V_{DF}(1)		2.7		5.5	V
Switch Source Voltage	V_{SF}		V_{DF} –0.2		V_{DF}	V
Input Low Voltage	V_{IL}		V_{SS}		0.2V_{DD}	V
Input High Voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Switch Current	I_{DF}		0		500	mA
Supply Current	I_{DD2}(2)	All switches active		100	200	µA
Standby Current	I_{DDSB}	All switches off		2	4	µA
Input Low Current	I_{IL}	V_{IN} = 0V		-	-2	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}		-	2	µA
Switch on Resistance	R_{ON}	All conditions		.2	.3	Ω
Switch on Resistance	R_{ON}	25°C,V_{DF}=3.3V		.15		Ω
AC Characteristics						
$\overline{LOAD}$ Pulse Width	t_W		50		-	ns
IN_X to LOAD Inactive Setup Time	t_{SU}		20		-	ns
LOAD inactive to IN_X Hold Time	t_{HD}		10			ns

Note 1: In addition to the power dissipated by the oscillator and 2 charge pumps, the drop across the switches also contributes to the on chip power. This power per switches is given by: $I_{DF}(V_{DF}–V_{SF})$. The total on-chip power should be held below 0.5W.

Note 2: The current consumed by the IC is proportional to the number of switches on. If only 1 FET is on, I_{DD} will be 1/2 of specified value.

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Device Description

Each switch channel consists of a transparent latch, charge pump, and N-Channel FET. Logic inputs to the drivers are latched when $\overline{LOAD}$ goes high. The logic high signal from the latch activates the charge pump and, a few milliseconds later, the FET is fully turned on. On chip circuitry controls the FET turn on, which typically takes 1ms (fig 2.), to avoid the power supply current spikes (fig. 1) which would occur if the switch turned on fast into a fully discharged load capacitance. The chip has a common oscillator that drives the 2 charge pumps and runs at approximately 500KHz.

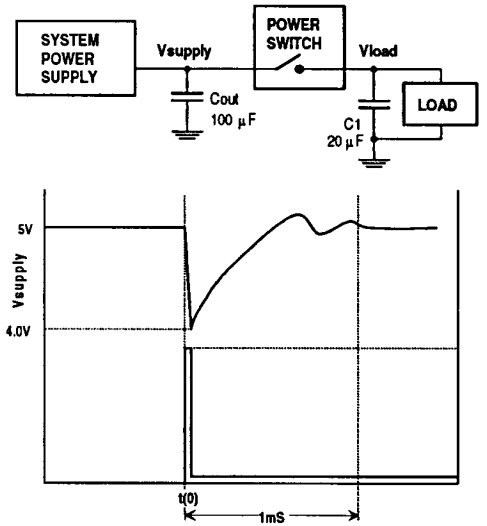

Figure 1. Power Supply glitch caused by fast T_{ON}

The automatic power down feature works by monitoring the latch outputs. When all the latch outputs are at a logical zero, the output of the NOR gate is high and powers down the oscillator to conserve power.

The AV9312/9512 FETs do not contain source to drain diodes. If the part is used for switching inductive loads, an external diode should be connected across the FET.

The source pins and drain pins should be connected together externally for each output switch to obtain minimum switch on resistance. So, D1 (pin#9) should be connected to D1 (pin #10) and likewise with D2, S1, and S2.

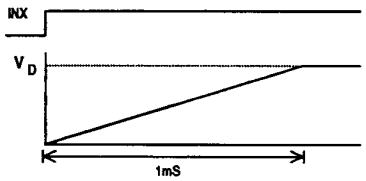

Figure 2. ICS9312/9512 controlled output rise-time

To insure the FET switches are off, the $\overline{RESET}$ pin should be pulsed low.

An edge detector monitors the 4 latch outputs and activates the timer when any output goes high . The Ready signal, which comes from the timer, goes low immediately and then goes high again typically in 6ms, thus generating a negative going pulse (see Figure 1). Ready returns to the high state when output FET is stable and fully turned on.

The automatic power down feature works by monitoring the latch outputs. When all the latch outputs are at a logical zero, the output of the NOR gate is high and asserts the power down to the oscillator.

The AV9312/9512 FETs do not contain source to drain diodes, so when the part is used for switching inductive loads an external diode should be connected across the FET.