128Kx9 Monolithic High Speed Synchronous Static RAM

ADVANCE INFORMATION

The EDI2090C is a high performance, 1 megabit synchronous static RAM organized as 128Kx 9 bits, available in six versions.

Inputs are registered or latched on the rising edge of CLK (K), depending on version. The output can be self-timed, registered, or latched, also depending on version.

Address, Data, and Control need to be held valid for a small percentage of cycle time and output timing can be matched to very tight system constraints.

These options allow the designer tremendous flexibility in the design of very high speed computer systems.

Features

128Kx9 bit Synchronous Static Random Access Memory
- Fast Access Times 15, 20 and 25ns
- Works with System Clocks to 65MHz

Thru-hole and Surface Mount Package Options (Proposed)
- DIP
- SOJ

Single +5V (±10%) Supply Operation

Pin Names

AØ-A15	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
G1-$\overline{G2}$	Output Enable
K1-K2	Clock
DQØ-DQ8	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Part No.	Input	Output	#CLK
EDI2090C	Latched	Latched	1
EDI2091C	Registered	Registered	1
EDI2092C	Latched	Asynchronous	1
EDI2093C	Registered	Asynchronous	1
EDI2094C	Latched	Registered	2
EDI2095C	Registered	Registered	2

Pinout

To be determined

Functional Block Diagram