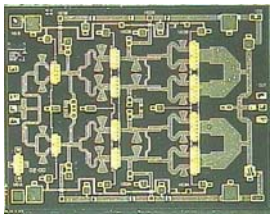
iTR39100
37-40 GHz 1 Watt Power Amplifier MMIC

Description

The iTR39100 is a high efficiency power amplifier designed for use in point to point radio, point to multi-point communications, LMDS and other millimeter wave applications. The iTR39100 is a 3-stage GaAs MMIC amplifier utilizing an advanced 0.15μm gate length Power PHEMT process and can be used in conjunction with other driver or power amplifiers to achieve the required total power output.

Features

- 18 dB small signal gain (typ.)
- 30 dBm saturated power out (typ.)
- Circuit contains individual source vias
- Chip Size 4.28 mm x 3.19 mm x 50 μm



Absolute Ratings

Parameter	Symbol	Value	Unit
Positive DC Voltage (+5 V Typical)	Vd	+ 6	Volts
Negative DC Voltage	Vg	- 2	Volts
Simultaneous (Vd - Vg)	Vdg	+ 8	Volts
Positive DC Current	I_D	1392	mA
RF Input Power (from 50 Ω source)	P_{IN}	18	dBm
Operating Base plate Temperature	T_C	-30 to +85	°C
Storage Temperature Range	T_{Stg}	-55 to +125	°C
Thermal Resistance (Channel to Backside)	R_{jc}	9	°C/W

Electrical Characteristics

(At 25°C) 50 Ω system, Vd=+5 V, Quiescent current (Idq) = 1000 mA

Parameter	Min	Typ	Max	Unit
Frequency Range	37		40	GHz
Gate Supply Voltage (Vg)[1]		-0.2		V
Gain Small Signal Pin=0 dBm	16	18		dB
Gain Variation vs. Frequency		+/-1.5		dB
Power Output at P1 dB Compression		29		dBm
Power Output Saturated (Pin=+14.5 dBm)	28	30		dBm
Drain Current at Pin=0 dBm		1000		mA

Parameter	Min	Typ	Max	Unit
Drain Current at P1 dB Compression		1160		mA
Drain Current at Psat		1200		mA
Power Added Efficiency (PAE) at P1dB		17		%
OIP3 (17 dBm/Tone) (10 MHz Tone Sep.)		35		dBm
Input Return Loss (Pin=0 dBm)		10		dB
Output Return Loss (Pin=0 dBm)		7		dB

Note:
1. Typical range of the negative gate voltage is -0.5 to 0.0V to set a typical Idq of 1000 mA.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC Ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 12 mils long corresponding to a typical 2 mil gap between the chip and the substrate material.

Figure 1
Functional Block Diagram

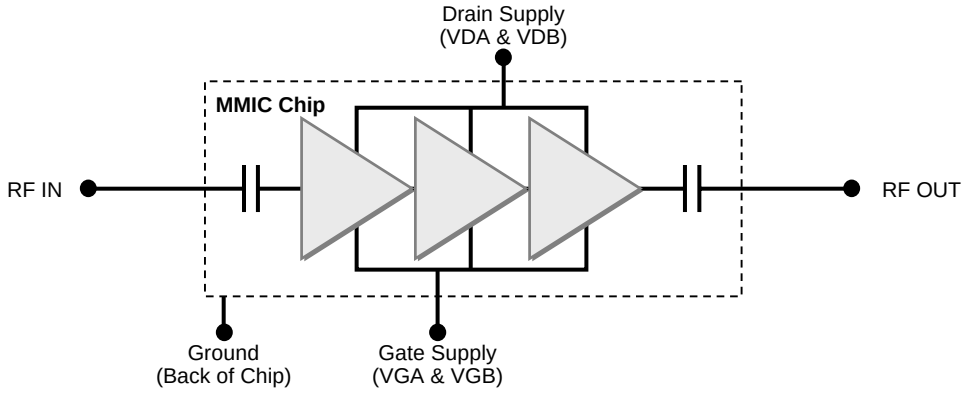

Figure 2
Chip Layout and Bond Pad Locations

(Chip Size=4.28 mm x 3.19 mm x 50 μm. Back of Chip is RF and DC Ground)

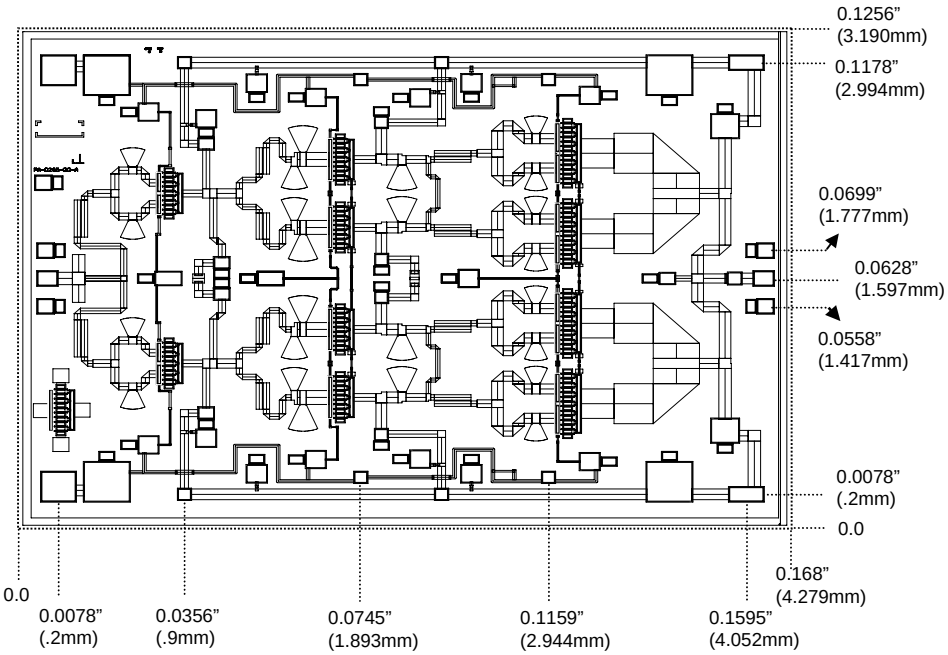

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Figure 3
Recommended Application Schematic Circuit Diagram

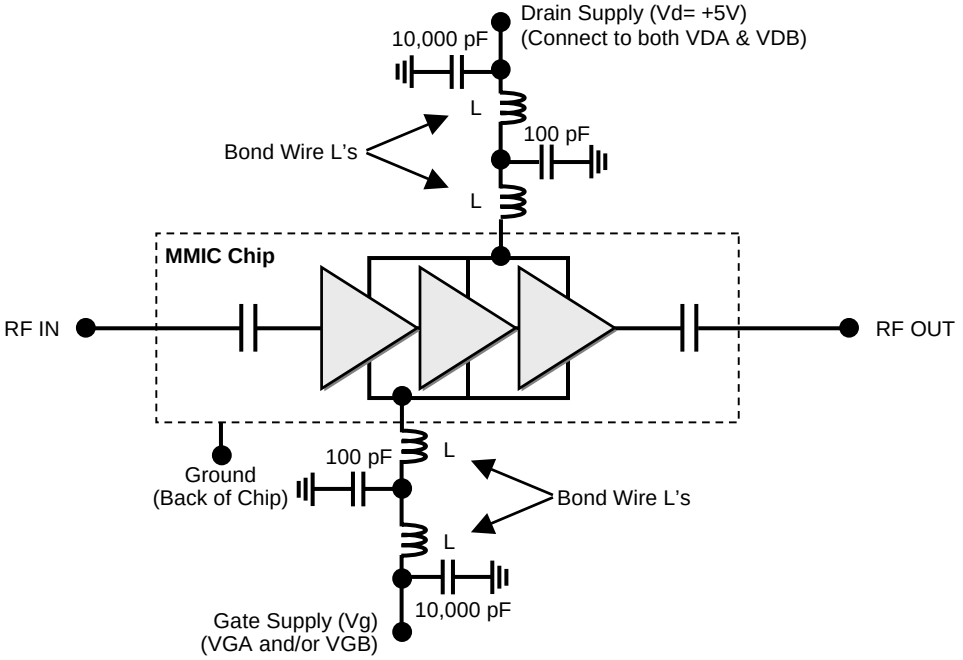
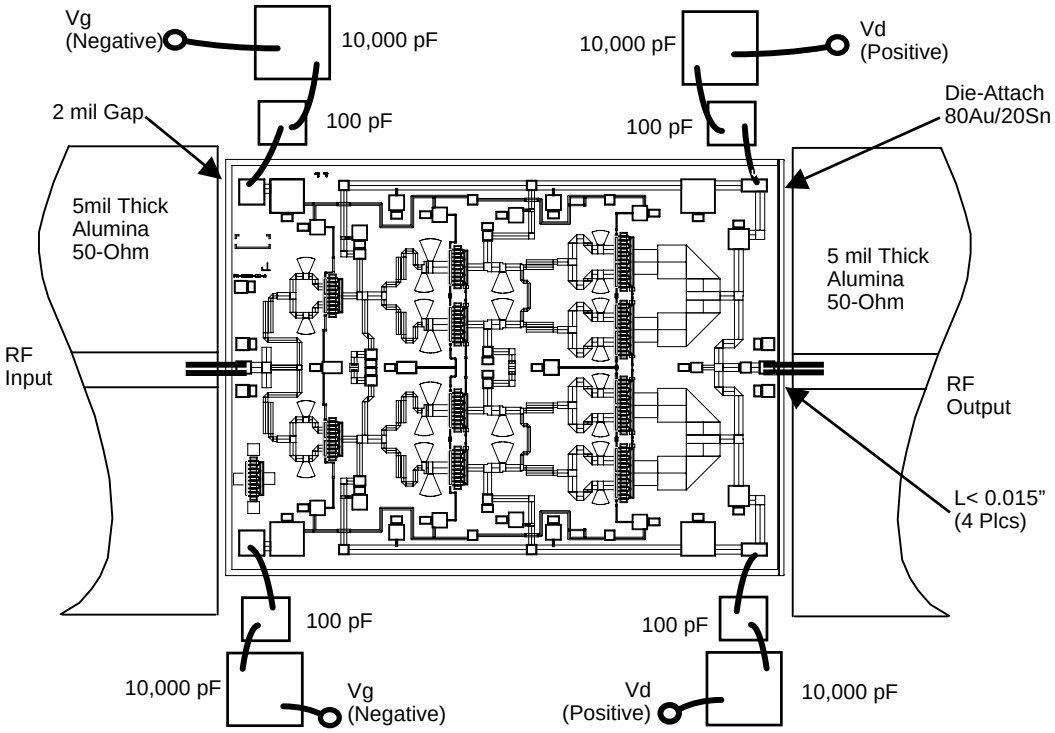


Figure 4
Recommended Assembly and Bonding Diagram



Note:
Use 0.003" x 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief. Vd should be biased from 1 supply on both sides as shown. Vg can be biased from either or both sides from 1 supply.

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Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (Vg) WHILE DRAIN VOLTAGE (Vd) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5 V to Vg.

Step 3: Slowly apply positive drain bias supply voltage of +5 V to Vd.

Step 4: Adjust gate bias voltage to set the quiescent current of Idq=1000 mA.

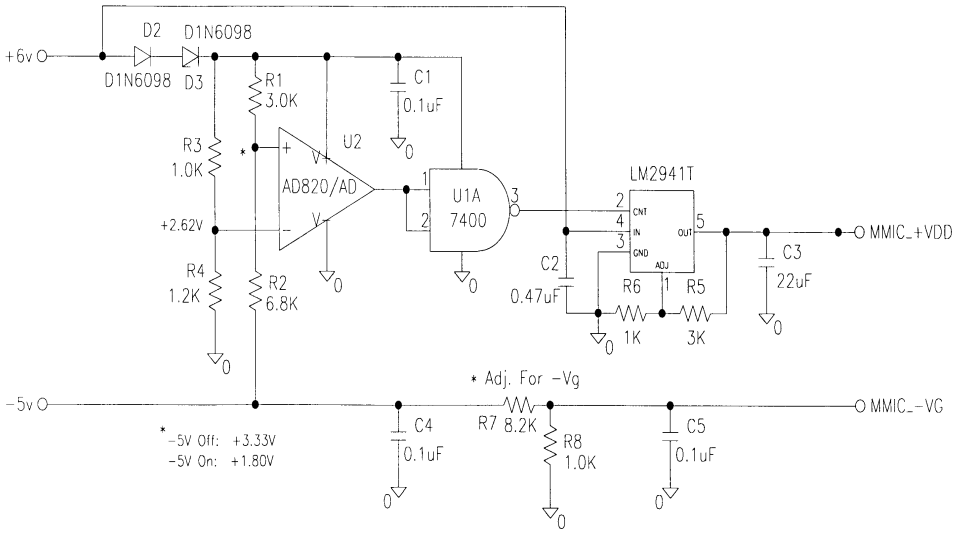
Step 5: After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

(i) Turn off RF input power.
(ii) Turn down and off drain voltage (Vd).
(iii) Turn down and off gate bias voltage (Vg).

Application Information Auto-Bias Circuit

Note:
An example of an auto bias sequencing circuit to apply negative gate voltage and positive drain voltage for the above procedure is shown below.



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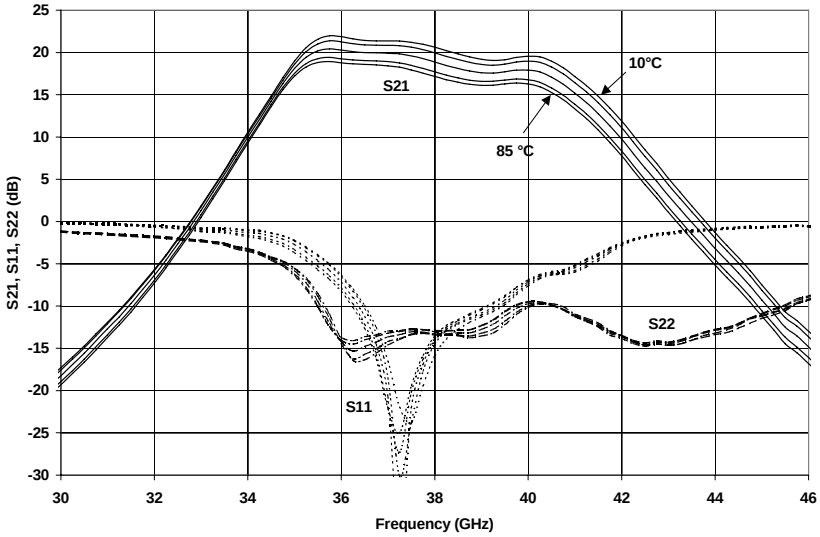
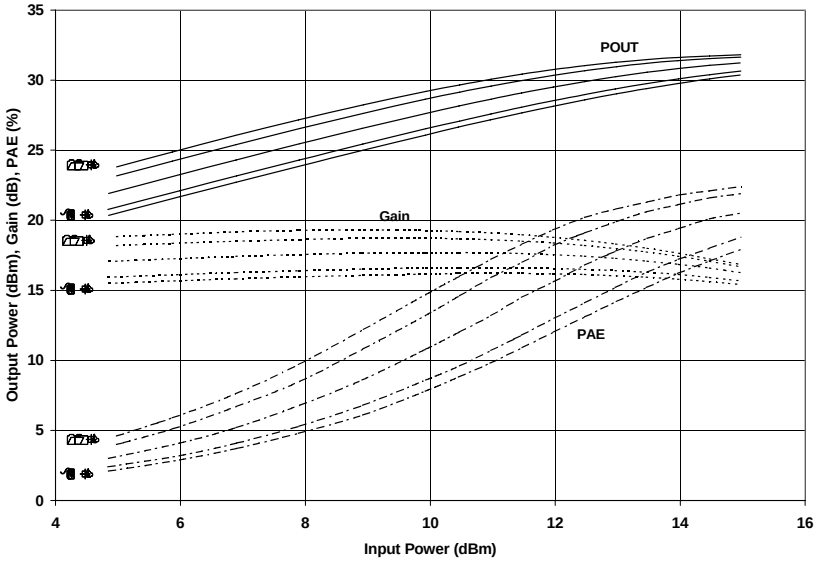
Performance Data

iTR39100 S-Parameters Vs. Frequency Vs. Temperature
Bias Vd=5 V, Id=1000 mA
Base Plate Temp 10, 25, 50, 75, and 85 °C



iTR39100 Power, Gain, PAE Vs. Frequency Vs. Temperature
Frequency =39 GHz, Bias Vd=5 V, Id=1000 mA
Base Plate Temp 10, 25, 50, 75, and 85 °C



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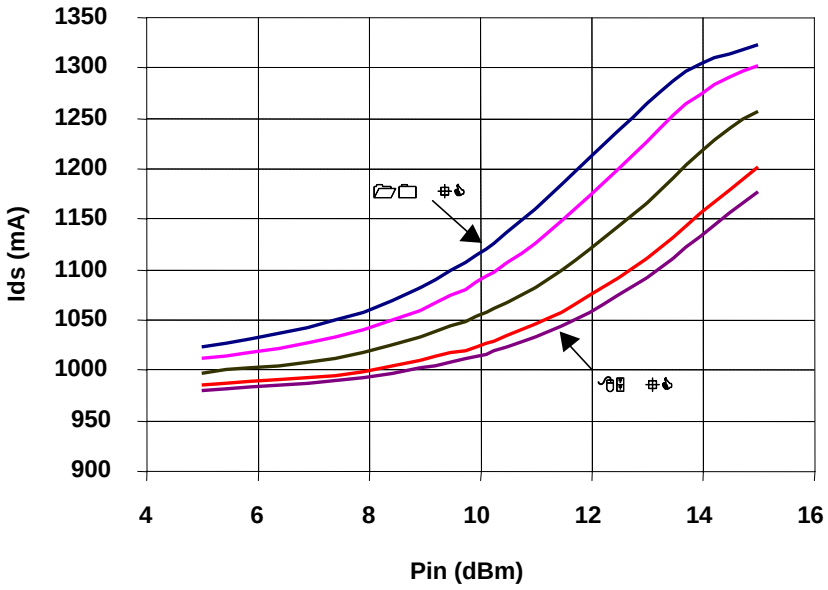
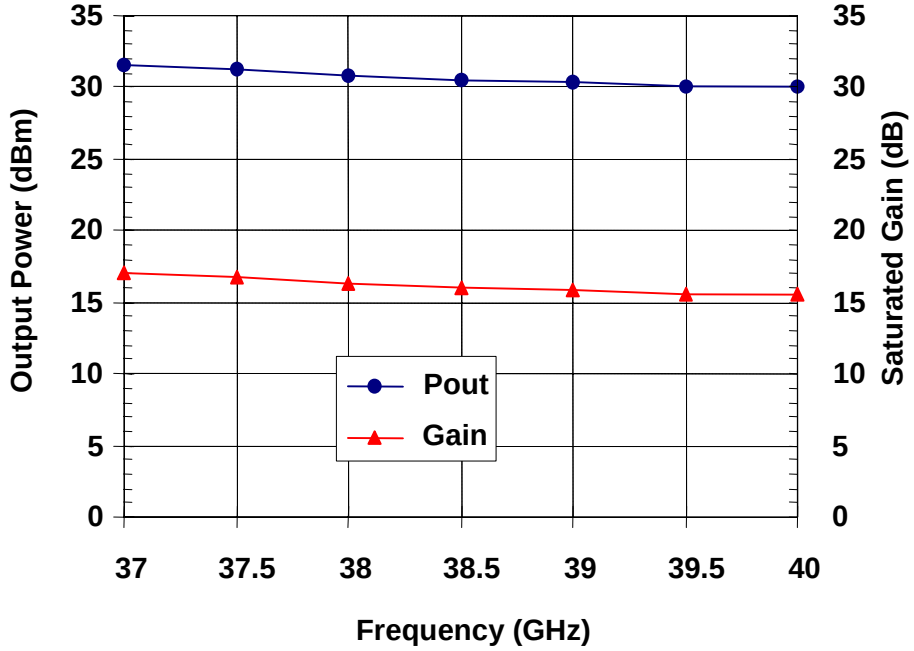
Performance Data

iTR39100 Ids Vs. Pin Vs. Temperature
Frequency =39 GHz, Bias Vd=5 V, Id=1000 mA
Base Plate Temp 10, 25, 50, 75, and 85 °C



iTR39100 Saturated Power and Gain Vs. Frequency
Pin = 14.5 dBm, Bias Vd=5 V, Id=1000 mA T=25 °C



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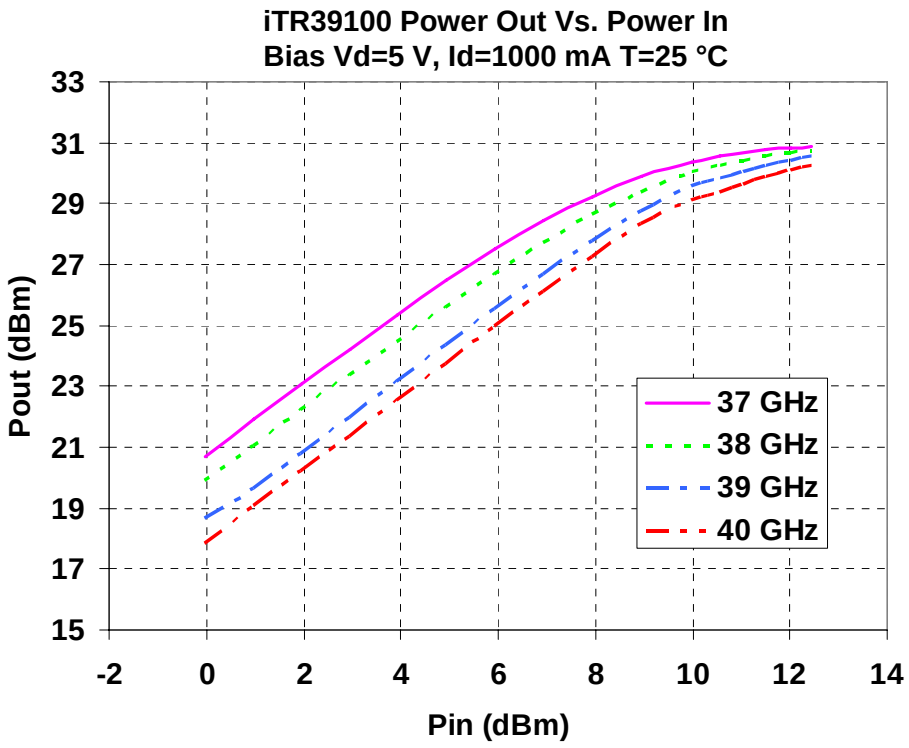

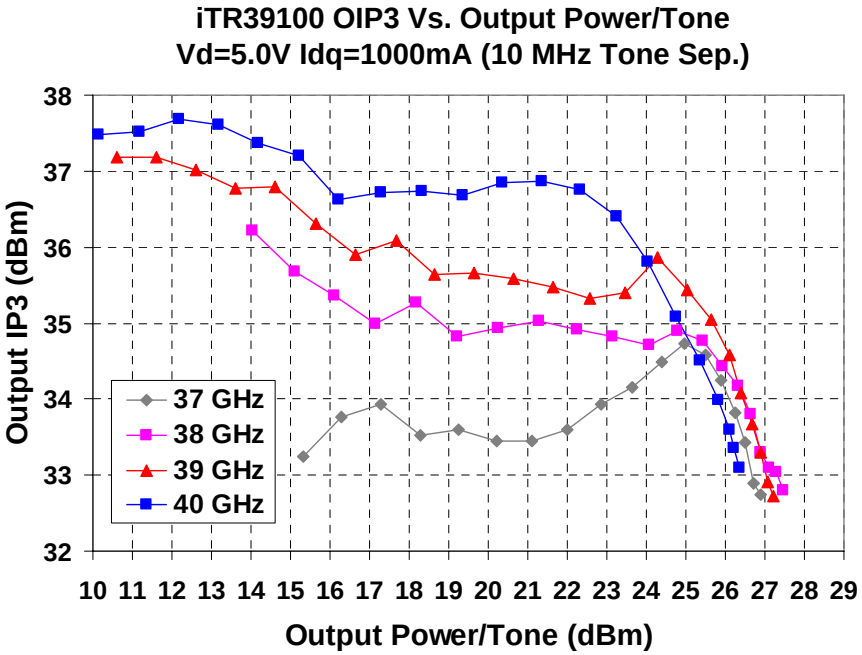

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